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Project memo

Modular Multi-level Energy Storage System

Modelling and design optimization

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ABSTRACT
This document describes the developed design algorithm for a Modular Multi-level Energy Storage System (MM-ESS) based on battery cell technology, along with the modelling of main MM-ESS components for evaluation of total system/components cost, overall volume, overall weight, and system power losses.

The proposed design algorithm has been developed as part of the SINTEF Energy activities within WP3 of SEABAT project, where a Hybrid Energy Storage System for marine applications, based on two different battery cell technologies, is investigated and the MM-ESS has been proposed as core architecture for that purpose.

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VERSION	DATE	VERSION DESCRIPTION
1.0	2022-10-10	First version for comments.
1.1	2022-10-17	Modified/improved the overall volume and weight evaluation by including string cabinet/enclosure model and evaluation. Extra result examples added in chapter 5.
1.2	2023-04-12	Modified/improved battery cell heatsink modelling by including thermal pad material between fin-base structure and cold plates

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Table of contents

1 Preliminaries

1.1 General Methodology

The meta-parametrised meta-modelling approach presented in [1] is adopted as main methodology for the design of the Modular Multi-level Energy Storage System (MM-ESS). This approach is based on mathematical modelling and pareto-frontier multi-objective optimization techniques.

The target is to map the MM-ESS design space into a performance space so the different trade-offs between relevant performance indices can be analysed accounting for the freedom of the free design parameters of the MM-ESS.

1.2 Scope

The scope of this document is to describe the proposed design algorithm for MM-ESS along with the modelling of main MM-ESS components for evaluation of relevant performance indices like component cost, overall volume/weight, and nominal power losses. The proposed design algorithm has been developed as part of the SINTEF Energy activities within WP3 of SEABAT project, where a Hybrid Energy Storage System (HESS) for marine applications, based on two different battery cell technologies, is investigated and the MM-ESS has been proposed as core architecture for that purpose. The main results of application of the MM-ESS architecture for the design of HESS for specific marine applications are reported in [2].

1.3 General considerations

- The design algorithm is focused on exploring the freedoms in circuit/topology parameters and number of components while keeping the same control strategy, sub-module architectures and component technologies, The algorithm can be adapted to other control strategies and/or submodule architectures by modifying the design rules. Different components technologies can be evaluated by running the algorithm with different component parameters representing each technology.
- The Energy storage sub-module is based on Li-ion battery cell technology. However, the topology can be used with other energy storage technologies.
- The proposed MM-ESS design algorithm has been developed considering a required energy storage capacity to be installed and power capability, without linked those requirements to a specific load profile or application. The algorithm can be applied to any application by carrying out a preliminary analysis considering application load profile, desired system lifetime, calendar/cycling properties of the considered core battery cell, so the battery energy system is sized to ensure that the required usable energy by the application is met by the available usable energy at the end of desired battery lifetime. A methodology to select required power and energy ratings based on a given load profile for a battery system is reported in [3]

2 Modular Multi-level Energy Storage System

2.1 System Architecture

Figure 2-1 shows the main architecture of the considered Modular Multi-level Energy Storage System (MM-ESS), which is based on a Modular Multilevel Converter (MMC) topology and liquid cooling system. The MM-ESS is mainly composed of:

- N_{str} independent strings connected in parallel,
- a master controller, which coordinates the power split between the strings,
- HV contactors with feedback, one for each main power terminal,
- an insulation measurement device (IMD),
- a HV main fuse,
- a voltage measurement device, to measure the main MM-ESS voltage,
- the main coolant in/out ports and coolant channels,
- and the emergency off switch.

Each string is mainly composed of:

- N_{mod} modules connected in series, each with two service connectors to easily switch the module, a power supply connector and two coolant ports (in/out),
- a string inductor, to smooth the string current
- a string controller, which controls the string power flow by ensuring the right string voltage level,

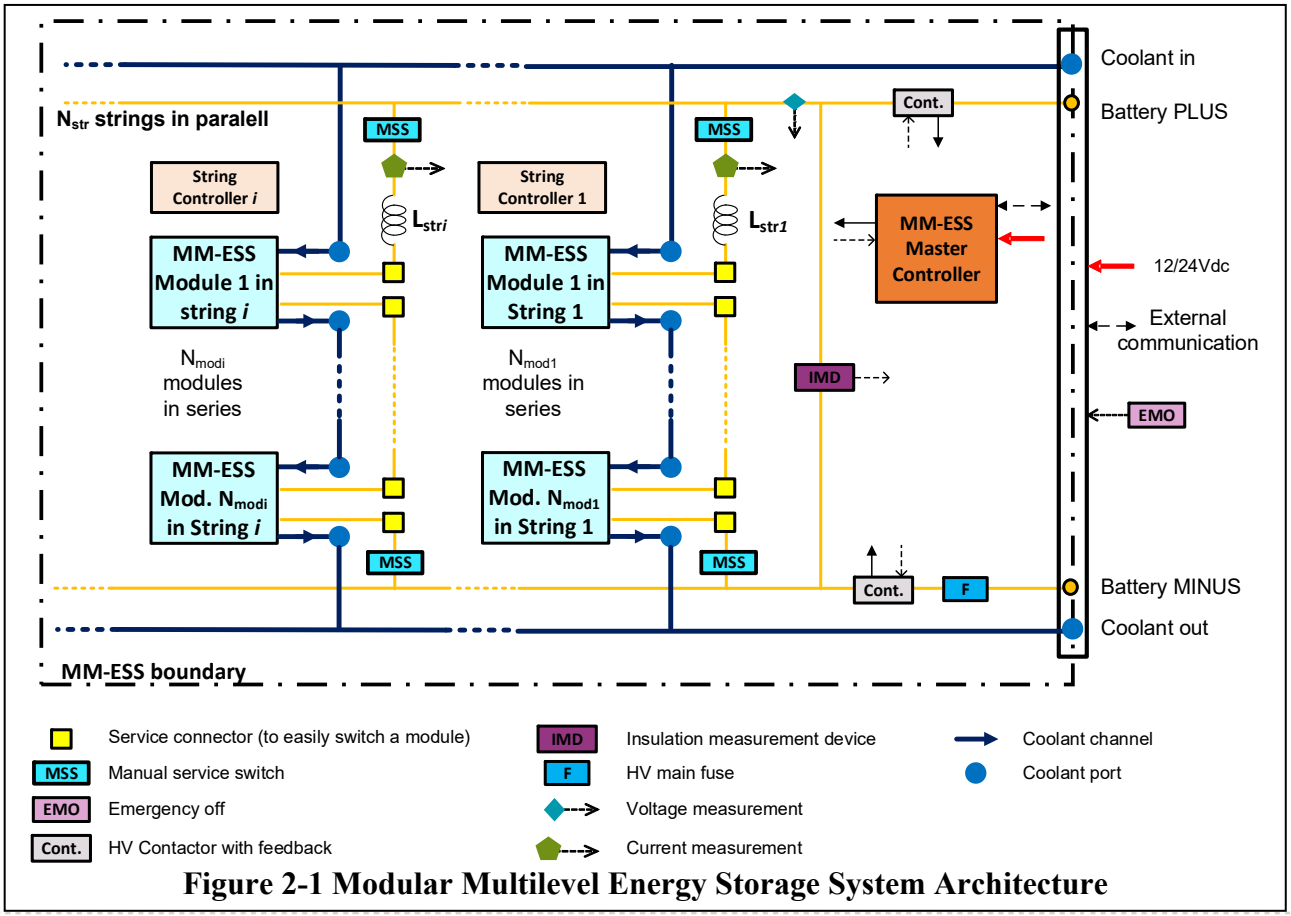


Figure 2-1 Modular Multilevel Energy Storage System Architecture

- a current measurement device, to measure the string current,
- and two manual service switches, to connection/disconnection of the full string,

The key feature of the MM-ESS is the use of energy storage modules with power flow control (by switching on/off the module). Figure 2-2 shows the considered MM-ESS module definition. The module is composed by two main sub-modules: the energy storage sub-module and the power converter sub-module.
The energy storage sub-module is composed by

- a battery cell array (series and/or parallel interconnection of N_{cell} battery cells),
- a battery module heatsink,
- a battery management system (BMS),
- a HV fuse,
- N_{sCell} voltage measurement devices (monitor of cell voltage), assuming that the battery cell array is formed by the series interconnection of N_{sCell} sets of N_{pCell} battery cells parallel connected, (when the battery cell array is formed by the parallel interconnection of N_{pCell} sets of N_{sCell} battery cells series connected, the $N_{sCell}*N_{pCell}$ voltage measurement devices will be needed),
- around ¼ N_{cell} temperature measurement devices (about one for every four cells)
- and two service connectors to easily switch the energy storage sub-module

On the other hand, the power converter sub-module is based on the bidirectional half bridge DC/DC converter topology, and it is composed by:

- two Power Switch Devices (PSDs)
- a capacitor bank,
- a driver circuit and controller,
- a heatsink, to cool the PSDs
- and a voltage measurement device.

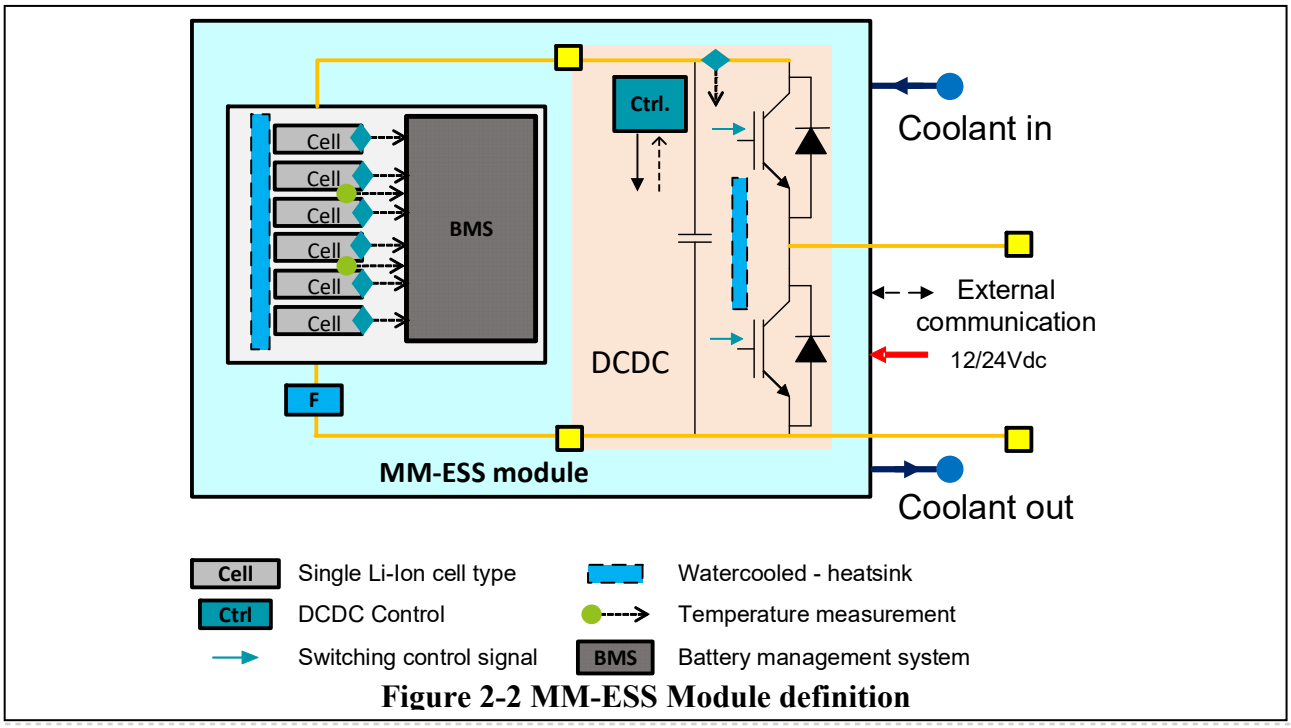


Figure 2-2 MM-ESS Module definition

The use of MM-ESS modules with power flow control functionality brings some flexibility to the system:

- Each string is controlled independently and coordinated by the master controller, so strings with different characteristics can be connected in parallel. The master controller can split the total power to the connected strings based on the maximum string ratings, so strings with higher current ratings supply more current (e.g., proportionally).
- MM-ESS modules with different characteristics (based on different cells and/or power ratings or with different state of health) can be used series connected in the same string. The MM-ESS modules will be switched on/off as needed to fulfil the desired string voltage. The maximum current of the string will be limited by the maximum current of the MM-ESS module with the lowest maximum current.
- It is possible to install more modules in series than needed to fulfil the voltage level requirement, so a better compromise between the required energy and the installed energy can be obtained. Also, different levels of system reliability can be achieved by redundance on the modules/strings.

2.2 Main MM-ESS design rules:

2.2.1 Energy capacity

In general, the installed energy capacity of the MM-ESS (E_{MMESS}) (at beginning of life (BOL)) can be expressed by

$$E_{MMESS} = \sum_{j=1}^{N_{str}} \sum_{i=1}^{N_{mod(j)}} E_{mod(i,j)}$$

where N_{str} is the number of parallel connected strings, $N_{mod(j)}$ is the number of modules installed in the string j, and $E_{mod(i,j)}$ is the installed capacity of the module i in the string j.
A special case can be considered when the MM-ESS is defined by identical modules and strings, so E_{MMESS} can be expressed by

$$E_{MMESS} = N_{str} \cdot N_{mod} \cdot E_{mod}$$

In similar way, the Usable Energy Capacity of the MM-ESS is defined by the usable energy capacity of each module in the system:

$$\mathrm{USR_{MMESS}} = \frac{\sum_{j=1}^{N_{str}} \sum_{i=1}^{N_{mod(j)}} USR_{mod(i,j)} \cdot E_{mod(i,j)}}{E_{MMESS}}$$

where $\mathrm{USR_{MMESS}}$ is the Usable SOC Range in per unit of the MM-ESS, and $USR_{mod(i,j)}$ is the usable SOC range of the module i in the string j. When identical MM-ESS modules are considered, then:

$$\mathrm{USR_{MMESS}} = USR_{mod}$$

2.2.2 Maximum continuous charge/discharge current

The maximum continuous charge/discharge current ($I_{MMESS.MCC}$ / $I_{MMESS.MCD}$) of the MM-ESS can be expressed by

$$I_{MMESS.MCC} \leq \sum_{j=1}^{N_{str}} \left(\min\left(I_{mod.MCC(i,j)}\right) \ \forall\, i = 1, \dots, N_{mod(j)}\right)$$

$$I_{MMESS.MCD} \leq \sum_{j=1}^{N_{str}} \left(\min\left(I_{mod.MCD(i,j)}\right) \ \forall\, i = 1, \dots, N_{mod(j)}\right)$$

where $I_{mod.MCC(i,j)}$ and $I_{mod.MCD(i,j)}$ are the maximum continuous charge and discharge current of the module i in the string j, respectively. When identical modules are considered, then the previous expressions can be simplified as follows:

$$I_{MMESS.MCC} \leq N_{str} \cdot I_{mod.MCC}$$
$$I_{MMESS.MCD} \leq N_{str} \cdot I_{mod.MCD}$$

2.2.3 String Voltage

The voltage of the string j can be expressed by

$$V_{str(j)} = \sum_{i=1}^{N_{mod(j)}} D_{mod(i,j)} \cdot V_{mod(i,j)} \ \forall\, j = 1, \dots, N_{str}$$
$$V_{mod(i,j)} \in \{V_{mod.min(i,j)}, V_{mod.max(i,j)}\}$$

where $V_{mod(i,j)}$ is the voltage of module i in the string j, which varies depending on SOC within the module voltage window defined by the minimum and maximum module voltage $V_{mod.min(i,j)}$ and $V_{mod.max(i,j)}$, respectively, and $D_{mod(i,j)}$ is the duty cycle of the module i in the string j within the effective control string period (T_{str}).

The required string voltage within T_{str}, which is defined by the required MM-ESS voltage and required string power, is built up by keeping $N_{mod(j)} - N_{act(j)}$ modules switched off (by passed), $N_{act(j)}$-1 switched on and the remained module is PWM controlled with switching frequency T_{sw}. A sorting algorithm (based on SOC, temperature and/or SOH) can be used to decided which modules are switched on, by-passed or PWM controlled within the predefined T_{str}. $N_{act(j)}$ refers to the number of active modules (modules supplying/storing energy) within the period T_{str}.

2.2.4 Number of modules

When a maximum MM-ESS voltage ($V_{MMESS.max}$) is required to be provided, then a maximum number of active modules ($N_{act.max(j)}$) needs to be fulfilled at worst case scenario (modules near to its minimum voltage) and therefore a minimum number of modules to be installed ($N_{mod.\min(j)} = N_{act.max(j)}$) can be stablished:

$$V_{MMESS.max} < \sum_{i=1}^{N_{mod.\min(j)}} V_{mod.min(i,j)} \quad \forall\, j = 1, \dots, N_{str}$$

When identical modules are considered, then the previous expression can be simplified as follows:

$$V_{MMESS.max} < N_{mod.min} \cdot V_{mod.min}$$

Figure 2-3 shows an example of the required minimum number of modules as function of minimum module voltage for different maximum MM-ESS voltages, and when identical modules are considered.

Considering $N_{mod.\min(j)}$, the number of installed modules per string $N_{mod(j)}$ can be expressed as function of the number of redundant modules per string $N_{Redumod(j)}$:

$$N_{mod(j)} = N_{mod.\min(j)} + N_{Redumod(j)}$$

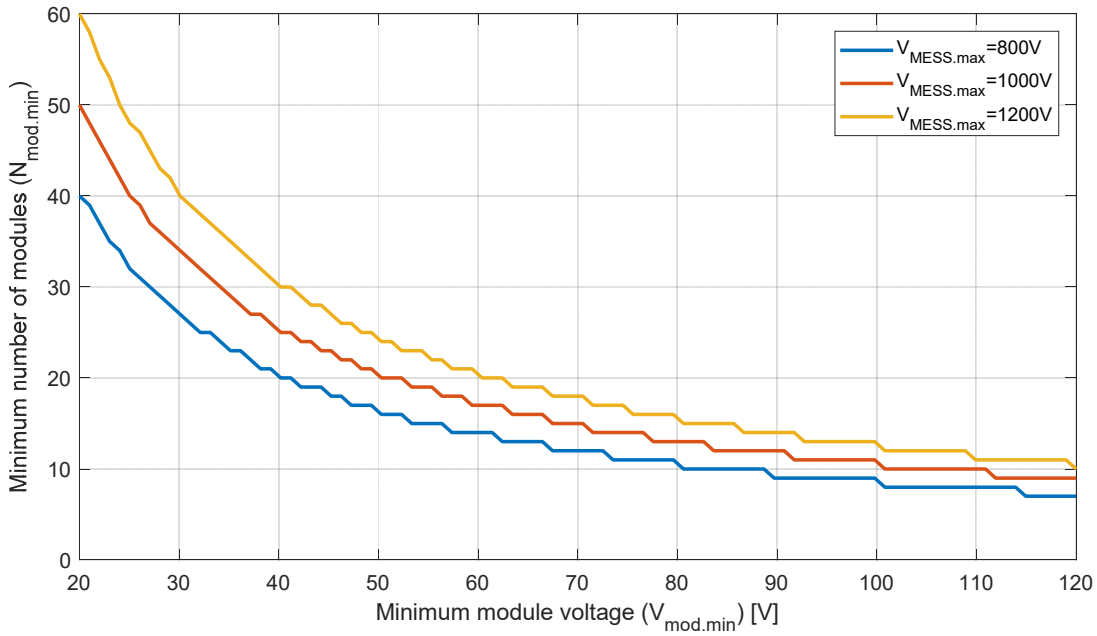


Figure 2-3 Minimum number of modules per string versus minimum module voltage for different required MESS maximum voltages and when identical modules are considered.

2.2.5 Maximum charge/discharge power

The MM-ESS maximum discharge power ($P_{MMESS.MCD}$) is the product of the maximum continuous discharge current and the maximum achievable DC battery voltage:

$$P_{MMESS.MCD} = I_{MMESS.MCD} \cdot \min\left(\sum_{i=1}^{N_{mod(j)}} V_{mod.max(i,j)} \;\forall\, j = 1, \dots, N_{str}\right)$$

The MM-ESS maximum charge power ($P_{MMESS.MCD}$) could be defined in similar way as $P_{MMESS.MCD}$, however as normally $I_{MMESS.MCC}$ is limited when battery is nearly full charged ($V_{mod} = V_{modmax}$) then an alternative definition, based on the average module voltage, is used here:

$$P_{MMESS.MCC} = I_{MMESS.MCC} \cdot \min\left(\sum_{i=1}^{N_{mod(j)}} \frac{V_{mod.min(i,j)} + V_{mod.max(i,j)}}{2} \;\forall\, j = 1, \dots, N_{str}\right)$$

However, when the MM-ESS is connected to a DC grid with nominal DC link voltage (V_{gridDC}), then $P_{MMESS.MCD}$ and $P_{MMESS.MCC}$ are limited by V_{gridDC} and the maximum allowed peak-to-peak voltage ripple (δV_{gridPP}):

$$P_{MMESS.MCD} = I_{MMESS.MCD} \cdot \left(V_{gridDC} + \frac{\delta V_{gridPP}}{2}\right)$$
$$P_{MMESS.MCC} = I_{MMESS.MCC} \cdot \left(V_{gridDC} + \frac{\delta V_{gridPP}}{2}\right)$$

When identical modules are considered, then the previous expressions can be simplified as follows:

$$P_{MMESS.MCD} = N_{str} \cdot I_{mod.MCD} \cdot \left(V_{gridDC} + \frac{\delta V_{gridPP}}{2}\right)$$
$$P_{MMESS.MCC} = N_{str} \cdot I_{mod.MCC} \cdot \left(V_{gridDC} + \frac{\delta V_{gridPP}}{2}\right)$$

2.2.6 String Inductors

The main function of the string inductor is to limit the current ripple in the string. Under normal MM-ESS operation, only one module per string is PWM operated within the effective control string period (T_{str}), and therefore the string current ripple is related to the PWM operation of one module. For the considered DC/DC power converter topology (within each MM-ESS module), the string inductance (L_{str}) and the peak-to-peak current ripple (ΔI_{str}) are related as follows:

$$L_{str} \cdot \frac{\Delta I_{str}}{D_{mod} \cdot T_{sw}} = (1 - D_{mod}) \cdot V_{mod}$$

where, D_{mod} is the duty ratio of the k-th module, which is the module been PWM operated within the string, with the effective switching period T_{sw} ($T_{sw} \leq T_{str}$), and module voltage V_{mod}.

The string inductor can be sized to limit ΔI_{str} to the maximum allowed value and for the worst operating conditions, it is $D_{mod(k)} = 0.5$ and V_{mod} equals to the maximum module voltage within the string, therefore:

$$L_{str} \geq \frac{T_{sw} \cdot V_{mod.mxSTR}}{4 \cdot \delta i_{LstrPP} \cdot I_{strN}}$$

$$V_{mod.mxSTR} = \max \{V_{mod.\max(i)} \; \forall \; i = 1, \dots, N_{mod}\}$$

Where the maximum allowed peak-to-peak string current ripple ($\Delta I_{str.max}$) is expressed in terms of the nominal string current I_{strN} and δi_{LstrPP}, which is the maximum allowed ratio of peak-to-peak current ripple to the nominal DC current ($\Delta I_{str.max} = \delta i_{LstrPP} \cdot I_{strN}$). For this topology, the nominal string current is linked to the lowest maximum continuous current between all the modules in the string, therefore:

$$I_{strN} = \max (I_{str.MCC}, I_{str.MCD})$$
$$I_{str.MCC} = \min\left(I_{mod.MCC(i)} \; \forall \; i = 1, \dots, N_{mod}\right)$$
$$I_{str.MCD} = \min\left(I_{mod.MCD(i)} \; \forall \; i = 1, \dots, N_{mod}\right)$$

When the current waveform is close to triangular waveform, as normally in the considered DC/DC converter topology, then the peak-to-peak ripple and the rms ripple are related by:

$$\delta i_{LstrPP} = 2 \cdot \sqrt{3} \cdot \delta i_{LstrRMS}$$

Normally, $\Delta I_{str.max}$ is directly linked to the system requirements and/or regulations regarding the maximum allowed current harmonic injections. However, the maximum peak current is also limited by the module peak current, so an additional constraint can be considered for δi_{LstrPP} as follows:

$$\delta i_{LstrPP} \leq 2 \cdot \left(\frac{\min (I_{str.PeakC}, I_{str.PeakD})}{I_{strN}} - 1\right)$$

$$I_{str.PeakC} = \min\left(I_{mod.PeakC(i)} \; \forall \; i = 1, \dots, N_{mod}\right)$$
$$I_{str.PeakD} = \min\left(I_{mod.PeakD(i)} \; \forall \; i = 1, \dots, N_{mod}\right)$$

Some degrees of freedom in the selection of $\Delta I_{str.max}$ can be added by considering interleave PWM modulation along the strings to reduce the total system current ripple (by counteract the ripple of different strings) and by adjusting/increasing the switching frequency at low power levels. However, here, it is assumed that either δi_{Lstr} or $\Delta I_{str.max}$ are given design constants. Figure 2-4 shows an example of the required string inductance value as function of $V_{mod.mxSTR}$ and $\Delta I_{str.max}$ when a switching frequency of 3kHz ($T_{sw} = 0.33ms$) is considered.

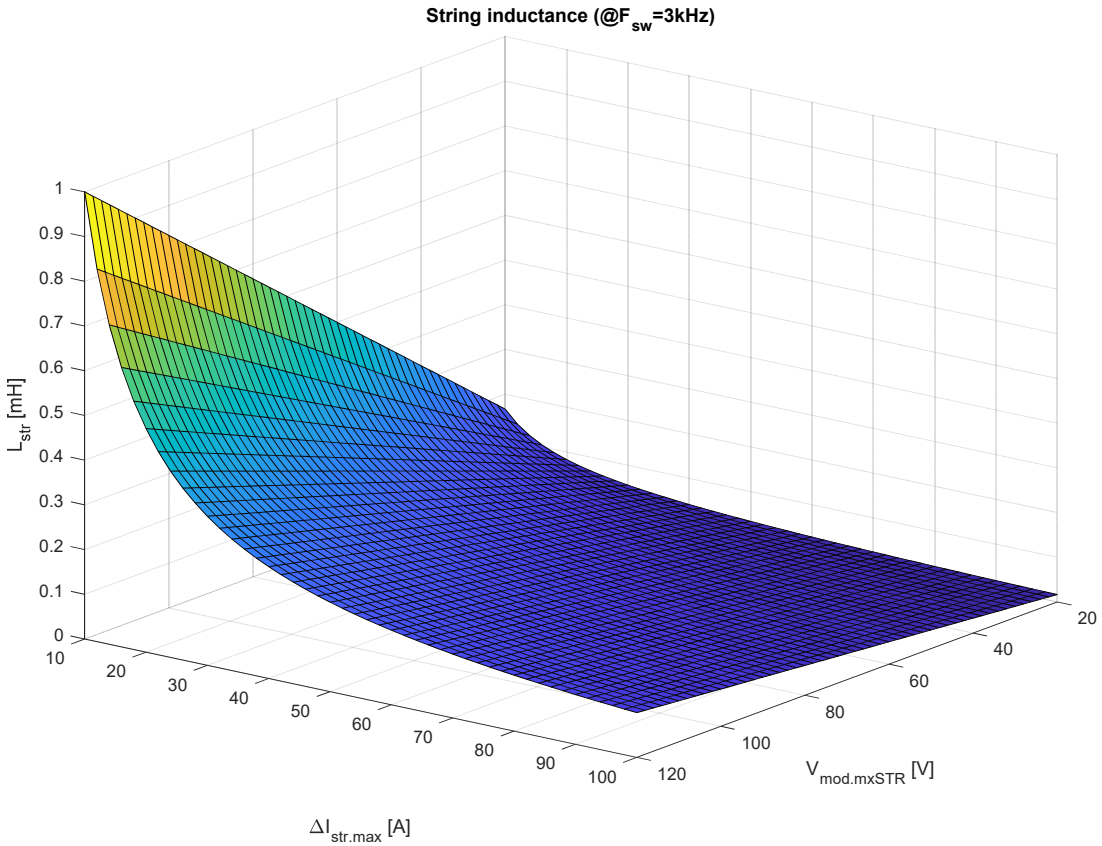


Figure 2-4 String inductance versus module max. voltage and max. peak-to-peak string current ripple

3 MM-ESS design algorithm

Figure 3-1 shows the proposed MM-ESS design algorithm. The algorithm assumes that the MM-ESS will be composed by identical modules (modules composed by the same type and number of battery cells) and the parallel connection of identical strings (strings with the same number of series connected modules).
It should be noted that the design algorithm shown in Figure 3-1 is a global representation at system level, and the design algorithm compress three sub-design algorithms: Battery cells heatsink design, the DC/DC converter design, and the string inductor design, which will be described in the next sub-sections.

3.1 Main design inputs

The main inputs for the MM-ESS design are as follows:

3.1.1 Maximum operating Voltage ($V_{MMESS.max}$)

It is the maximum MM-ESS output voltage that is required to be regulated by the MM-ESS. When the MM-ESS is planned to be connected to a strong DC grid, or a DC grid regulated by other devices, then this voltage is the nominal DC voltage of the DC grid (V_{GridDC}) plus the maximum peak voltage ripple of the grid:

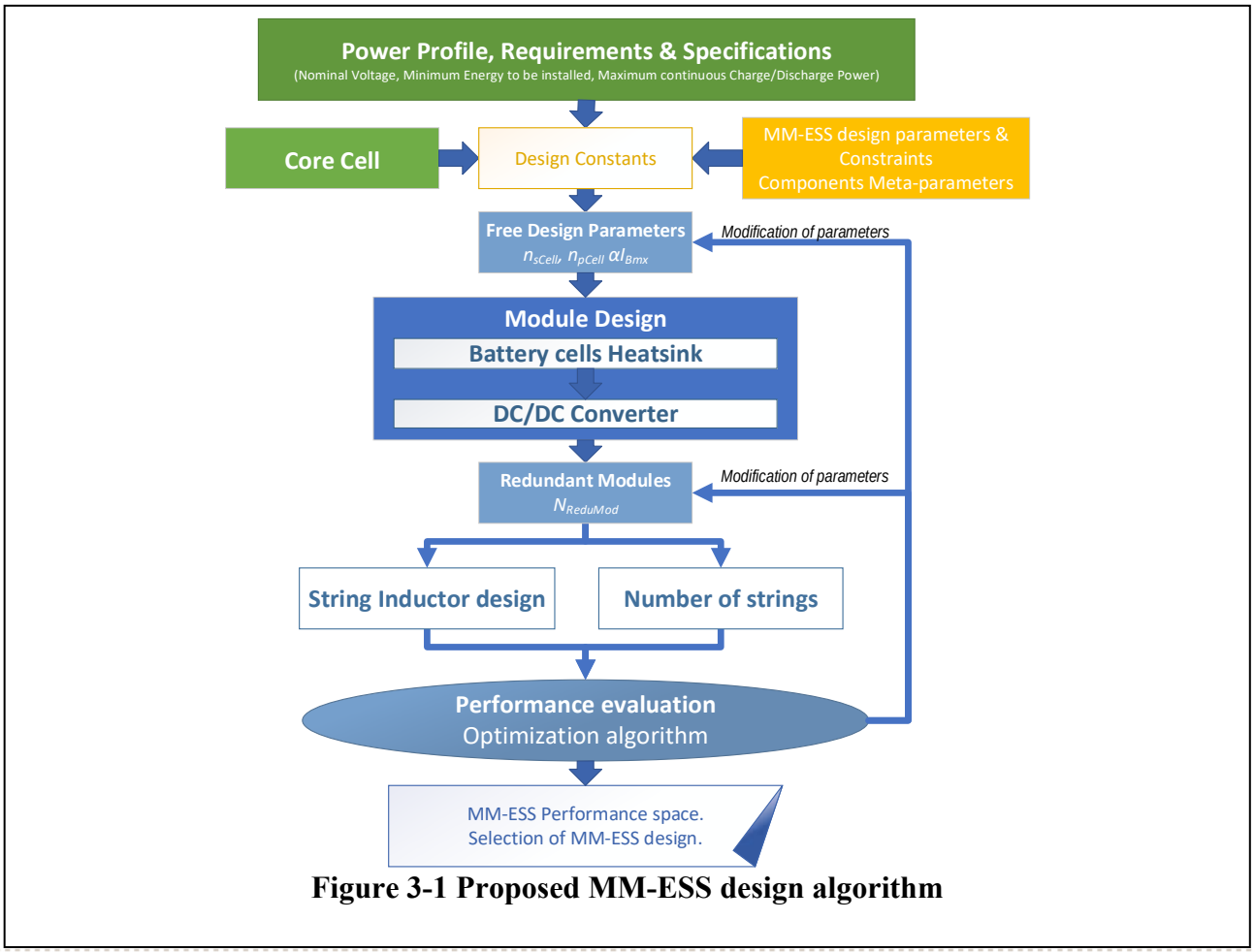


Figure 3-1 Proposed MM-ESS design algorithm

$$V_{MMESS.max} = \left(V_{gridDC} + \frac{\delta V_{gridPP}}{2}\right)$$

For a given module, this input directly set a constrain in the minimum number of modules per string (as defined in section 2.2.4):

$$N_{mod.min} \geq \frac{V_{MMESS.max}}{V_{mod.min}}$$

3.1.2 Minimum operating Voltage ($V_{MMESS.min}$)

It is the minimum voltage that is required to be regulated by the MM-ESS or the minimum voltage that the MM-ESS is operated when maximum continuous power is supplied. When the MM-ESS is planned to be connected to a regulated DC grid, then $V_{MMESS.min}$ can be expressed by

$$V_{MMESS.min} = \left(V_{gridDC} - \frac{\delta V_{gridPP}}{2}\right)$$

3.1.3 Minimum Energy to be installed (E_{ins})

It is the required total battery energy capacity to be installed at the beginning of the battery cell life. For a given module, this input sets a constraint in the minimum number of strings and modules per strings (as defined in section 2.2.1):

$$N_{str} \cdot N_{mod} \geq \frac{E_{ins}}{E_{mod}}$$

3.1.4 Maximum required continuous charge/discharge power (P_{MCC}/P_{MCD})

These are the maximum power that the MM-ESS is required to receive/deliver in a continuous regimen (normally more than 60s). These power values have been considered over the peak power values (power that can be handle by the MM-ESS for less than 1s-30s) because normally impose a stronger requirement, however same expressions/constraints can be used to consider peak power values as inputs. These inputs directly set a constraint in $I_{MMESS.MCC}$ and $I_{MMESS.MCD}$, and when considering the minimum voltage that should handle the MM-ESS during normal operation ($V_{MMESS.min}$), then a constraint in the number of strings for a given module can be defined:

$$N_{str} \geq \frac{1}{V_{MMESS.min}} \cdot \max\left(\frac{P_{MCC}}{I_{mod.MCC}}; \frac{P_{MCD}}{I_{mod.MCD}}\right)$$

3.1.5 Core battery cell

This input refers to the set of relevant properties that defines a considered battery cell.
The considered battery cell technologies are NMC, LFP and LTO (Anode), as they are the most common used in marine applications. Within these technologies, there are many kinds of cells according to the stoichiometric ratio of the chemistry components. The multi-domain design approach considered within this work requires electrical, thermal, and mechanical cell properties. For that reason, instead of modelling a general battery cell technology, the design methodology is

adapted to a specific battery cell, so the type of battery cell is considered as input for the design algorithm.

The battery cell properties relevant for the design algorithm are:

- Physical properties
  - Shape: Prismatic or pouch cells can be used within the models and assumption of the algorithm. To consider cylindrical cells some changes need to be done in the battery module heatsink design algorithm.
  - Cell length (L_{cell})
  - Cell thickness (t_{cell})
  - Cell width (W_{cell})
  - Cell weight ($Weight_{cell}$)
  - Cell cost ($Cost_{cell}$)
- Electrical Properties
  - Average cell voltage
  - Minimum cell voltage
  - Maximum cell voltage
  - Nominal cell energy capacity at BOL
  - Nominal cell AH capacity at BOL
  - Maximum continuous charge current ($I_{Cell.MCC}$)
  - Maximum continuous discharge current ($I_{Cell.MCD}$)
  - Charge/discharge cell resistance at 50% SOC and BOL
  - Maximum increment of cell resistance at EOL
  - Usable/recommended SOC range (USR_{cell}), maximum and minimum cell SOC.
  - (optional) Maximum peak charge current ($I_{Cell.peakC}$)
  - (optional) Maximum peak discharge current ($I_{Cell.peakD}$)
  - (optional) OCV versus SOC characteristic
  - (optional) Cell resistance versus SOC characteristic
- Thermal Properties
  - Maximum cell temperature during discharge
  - Maximum cell temperature during charge
  - Through-plane thermal conductivity
  - In-plane thermal conductivity
- Aging figures (optional, not used within this algorithm but indirectly needed to estimate E_{ins} from the required usable energy at EOL)
  - Minimum percent capacity loss per year because only calendar aging, no cycling.
  - Cycle life characterization
    - Number of cycles
    - Depth of discharge
    - EOL capacity (after the given number of cycles)
    - Charge/discharge rate
    - Cell temperature

3.2 Design parameters and constants

The global MM-ESS design parameters, constants, and specified constraints, which are set up front and are not optimized within the design algorithm, are listed as following:

Module – battery array design

- Target maximum cell operating temperature ($T_{cell.max}$)
- Heatsink water/liquid maximum inlet temperature for cold plate (T_{watmx})
- Maximum cell weight per module ($Weight_{C4M.max}$) - this limits the maximum number of cells per module that will be considered in the design algorithm.
- Minimum average module voltage to be considered in the design ($V_{ModMN4D}$) – this defines the minimum number of series connected cells per module to be considered in the design algorithm.
- Maximum average module voltage to be considered in the design ($V_{ModMX4D}$) - this defines the maximum number of series connected cells per module to be considered in the design algorithm
- Minimum considered value for the maximum battery cell utilization ratio within the design algorithm ($\alpha I_{Bmx.MN}$) (utilization of the current capacity of the cell)
- Number of possible αI_{Bmx} considered within the design ($N_{\alpha IBmx}$). (It limits the number of design candidates)

Module - DC/DC converter design

- DC/DC converter switching frequency (F_{sw})
- Maximum expected stray inductance between battery cell array and DC/DC converter capacitor bank (L_{dBC})
- Maximum accepted parallel connected power semiconductor devices (n_{PMOSmx}) per module
- Power MOSFET equivalent chip area ($A_{ChipMOS}$)
- Power semiconductor blocking voltage utilization factor ($k_{Vblock} < 1$)
- Ratio of the maximum desired semiconductor operating junction temperature to the absolute maximum allowed semiconductor junction temperature ($k_{Tjmx} < 1$)
- Gate driver voltage supply (V_{Dr})
- Maximum average inlet air temperature for air forced heatsink (T_{airmx})
- Maximum ambient temperature inside the power module when no heatsink is considered (T_{ambmx})
- Safety margin for absolute maximum MOSFET current given by the minimum between package limit and silicon limit ($KSF_{IMOSmx} < 1$).
- Safety margin for minimum ON gate resistance ($KSF_{RgON} < 1$)
- Maximum allowed rate of change of diode current during turn-off process $\left(\frac{di_F}{dt}\right)_{Max}$
- Space factor including space between discrete capacitors ($KS_{Cdc} > 1$)
- Maximum allowed relative peak capacitor overvoltage (δV_{Cdc})
- Other Power Switch Device (PSD) component cost ($Cost_{PSD0}$) - This includes the external gate resistances, RC snubbers and Ferrite bead.
- Other DC/DC converter component cost ($Cost_{OCCPC}$) – this also includes control electronics cost.
- Other common component area including IC, control electronics and sensors, among others (A_{PCB0})
- Number of layers for power PCB ($N_{layerPCBP}$)

- Power PCB cooper thickness (d_{cuPCBP})
- Number of layers for control PCB ($N_{layerPCBC}$)
- Control PCB cooper thickness (d_{cuPCBC})
- PCB density (ρ_{PCB})
- PCB thickness (t_{PCB})
- Average weight of individual components in the power converter ($Weight_{comp}$)
- Number of components per Power MOSFET in the PSD ($N_{CompPSD}$)
- Number of other common components ($N_{CompOCC}$)
- Converter housing density ($\rho_{ConvHousing}$)
- Labour cost per component ($C4C_{ConvLab}$)
- Converter housing reference cost ($Cost_{HousingREF}$)
- Converter housing reference volume ($Vol_{HousingREF}$)
- Converter housing reference weight ($Weight_{HousingREF}$)
- Converter housing reference thickness ($t_{HousingREF}$)
- Power Converter Module supplier gross margin (Ξ_{PCM})
- Delta space for overall converter volume evaluation (Δx_{conv})

String design

- Ratio of maximum allowed internal system voltage to maximum output voltage ($K_{Viso} > 1$) – this limits the total number of series connected modules per string (N_{mod})
- Maximum allowed RMS string current ripple ($\delta i_{LstrRMS}$)
- Utilization ratio of volume inside the string cabinet ($k_{Ucab} \leq 1$)

Other general cost related parameters

- Service connector cost at module level ($Cost_{SCMod}$)
- Service connector cost at string level ($Cost_{SCStr}$)
- Manual service switch cost ($Cost_{MSSW}$)
- High Voltage sensor cost ($Cost_{HVSensor}$)
- Cell Temperature sensor cost ($Cost_{TSensor}$)
- String Current sensor cost ($Cost_{CSensor}$)
- Insulation measurement device cost ($Cost_{IMD}$)
- High voltage connection with interlock cost ($Cost_{HVCI}$)
- Cost of a high voltage contactor with feedback ($Cost_{HVCF}$)
- Pre-charge resistor cost ($Cost_{PCR}$)
- Cost per watt of main fuse ($C4W_{MainF}$)
- Cost per watt of module fuse ($C4W_{ModF}$)
- Power supply connector cost ($Cost_{PSC}$)
- Cost of module BMS per battery cell ($C4C_{BMS}$)
- Emergency-off switch cost ($Cost_{EOS}$)
- Master controller cost ($Cost_{MstCtr}$)
- String controller cost ($Cost_{StrCtr}$)
- Coolant ports cost ($Cost_{CoolP}$)
- Coolant channel cost ($Cost_{CoolCH}$)

3.3 Free design parameters

For a given core cell, the module design is defined by three free design parameters: the number of series (n_{sCell}) and parallel (n_{pCell}) connected cells per module and the maximum battery cell utilization ratio αI_{Bmx}, defined by

$$\alpha I_{Bmx} = \frac{I_{mod.MCC}}{n_{pCell} \cdot I_{Cell.MCC}} = \frac{I_{mod.MCD}}{n_{pCell} \cdot I_{Cell.MCD}}$$

where $I_{Cell.MCC}/I_{Cell.MCD}$ are the maximum continuous charge/discharge currents that the cell can handle and $I_{mod.MCC}/I_{mod.MCD}$ are the maximum continuous charge/discharge currents per module, so αI_{Bmx} is always lower or equal to 1, but it allows to design/size all other components of the module according to the string current with more freedom.

The maximum and minimum values for n_{sCell} are set by the maximum and minimum average module voltage ($V_{ModMX4D}$ and $V_{ModMN4D}$) to be considered in the design, respectively:

$$\frac{V_{ModMN4D}}{V_{cell}} \leq n_{sCell} \leq \frac{V_{ModMX4D}}{V_{cell}}$$

On the other hand, n_{pCell} is sweep between 1 and $n_{pCell.Max}$, with $n_{pCell.Max}$ defined as follows:

$$n_{pCell.Max} = floor\left\{\frac{Weight_{C4M.max}}{n_{sCell} \cdot Weight_{cell}}\right\}$$

$$1 \leq n_{pCell} \leq n_{pCell.Max}$$

where $Weight_{C4M.max}$ is the maximum cell weight per module, which is considered as a design parameter to limit the total module weight.

For each (n_{sCell}, n_{pCell}) combination, a predefined number of module design possibilities ($N_{\alpha IBmx}$) are evaluated by sweeping the free parameter αI_{Bmx} between $\alpha I_{Bmx.MN}$ and 1, with $\alpha I_{Bmx.MN}$ as the design parameter to specified the minimum considered value for αI_{Bmx} within the design algorithm. Therefore:

$$\alpha I_{Bmx.MN} \leq \alpha I_{Bmx} \leq 1$$

With the first three free design variables defined, then the battery array is established, and the battery cell heatsink is designed according to section 3.4 and the DC-DC power converter is also designed following the algorithm described in section 3.5.

Once the module is defined, then the number of modules per string (N_{mod}) can be calculated. For this topology, as previously mentioned, there is a minimum number of modules per string ($N_{mod.min}$) to be fulfilled which is directed constrained by the specified nominal voltage. However, there is one more degree of freedom in the string design as it is possible to have redundant modules per string (redundant regarding voltage), so the number of redundant modules per string (N_{RedMod}) has been considered as additional free design parameter, then N_{Mod} is calculated by

$$N_{mod} = N_{mod.min} + N_{RedMod}$$

$$0 \leq N_{RedMod} \leq N_{RedMod.Max}$$

The maximum number of redundant modules per string ($N_{RedMod.Max}$) is limited by:

$$N_{RedMod.Max} < floor\left(\frac{K_{Viso} \cdot V_{MMESS.max}}{n_{sCell} \cdot V_{cell.max}}\right) - N_{mod.min}$$

where, K_{Viso} is the ratio of maximum allowed internal system voltage to maximum output voltage.

Once the number of modules per string is defined, then the string inductor can be design/evaluated, following the methodology described in section 3.6. Also, the number of strings can be calculated to fulfil the required energy and power capacity, as follows:

$$N_{str} = \max\left\{\frac{E_{ins}}{E_{mod} \cdot N_{mod}}; \frac{1}{V_{MMESS.min}} \cdot \max\left(\frac{P_{MCC}}{I_{mod.MCC}}; \frac{P_{MCD}}{I_{mod.MCD}}\right)\right\}$$

3.4 Battery modules heatsink design algorithm

Battery cell thermal management is based on water cooling. Two methods based on water cooling heatsink could be considered: Fin cooling and microchannel cold plates. The considered concept of battery module with cooling system based on thermal conductive fins and cold plates is illustrated in Figure 3-2. On the other hand, Figure 3-3 shows the considered battery module with microchannel cold plates between each battery cell. These two concepts are applicable for battery cells in prismatic and pouch formats/shapes.

The battery module heatsink design sub-algorithm within this MM-ESS design algorithm considers the cooling system based on thermal conductive fins and cold plates, shown in Figure 3-2. The model, design methodology and implementation of the battery module water-cooled heatsink developed within this work is described in [4]. Here, a summary of the algorithm is introduced for

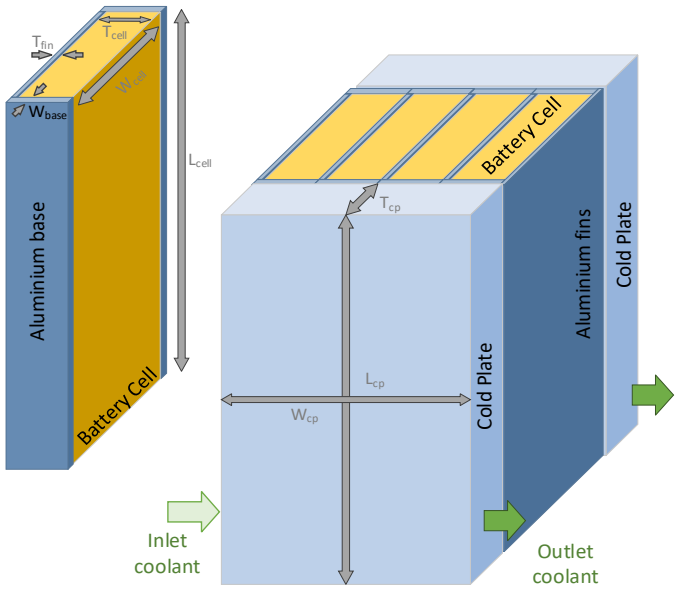


Figure 3-2 Battery module with cooling system based on thermal conductive fins and cold plates.

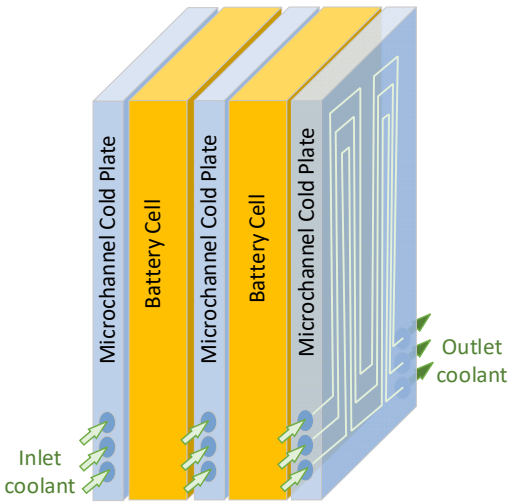


Figure 3-3 Battery module with microchannel cold plates between the battery cells.

the sake of completeness. On the other hand, a model for microchannel cold plates is introduced in appendix B.

The developed battery module heat sink design algorithm is shown in Figure 3-4.

The main inputs for this design algorithm are the dimensions of the core cell (L_{cell}, W_{cell}, t_{cell}), the equivalent/average in-plane and trough-plane cell thermal conductivities from the centre of the cell (κ_{Cellx} and κ_{Celly}), the total number of cell per module ($n_{sCell} \cdot n_{pCell}$), and the required thermal resistance per cell ($R_{thHSMax}$), which is estimated by:

$$R_{thHSMax} = \frac{T_{cellOp} - T_{watmx}}{Q_{cellMX}}$$

where, T_{cellOp} is the maximum operating cell temperature (always minor or equal to the maximum allowed cell temperature (T_{cellMX}) under worst operating conditions), T_{watmx} is the maximum inlet/outlet water temperature and Q_{cellMX} is the maximum average cell heat for worst operating conditions. The average cell heat is assumed to be driven by the cell power loss, so Q_{cellMX} will be given at EOL nominal operation:

$$Q_{cellMX} = kR_{EOL} \cdot (\alpha I_{Bmx})^2 \cdot \max\{R_{cellMX.C} \cdot I^2_{Cell.MCC};\ R_{cellMX.D} \cdot I^2_{Cell.MCD}\}$$

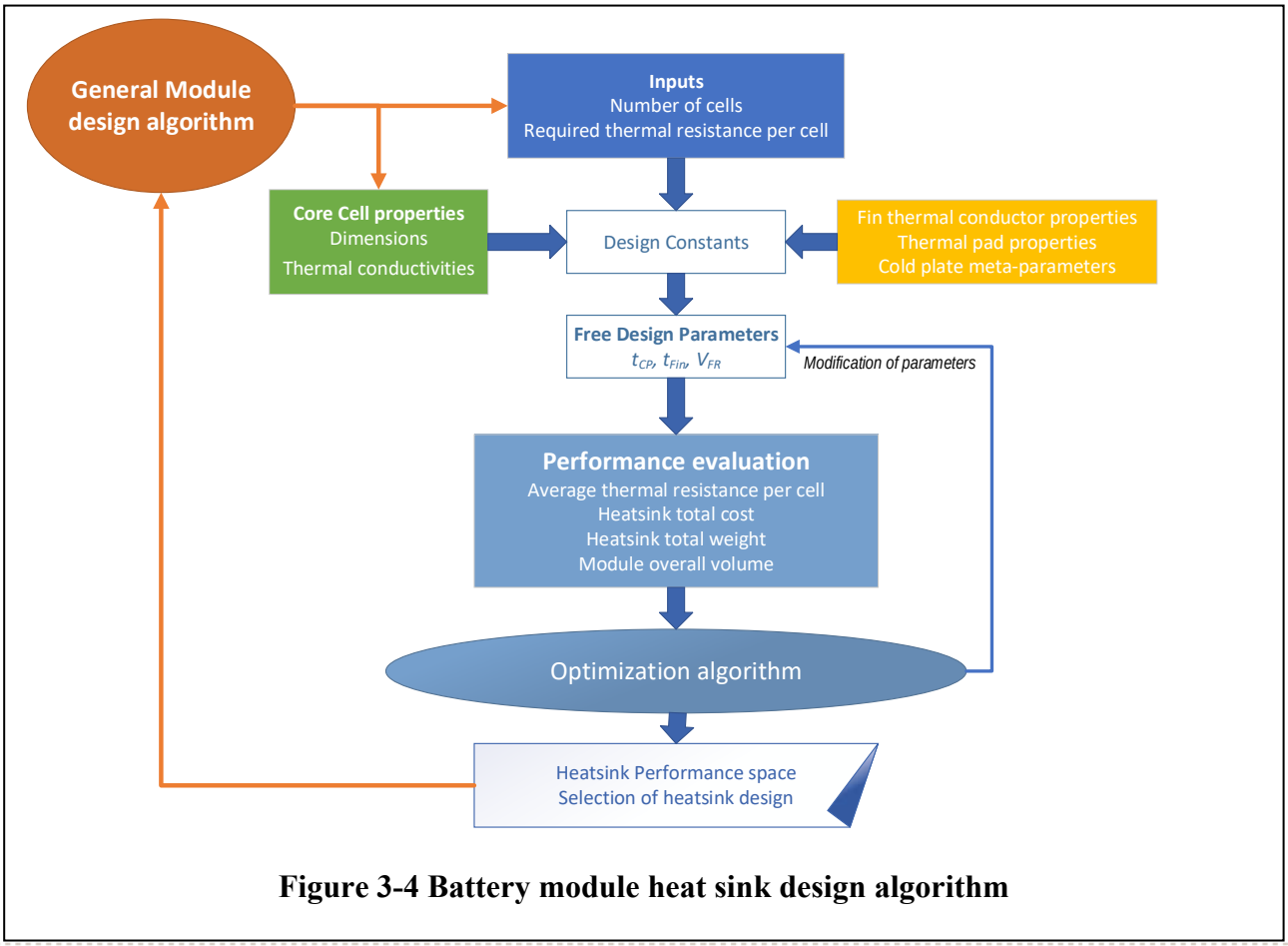


Figure 3-4 Battery module heat sink design algorithm

where $R_{cellMX.C}$ and $R_{cellMX.D}$ are the maximum charge and discharge cell resistance at BOL, respectively, and kR_{EOL} is the expected increment ratio of cell resistance at EOL criteria respect to BOL (typically 1.3~2).

The free design parameters considered for this heatsink configuration to achieve the desired/required thermal resistance are the fin thickness (t_{Fin}), the cold plate thickness (t_{CP}), the inlet water flow rate (V_{FR}) and the fin material. Two fin material are considered: aluminium and copper. The fin thickness is swept considering a minimum fin thickness of 0.5 mm and a maximum fin thickness equal to half the cell thickness. On the other hand, t_{CP}, and V_{FR} are swept within a constrained range, which depends on the considered cold plate technology. The cold plates are modelled and evaluated following the meta-models and meta-parameters introduced in appendix A.4.

The mapped heat sink performance space is composed by the average thermal resistance per cell, the heatsink cost, heatsink mass and the battery module overall volume (heatsink including the battery cells). The output from this sub-algorithm is the solution with lowest cost with average thermal resistance lower or equal to $R_{thHSMax}$.

3.5 DC-DC converter design algorithm

3.5.1 Topology and Main components

The DC/DC power converter module is based on a half bridge topology which is shown in Figure 3-5. The main components considered within the DC/DC converter design are:

- Power Switch Devices (PSD): Half bridge topology has two paired power switch devices, which allows to connect the battery module to the string to charge/discharge power or by-pass the string current with the battery energy storage module disconnected. Figure 3-6 illustrates the considered PSD architecture. A PSD is defined as n_{pMOS} semiconductor devices parallel connected with the Power MOSFET as core technology based on the target range voltage of the modules (Module voltage lower than 150 V). Parallel connection of Power MOSFET is considered to fulfil current/thermal requirements of the PSD. It is also considered that each Power MOSFET will include the external gate resistances R_{gON} and R_{gOFF}, the input/output RC snubbers and the Ferrite bead as common components.
- Heatsink: the main propose of the heatsink is dissipate the MOSFET losses so the temperature

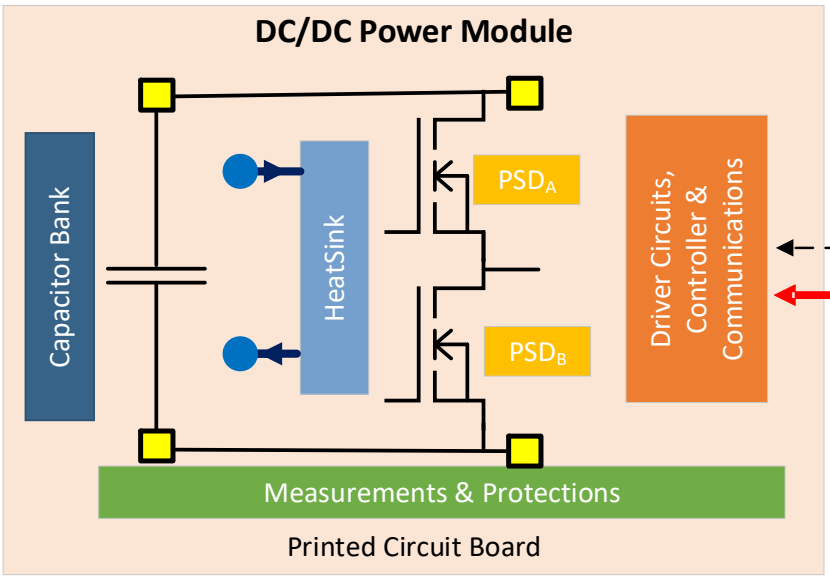


Figure 3-5 DC/DC Power Module: Half-bridge topology and Main components

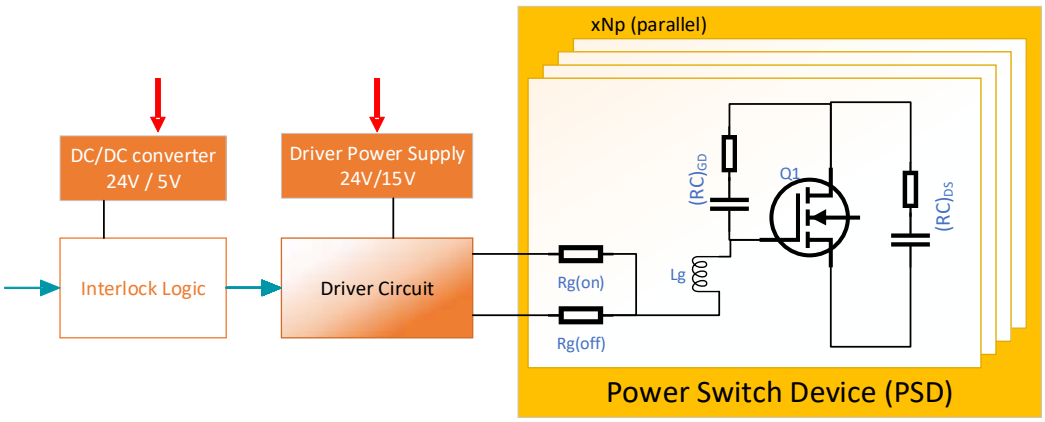


Figure 3-6 Power Switch Device (PSD) definition

of the power MOSFET keeps bellow its maximum designed value. Depending on the current/voltage rating of the converter and the free design parameters, the losses per MOSFET can end up in different heatsink thermal resistance requirements, so four cases have been considered: 1) no heatsink needed; 2) a heatsink based on natural convection; 3) an air-forced heatsink (heatsink structure + fan); and 4) a water cold plate. The heatsink type is selected to get a cost-effective solution (heatsink type that allows fulfil thermal requirements at the lowest cost).

- Capacitor Bank: The main purpose of the capacitor bank is to limit overvoltage associated with stray inductance between Battery array Module (BM) and capacitor bank loop at PSD commutation. Film capacitors are considered for this propose. The capacitor bank in this application is mainly considered for snubber function but not DC-link energy buffer.
- Driver Circuit, controller, and communications: This stage interface the control signals coming from the string controller and generate the PWM signals to control the power MOSFETs. The microcontroller/FPGA that is needed for control and communication with the BMS and string controller, depending on required complexity (bandwidth), can add significant cost per sub-module. Significant savings can be expected if the DC/DC control and BMS functions are merged on the same physical controller.
- Measurements and protections: Common circuit components along the PCB area to ensure proper converter operation.
- Power Circuit Board and Housing.

3.5.2 Reference Power Cell Board layout

The converter design evaluation and main components sizing is done based on the power cell board layout presented in Figure 3-7, which is based on a developed in-house power cell board for a modular multi-level converter [5]. For illustration proposes, the board layout presented in Figure 3-7 considers five parallel connected MOSFET per PSD (named Q_{Ai} for PSD_A and Q_{Bi} for PSD_B), and a capacitor bank with eight discrete capacitors. A top mounted heatsink is installed when it is needed. Two driver circuit, one for each PSD, are illustrated. Measurements and protections are illustrated as a block, but these components are normally spread around the PCB area.

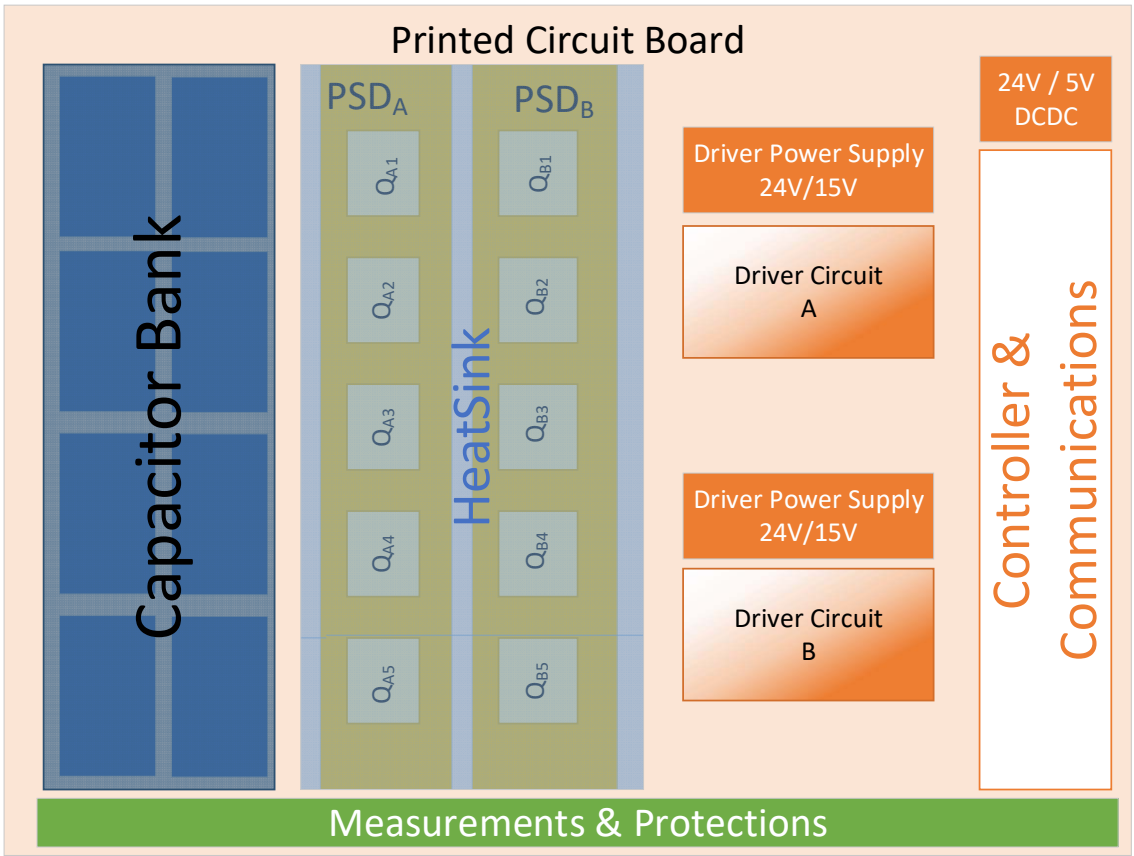


Figure 3-7 DC/DC Power Module – Reference Power Cell Board layout

3.5.3 Main design guidelines

3.5.3.1 Capacitor Bank

The required total DC capacitance (C_{DC}) is sized to limit overvoltage associated with stray inductance between Battery sub-Module (BM) and capacitor bank loop at PSD commutation:

$$C_{DC} \geq \frac{L_{\delta BC} \cdot I_{mod.max}^2}{(\delta V_{dc} \cdot V_{mod.max})^2}$$

$L_{\delta BC}$: the battery–capacitor stray inductance (typically 100-600 nH when BM placed close to converter (main from DC busbar), when BM far from converter then cable inductance needs to be added)
δV_{dc}: the maximum allowed relative capacitor overvoltage $\left(\delta V_{dc} = \frac{V_{peak} - V_{mod.max}}{V_{mod.max}}\right)$.
$V_{mod.max}$: Maximum battery module voltage. ($V_{mod.max} = n_{sCell} \cdot V_{cell.max}$)

$I_{mod.max}$: maximum battery module current

$$I_{mod.max} = n_{pCell} \cdot \alpha I_{Bmx} \cdot \max\{I_{Cell.MCC}; I_{Cell.MCD}\}$$

The DC capacitance is also ruled by maximum allowed dV/dt for the selected technology, so the capacitor bank can handle the nominal current at each commutation action:

$$\frac{dV_c}{dt}_{MAX} \geq \frac{I_{mod.max}}{C_{DC}}$$

$\frac{dV_c}{dt}_{MAX}$: maximum allowed dV/dt for a discrete capacitor of the selected capacitor technology.

3.5.3.2 PSD and Heatsink design

The PSD design is mainly determined by the number of parallel connected MOSFET (n_{pMOS}) and the core power MOSFET device. Based on the meta-parameterized approach for MOSFET device modelling presented in appendix A.2, the selection of the MOSFET device is mainly determine by the required blocking voltage ($V_{BlockMOS}$) and the available equivalent chip area ($A_{ChipMOS}$). To simplify the design, it has been assumed a constant equivalent chip area of 50mm^2 and instead the total equivalent chip area can be varied by changing n_{PMOS}.
The required blocking voltage can be estimated by

$$V_{BlockMOS} = \frac{V_{mod.max}}{k_{Vblock}}$$

k_{Vblock}:Blocking voltage utilization factor.

The number of parallel connected MOSFET is ruled by the desired maximum operating current, in this case the maximum module current, so the MOSFET never overpass its maximum ratings (current and junction temperature)
The MOSFET maximum continuous current (I_{MOSmx}) is limited (besides others) by

$$I_{MOSmx} = k_{SFIMOS} \cdot I_{MOSpackMX} \geq \frac{I_{mod.max}}{n_{pMOS}}$$

where, k_{SFIMOS} is the safety margin for absolute maximum MOSFET current given by the package current limit and $I_{MOSpackMX}$ is the MOSFET package current limit, which can be found in the device datasheet.

The MOSFET maximum current is also limited by the designed maximum operating MOSFET junction temperature, which is linked to the way the MOSFET losses are dissipated and the heatsink design. The required heatsink thermal resistance can be estimated based on the average thermal model for power MOSFETs. Based on the wide design range of converter current/voltage ratings, four heatsink cases have been considered to find the most cost-effective PSD design:

- **Case 1: No heatsink**

To check if a heatsink is required, the required junction to ambient thermal resistance per MOSFET ($R_{thJA.Req}$) is estimated and compared with the minimum junction to ambient thermal resistance per MOSFET ($R_{thJA.Min}$) found in the device datasheet:

$$R_{thJA.Req} = \frac{k_{T_j} \cdot T_{jmx} - T_{ambMX}}{P_{LossMOSi.MX}}$$

k_{T_j}: ratio of the designed maximum operating junction temperature to the absolute maximum allowed MOSFET junction temperature.
T_{jmx}: absolute maximum allowed MOSFET junction temperature
$P_{LossMOSi.MX}$: Total maximum losses (conduction and switching) of one discrete Power MOSFET within the PSD
T_{ambMX}: maximum inner module ambient temperature.

If $R_{thJA.Req} < R_{thJA.Min}$ then a heatsink is required, otherwise the operating MOSFET junction temperature (T_{jMOS}) can be estimated by

$$T_{jMOS} = R_{thJA.Min} \cdot P_{LossMOSi} + T_{ambMX}$$

- **Case 2: Heatsink without forced airflow.**

In this case a heatsink aluminium structure is placed on top of Power MOSFET devices but without air-forced (no fan). The required heatsink to ambient thermal resistance can be estimated by:

$$R_{thNHS.Req} = \frac{k_{T_j} \cdot T_{jmx} - \left(R_{thJC} + R_{thCS}\right) \cdot P_{LossMOSi.MX} - T_{ambMX}}{n_{PMOS} \cdot P_{LossMOSi.MX}} > 0$$

R_{thJC}, R_{thCS}: junction-to-case and case-to-sink MOSFET thermal resistances
$R_{thNHS.Req}$: Required heatsink to ambient thermal resistance.

- **Case 3: Air Forced Heatsink.**

In this case the heatsink is composed by the aluminium structure and a fan. The required heatsink to air thermal resistance can be estimated by

$$R_{thAHS.Req} = \frac{k_{T_j} \cdot T_{jmx} - \left(R_{thJC} + R_{thCS}\right) \cdot P_{LossMOSi.MX} - T_{airMX}}{n_{PMOS} \cdot P_{LossMOSi.MX}} > 0$$

T_{airMX}: maximum air flow temperature.
$R_{thAHS.Req}$: Required heatsink to air thermal resistance.

- **Case 4: Water cold plate.**

When a water cold plate is place on top of MOSFET devices, then the required cold plate thermal resistance can be estimated by

$$R_{thCPHS.Req} = \frac{k_{T_j} \cdot T_{jmx} - \left(R_{thJC} + R_{thCS}\right) \cdot P_{LossMOSi.MX} - T_{wMX}}{n_{PMOS} \cdot P_{LossMOSi.MX}} > 0$$

T_{wMX}: maximum water/coolant fluid temperature.
$R_{thCPHS.Req}$: Required cold plate heatsink thermal resistance.

It is assumed that the battery cells are water cooled, so T_{wMX}, T_{airMX} and T_{ambMX} are corelated with a maximum temperature different between them. Taken as reference T_{wMX}:

$$T_{airMX} = T_{wMX} + \Delta T_{w2airMX}$$
$$T_{ambMX} = T_{wMX} + \Delta T_{w2ambMX}$$

$\Delta T_{w2airMX}$: maximum temperature difference between cold plate inlet/outlet water temperature and forced air (set as 5°C)
$\Delta T_{w2ambMX}$: maximum temperature difference between cold plate inlet/outlet water temperature and ambient temperature inside the module (set as 15°C).

3.5.3.3 Driver Power Supply (DPS)

Driver power supply is sized according to PSD gate & driver power requirements. The required power by the DPS (P_{DPS}) is estimated based on the average gate power per switching cycle as following:

$$P_{DPS} = P_{DPS0} + \frac{n_{pMOS}}{\eta_{Driver}} \cdot \left(2 \cdot P_{QGMOSi} + \left(R_{Gon} + R_{Goff} \right) \cdot \left(\frac{2 \cdot P_{QGMOSi}}{V_{Dr}} \right)^2 \right)$$

P_{QGMOSi}: average gate losses of one discrete Power MOSFET within the PSD
R_{Gon}: turn-on equivalent gate resistance
R_{Goff}: turn-off equivalent gate resistance
η_{Driver}: Gate circuit average efficiency
V_{Dr}: driver voltage
P_{DPS0}: DPS offset power

It should be noted that two DPSs are required for the considered converter layout, one for each PSD. Figure 3-8 shows an evaluation example of P_{DPS} as function of n_{pMOS} for different Power MOSFET devices and for $f_{sw} = 3kHz, V_{Dr} = 15V, \eta_{Driver} = 80\%, R_{Gon} = R_{Goff} = 2.7\Omega$ and $P_{DPS0} = 0.5W$.

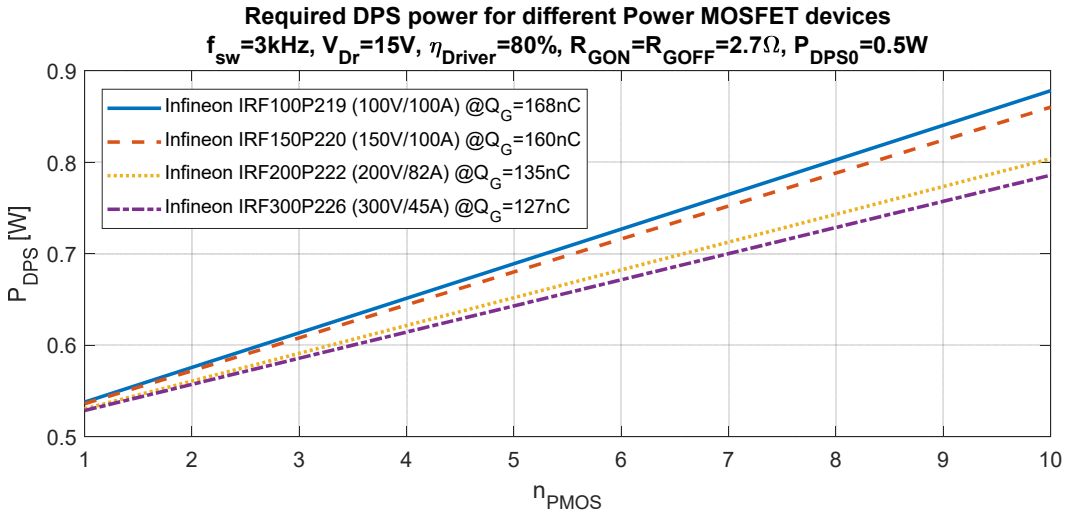


Figure 3-8 Example of required DPS power for different Power MOSFET devices

3.5.3.4 Printed Circuit Board (PCB)

PCB design is beyond the scope of this work, however the PCB area needs to be estimated to evaluate the converter performance, as it influences the size and cost of the converter. For the considered converter layout, the PCB can be divided into two types: the power PCB and the control PCB. The power PCB compress all components that carry out the main power of the converter, like the power MOSFETs and the capacitor bank. On the other hand, the control PCB is composed by all other components that does not carry out the main power of the converter, like the gate circuits, controller, and communications. The main difference between the two PCB types are the used number of layers and the copper thickness, which are higher for the power PCB compared with control PCB. A power PCB with 4 layers / 105µm copper thickness and a control PCB with 2 layers / 35µm copper thickness, have been considered for all converter designs.

The total PCB area is estimated by the summation of the power PCB area ($A_{PCB.Power}$) and the control PCB area ($A_{PCB.control}$):

$$A_{PCB} = A_{PCB.Power} + A_{PCB.control}$$

For the considered converter design and layout, the PCB area can also be divided into three parts: the capacitor bank area (A_{Cdc}), the total PSD area (A_{PSD}) and the area of other common components (A_{OCC}):

$$A_{PCB} = A_{Cdc} + A_{PSD} + A_{OCC}$$

The capacitor bank area occupied in the PCB can be approximated by the total capacitor bank volume (Vol_{Cdc}) and the high of the single discrete capacitors composing the capacitor bank (H_{Cdci}):

$$A_{Cdc} = \frac{Vol_{Cdc}}{H_{Cdci}}$$

The total PSD area (A_{PSD}) is composed by the area of power devices ($A_{PSD.P}$) and the area of control/gate devices ($A_{PSD.C}$), and it can be approximated by

$$A_{PSD} = A_{PSD.P} + A_{PSD.C} = 2 \cdot n_{pMOS} \cdot A_{PSDi}$$
$$A_{PSD.P} = 2 \cdot n_{pMOS} \cdot k_{spMOS} \cdot A_{MOS.Pack}$$

where, A_{PSDi} is the area per power MOSFET including snubber and gate circuit components, which can be considered proportional to the power MOSFET pack area ($A_{MOS.Pack}$) (normally found in the device datasheet):

$$A_{PSDi} = k_{APSDi} \cdot A_{MOS.Pack}$$

k_{APSDi}: ratio of PSD area per MOSFET to the MOSFET pack area (considered as a design constant/parameter, $k_{APSDi} = 3$ considered as default for all designs).
k_{spMOS}: space factor accounting for space between power MOSFET within the PSD.

On the other hand, A_{OCC} can be considered as a constant design value because other common components do not change against module voltage or current ratings.

The power PCB area ($A_{PCB.Power}$) is estimated by:

$$A_{PCB.Power} = A_{Cdc} + A_{PSD.P} + \frac{A_{OCC}}{2}$$

The control PCB area ($A_{PCB.control}$) is estimated by:

$$A_{PCB.control} = A_{PSD.C} + \frac{A_{OCC}}{2}$$

3.5.4 Design algorithm

The implemented algorithm for DC-DC converter design is summarized and shown in Figure 3-9. The design inputs are the maximum module voltage ($V_{mod.max}$), the maximum module current ($I_{mod.max}$) and the switching frequency (F_{sw}). The switching frequency has also been considered as an input because it also affects the design/selection of other components beyond the DC/DC converter (like the string inductor).
The main free design parameters of the DC-DC converter sub-optimization are the number of parallel connected MOSFETs (n_{pMOS}) and the type of heatsink (HS_{type}).
n_{pMOS} is swept within the following range:

$$\frac{I_{mod.max}}{k_{SFIMOS} \cdot I_{MOSpkmx}} \leq n_{pMOS} \leq n_{pMOS.Max}$$

with $n_{pMOS.Max}$ as the maximum allowed number of parallel connected MOSFET, which is set as design constant to limit n_{pMOS} to practical values.
HS_{type} can have four different values (for the four considered cases): 0 for no heatsink, 1 for heatsink without forced airflow, 2 for air-forced heatsink, and 3 for liquid cold plate.

For the selection of the Power MOSFET devices, it has been considered at least a 100 % safety margin on blocking voltage ($k_{Vblock} = 0.5$) and absolute maximum DC current ($k_{SFIMOS} = 0.5$) from the maximum module voltage and module nominal DC current (scale by the number of parallel connected MOSFET), respectively.

The performance evaluation is done to find the DC-DC converter design with minimum cost as main criteria. Details on performance evaluation are introduced in section 4.6.

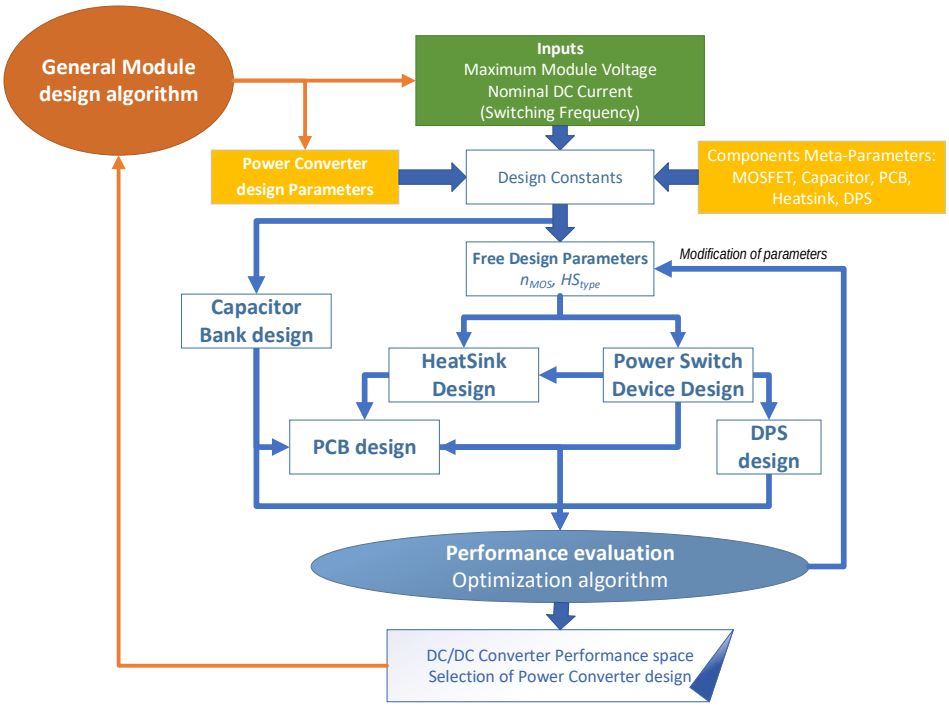


Figure 3-9 DC-DC converter design algorithm

3.6 String inductor design and evaluation

The string inductor should be selected/designed so that it can carry the maximum string current, which is set by the string modules, so the string inductor nominal current ($I_{L.N}$) should be at least equal to the maximum required continuous current of the modules including expected maximum current ripple component:

$$I_{L.N} \geq \sqrt{I_{mod.max}^2 + \left(\frac{f_{sw} \cdot V_{mod.max}}{8 \cdot \sqrt{3} \cdot L_{str}}\right)^2}$$

The inductor insulation voltage level ($V_{L.iso}$) should be at least the maximum string voltage level:

$$V_{L.iso} \geq V_{MMESS.max}$$

The inductor ripple frequency is equal to the module switching frequency:

$$f_{swL} = f_{sw} = \frac{1}{T_{sw}}$$

The string inductors are evaluated following the methodology introduced in [1], but introducing some factors to consider inductors with high current ratings but low inductance as could be the case in some designs for this topology. The inductor models, parameters and meta-parameters are introduced in the section 4.7 and appendix A.3.

3.7 MM-ESS performance space

The MM-ESS performance space is mainly defined by four performance indices:

1. MM-ESS cost: It compresses the main MM-ESS component cost without include any additional cost associated to the installation of the MM-ESS.
2. MM-ESS weight: It has been approximated as the sum of the main MM-ESS component mass.
3. Overall volume: It is estimated accounting only the overall volume of strings cabinets and therefore neglecting any additional volume associated to the location/adequation of MM-ESS in the application site (e.g., special room for battery system).
4. Average nominal losses: it is the average nominal loss of the MM-ESS within the expected operating range.

The definition and evaluation of these performance indices, along with the modelling of the main MM-ESS components, are presented in section 4.

Additionally, it can be also of interest to consider as part of the performance space, the MM-ESS installed and usable energy (E_{MMESS} and $\mathrm{USR_{MMESS}}$) as well as the maximum power capability ($P_{MMESS.MCC}$, $P_{MMESS.MCD}$) of each solution, as they can be slightly higher to the required ones specified by the input of the algorithm.

4 Modelling and Evaluation of key performance indices

4.1 MM-ESS cost

The MM-ESS cost ($Cost_{MMESS}$) has been evaluated considering only the cost of main components and neglecting any additional cost associated to transportation, adequation and installation in the application site. The main components cost is estimated by adding the cost of the strings ($Cost_{String}$) and the cost of common components at system level ($Cost_{CCS}$):

$$Cost_{MMESS} = N_{string} \cdot Cost_{String} + Cost_{CCS}$$

The cost of common components at system level is evaluated considering main common components as described in section 2.1, and it is estimated by:

$$Cost_{CCS} = Cost_{HVSensor} + Cost_{IMD} + 2 \cdot (Cost_{HVCI} + Cost_{HVCF} + Cost_{CoolP} + Cost_{CoolCH}) + Cost_{PCR} + Cost_{MainF} + Cost_{EOS} + Cost_{MstCtr}$$

Where the variables are defined as follows:
$Cost_{HVSensor}$: pack voltage sensor cost
$Cost_{IMD}$: insulation measurement device cost
$Cost_{HVCI}$: cost of a HV battery connection with interlock
$Cost_{HVCF}$: cost of a HV contactor with feedback
$Cost_{PCR}$: HV pre-charge resistor cost
$Cost_{MainF}$: HV main fuse cost
$Cost_{EOS}$: cost of an emergency-off switch
$Cost_{CoolP}$: cost of a main coolant port
$Cost_{CoolCH}$: cost of a main coolant channel
$Cost_{MstCtr}$: Master controller cost

All the previous cost components for $Cost_{CCS}$, except for $Cost_{MainF}$, have been considered as constant design values, and the considered values are reported in Table 1, which have been estimated based on off-the-shelf prices of commercial devices (as 60% of reference price). As for the HV main fuse, it should be sizeed according to the MM-ESS nominal/maximum current/power, and therefore its cost is estimated by:

$$Cost_{HVMF} = C4W_{MainF} \cdot \max\{P_{MMESS.MCD}, P_{MMESS.MCC}\}$$

where $C4W_{MainF}$ is the cost per watt of the main fuse, which has been estimated considering a 200A/1000V main fuse with a reference cost of 81 EUR ($C4W_{MainF} = 0.405\ EUR/kW$).

The total cost of a string is evaluated as follows:

$$Cost_{String} = Cost_{Lstr} + N_{Mod} \cdot Cost_{Mod} + Cost_{Cabinet} + Cost_{OCS}$$

where $Cost_{Lstr}$ is the cost of the string inductor, $Cost_{Mod}$ is the total cost of a module, $Cost_{Cabinet}$ is the cost of the string cabinet, and $Cost_{OCS}$ is the cost of other common components per string, which is evaluated by:

Table 1 Main MM-ESS cost parameters

	Parameter	Estimated Value	Reference component @manufacturer, ref. values
System level	$Cost_{HVSensor}$	87 EUR	WBV342U01-S @ Mianyang Weibo Electronic Co., Ltd: 0-1000V Input Voltage Sensor. (Listing price 145EUR/2022)
	$Cost_{IMD}$	348 EUR	ISOMETER® isoEV425 with AGH420 @ Bender: Ground-fault monitoring device for AC 690 V and DC 1000 V IT systems
	$Cost_{HVCI}$	39 EUR	PL082X-301-10D8 @Industrial-Amphenol: Powerlok 300 2 pole receptacle, with HVIL contacts, X coded.
	$Cost_{HVCF}$	72 EUR	HX24 SPST-NO 1.5kV/400A @GIGAVAC
	$Cost_{PCR}$	60 EUR	Precharge resistor @REC (4s/7s delay @ 11-68V)
	$Cost_{EOS}$	6 EUR	L51K23HUM112 @Emas
	$C4W_{MainF}$	0.405 $\frac{EUR}{kW}$	PV-200ANH1 FUSE 200A 1000V DC @EATON (reference cost: 81 EUR)
	$Cost_{MstCtr}$	360 EUR	NEURO vehicle management unit @TM4
	$Cost_{CoolP}$	108 EUR	CBX – Medium pressure, ball locking @Staubli (male + female)
	$Cost_{CoolCH}$	10 EUR	Silicon hose Ø11mm, length 1000mm @Bonrath
String level	$Cost_{SCStr}$	22.8 EUR	HVPT2A70/ HVSL630022A106 @AMPHENOL (male+female) for 70mm² cable
	$Cost_{MSSW}$	90 EUR	HBD21 @GIGAVAC: Manual Disconnect Switch
	$Cost_{CSensor}$	138 EUR	AHR 500 B10@LEM (500A, 0-5V)
	$Cost_{StrCtr}$	50 EUR	Assumed value
	$Cost_{Cab0}$	1275 EUR/m^3	Fitted values for the family of sheet-steel IP55 industrial cabinets from Schneider Electric manufacturer.
	$k_{CostCab0}$	543.48	
	$k_{CostCab1}$	-0.934	
Module level	$Cost_{SCMod}$	11.6 EUR	Cell socket: m/f 43020-1400/AT04-12PA-PM05 @Industrial-Amphenol, Signal socket m/f 93445-6212/AT04-6P-PM11 @Industrial-Amphenol:
	$C4W_{ModF}$	3.3 $\frac{EUR}{kW}$	L15S100.T@ Littelfuse, 100A 100V fuse (reference cost 33 EUR)
	$Cost_{PSC}$	9 EUR	1424877@Phoenix Contact, Male+female connector
	$k_{Cost_{HouseMod}}$	65.53 $\frac{EUR}{m^2 \cdot kg}$	$Cost_{HouseModREF} = 50EUR$ $Vol_{ModREF} = 33dm^3$ and $Weight_{ModREF} = 55kg$
	$Cost_{TSensor}$	1 EUR	B57861S0103F045@EPCOS, thermistor NTC
	$Cost_{BMS0}$	3.25 EUR	c-BMS100924@ Lithium balance, (Max. 24 cell, ref. price 78EUR)

$$Cost_{OCS} = 2 \cdot (Cost_{SCStr} + Cost_{MSSW} + Cost_{CoolP} + Cost_{HVCI}) + 3 \cdot Cost_{CoolCH} + Cost_{CSensor} + Cost_{StrCtr}$$

With the additional variables and parameters defined as following:

$Cost_{SCStr}$: Service connector cost at string level

$Cost_{MSSW}$: Manual service switch cost
$Cost_{CSensor}$: String Current sensor cost
$Cost_{StrCtr}$: String controller cost
The considered values for the previous parameters are reported in Table 1.

The string cabinet cost ($Cost_{Cabinet}$) is estimated based on its overall volume (Vol_{Cab}), which scales with the number of modules per string as described in section 4.3. The following function has been proposed considering cost data of different battery cabinets/enclosures available in the market:

$$\frac{Cost_{Cabinet}}{Vol_{Cab}} = Cost_{Cab0} + k_{CostCab0} \cdot (Vol_{Cab})^{k_{CostCab1}}$$

where, $Cost_{Cab0}$, $k_{CostCab0}$ and $k_{CostCab1}$ are the fitted parameters for cabinet cost estimation as function of cabinet volume. The family of sheet-steel IP55 industrial cabinets from Schneider Electric manufacturer have been taken as reference string cabinet technology for cost estimation. The reference values along with fitted model for string cabinet cost are shown in Figure 4-1. The fitted parameters are reported in Table 1.

The string inductor cost is evaluated following the methodology described in section 4.7.

The total cost of a module is estimated by

$$Cost_{Mod} = Cost_{ESM} + Cost_{PCM} + Cost_{HouseMod} + Cost_{OCM}$$

Where $Cost_{ESM}$ is the energy storage submodule cost, $Cost_{PCM}$ is the power converter submodule cost, $Cost_{HouseMod}$ is the overall module housing cost, and $Cost_{OCM}$ is the cost of other common components per module, which is estimated by:

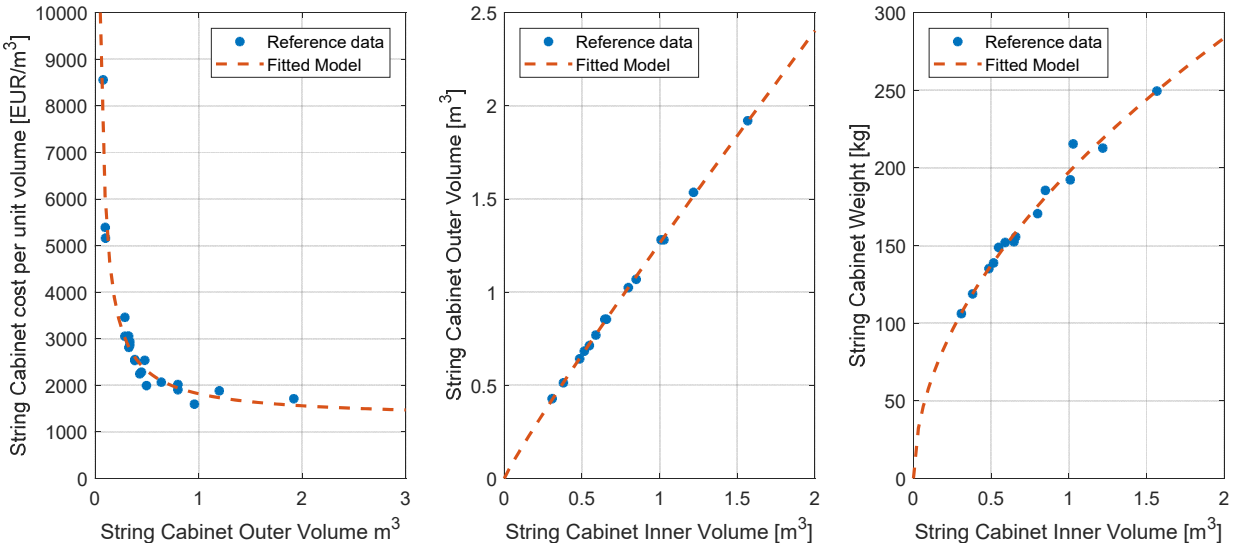


Figure 4-1 String Cabinet model: (left) Cost per unit volume versus outer volume, (middle) inner to outer volume relationship and (right) overall weight to inner volume relationship.

$$Cost_{OCM} = 2 \cdot (Cost_{SCMod} + Cost_{CoolP} + Cost_{CoolCH}) + Cost_{ModF} + Cost_{HVCI} + Cost_{PSC}$$

With the additional variables defined as following:
$Cost_{SCMod}$: service connector cost at module level (signal and power)
$Cost_{ModF}$: module fuse
$Cost_{PSC}$: power supply connector cost

The considered values for the previous parameters are reported in Table 1. Like the HV main fuse, the module fuse should be size according to the module maximum current/power, and therefore its cost is estimated by:

$$Cost_{ModF} = C4W_{ModF} \cdot V_{mod.max} \cdot I_{mod.max}$$

where $C4W_{ModF}$ is the cost per watt of the module fuse, which has been estimated considering a 100A/100V fuse with a reference cost of 33 EUR ($C4W_{ModF} = 3.3\ EUR/kW$).

The module housing cost is estimated assuming that is scales with the module outer area and weight of components, therefore it is approximate by:

$$Cost_{HouseMod} = k_{Cost_{HouseMod}} \cdot Weight_{Mod} \cdot (Vol_{Mod})^{\frac{2}{3}}$$

$$k_{Cost_{HouseMod}} = \left(\frac{Cost_{HouseModREF}}{Weight_{ModREF}}\right) \cdot \left(\frac{1}{Vol_{ModREF}}\right)^{\frac{2}{3}}$$

$k_{Cost_{HouseMod}}$ is the cost of module housing per unit area and unit weight, and $Cost_{HouseModREF}$ is the reference cost for the housing of the reference module with overall volume and weight of Vol_{ModREF} and $Weight_{ModREF}$, respectively. The reference values and parameters are also reported in Table 1.

Finally, $Cost_{ESM}$ and $Cost_{PCM}$ are evaluated following the methodologies described in sections 4.5 and 4.6, respectively.

The following cost components has not been included in this model, so maybe they can be considered for future versions of the algorithm:

- Components related to cell safety: pressure sensor, gas release system, fire management...
- Power supply 5V/24V, (It can be one per string or only one for the full battery system)

4.2 MM-ESS weight

The MM-ESS weight ($Weight_{MMESS}$) has been approximated as the sum of the main and heaviest active component mass, so it is estimated by:

$$Weight_{MMESS} = N_{string} \cdot (Weight_{Lstr} + N_{Mod} \cdot Weight_{Mod} + Weight_{Cab})$$
$$Weight_{Mod} \cong Weight_{ESM} + Weight_{PCM}$$

where, N_{string} is the number of strings, $Weight_{Lstr}$ is the string inductor weight, N_{Mod} is the total number of modules per string, $Weight_{Cab}$ is the overall weight of the empty string cabinet,

$Weight_{ESM}$ is the weight of the energy storage sub-module, and $Weight_{PCM}$ is the weight of the power converter sub-module.

The overall weight of the empty string cabinet has been estimated based on the required inner volume of the cabinet ($Vol_{Cab.Inner}$), by:

$$Weight_{Cab} = k_{massCab0} \cdot \left(Vol_{Cab.Inner}\right)^{k_{massCab1}}$$

where, $k_{massCab0}$ and $k_{massCab1}$ are the meta-parameters for cabinet weight estimation of the considered string cabinet technology. The family of mild-steel free-stand single access industrial cabinets (NEMA Type 12, IP55) from Hoffman manufacturer have been taken as reference string cabinet technology for weight estimation ($k_{massCab0}$=197.3 kg and $k_{massCab1} = 0.524$ when volume in m^3). The reference values along with fitted model for string cabinet weight are shown in Figure 4-1.

The string inductor weight is evaluated following the methodology described in section 4.7, while $Weight_{ESM}$ and $Weight_{PCM}$ are evaluated following the methodologies described in sections 4.5 and 4.6, respectively.

4.3 MM-ESS volume

The MM-ESS volume has been approximated accounting only the overall volume of the string cabinets, therefore it is estimated by:

$$Vol_{MMESS} = N_{string} \cdot Vol_{Cab}$$

where, N_{string} is the number of strings and Vol_{Cab} is the overall volume of the string cabinet, which can be estimated based on the required inner volume of the cabinet ($Vol_{Cab.Inner}$), by:

$$Vol_{Cab} = k_{volCab0} \cdot (Vol_{Cab.Inner})^{k_{volCab1}}$$

where, $k_{volCab0}$ and $k_{volCab1}$ are the meta-parameters for inner to outer cabinet volume estimation of the considered string cabinet technology. The family of mild-steel free-stand single access industrial cabinets (NEMA Type 12, IP55) from Hoffman manufacturer have been taken as reference string cabinet technology for volume estimation ($k_{volCab0}$=1.26m^3 and $k_{volCab1} = 0.929$ when volume in m^3). The reference values along with fitted model for string cabinet volume are shown in Figure 4-1.

The required inner volume for the string cabinet is estimated by:

$$Vol_{Cab.Inner} = \frac{(Vol_{Lstr} + N_{Mod} \cdot Vol_{Mod})}{k_{Ucab}}$$

$$Vol_{Mod} \cong Vol_{ESM} + Vol_{PCM}$$

where, N_{string} is the number of strings, Vol_{Lstr} is the string inductor volume, N_{Mod} is the total number of modules per string, k_{Ucab} is the utilization ratio of volume inside the string cabinet, Vol_{ESM} is the volume of the energy storage sub-module, and Vol_{PCM} is the volume of the power converter sub-module.

The string inductor volume is evaluated following the methodology described in section 4.7, while Vol_{ESM} and Vol_{PCM} are evaluated following the methodologies described in sections 4.5 and 4.6, respectively.

4.4 MM-ESS power losses

The MM-ESS power losses should be evaluated for a given operating point/condition, which is mainly defined by the MM-ESS operating voltage (V_{MMESS}), the MM-ESS power (P_{MMESS}) and the SOC/SOH of all modules composing the MM-ESS.
Considering the power losses at all the operating conditions is impractical for comparing the MM-ESS performance space within the design algorithm, therefore an average value of power losses at the beginning of battery life is considered here, which is described/defined in this section. However, the introduced models in this section for the main MM-ESS components are general enough to allows the power loss evaluation considering different operating conditions.

The MM-ESS power has been assumed to be positive when the MM-ESS is discharging, and negative during charging operation. Depending on the power flow direction the power losses may be different, especially for the battery cells as the internal cell resistance is normally different for charge and discharge operation.

The MM-ESS operating voltage has been constant for all the power loss evaluations. It is considered as the average value between the minimum and maximum operating voltages given as input to the design algorithm:

$$V_{MMESS} = \frac{V_{MMESS.max} + V_{MMESS.min}}{2}$$

Assuming that all strings are equally loaded, then the average string current can be evaluated by:

$$I_{str} = \frac{P_{MMESS}}{N_{string} \cdot V_{MMESS}}; \quad \begin{matrix} I_{str} \geq 0 \; for \; discharge \\ I_{str} < 0 \; for \; charge \end{matrix}$$

To simplify the evaluation, it can be assumed that, at a given operating condition, all the active modules per string have a SOC equal to the total SOC of the MM-ESS (SOC_{MMESS}), therefore the voltage of the module can be approximated to be a function of SOC_{MMESS} and considered to be the same for all active modules. Then, the RMS string current can be approximated by:

$$I_{strRMS}^2 = I_{str}^2 + \left(\frac{f_{sw} \cdot V_{mod}(SOC_{MMESS})}{8 \cdot \sqrt{3} \cdot L_{str}} \right)^2$$

where the string ripple current has been approximated to a triangular waveform and the duty cycle of the PWM converter been 0.5 (worst case for current ripple).

The MM-ESS power losses as function of I_{str} and SOC_{MMESS} (considered operating conditions) can be evaluated by:

$$P_{Loss.MMESS}(I_{str}, SOC_{MMESS}) = N_{string} \cdot (P_{LossL} + P_{LossPCM.SW} + N_{Mod} \cdot P_{LossPCM.Cond} + N_{act} \cdot P_{LossESM})$$

where P_{LossL} are the string inductor power losses, $P_{LossPCM.SW}$ and $P_{LossPCM.Cond}$ are the switching and conduction losses of the power converter sub-module, respectively, N_{act} is the number of active modules per string, N_{Mod} is the number of installed modules per string and $P_{LossESM}$ is the power losses of the energy storage submodule.

It should be mentioned that all modules connected to the string are always conducting the string current (either by connecting the battery module to the string or by passing it), but for a given control period, in average only one module is under PWM operation, which is used to control the string current and/or voltage regulation.

P_{LossL} is a function of the string current, and it is evaluated following the methodology described in section 4.7.

$P_{LossPCM.SW}$ and $P_{LossPCM.Cond}$ are evaluated as described in section 4.6. $P_{LossPCM.Cond}$ is a function of I_{str}, which is mainly determined by the conduction resistance of the power semiconductors, while $P_{LossPCM.SW}$ is a function of I_{str} and the module voltage (V_{mod}), which is a function of SOC_{MMESS}.

$P_{LossESM}$ is evaluated following the methodology described in section 4.5. It is a function of I_{str} and SOC_{MMESS}.

The number of active modules per string is calculated as following:

$$N_{act} = ceil\left\{\frac{V_{MMESS}}{V_{mod}(SOC_{MMESS})}\right\}$$

The average MM-ESS nominal power losses ($P_{LossNOM.MMESS}$) are calculated considering the operating range of SOC_{MMESS}, as following:

$$P_{LossNOM.MMESS} = \frac{1}{\mathrm{USR_{MMESS}}} \cdot \int_{SOC_{mn}}^{SOC_{mx}} P_{Loss.MMESS}(I_{str.MCD}, SOC) \cdot dSOC$$

$$I_{str.MCD} = \frac{P_{MMESS.MCD}}{N_{string} \cdot V_{MMESS}}$$

where, SOC_{mx} and SOC_{mn} are the maximum and minimum SOC for the MM-ESS, $\mathrm{USR_{MMESS}}$ is the MM-ESS Usable SOC Range ($\mathrm{USR_{MMESS}} = SOC_{mx} - SOC_{mn}$), $I_{str.MCD}$ and $I_{str.MCC}$ are the

maximum continuous discharge and charge string current, respectively, and all other variables as previously defined.

Finally, an average MM-ESS power loss value ($P_{LossAVG.MMESS}$) can be calculated considering the operating range of I_{str} and SOC_{MMESS}, as following:

$$P_{LossAVG.MMESS} = \frac{1}{\text{USR}_{\text{MMESS}}} \cdot \int_{SOC_{mn}}^{SOC_{mx}} \int_{-I_{str.MCC}}^{I_{str.MCD}} \frac{P_{Loss.MMESS}(i, SOC)}{(I_{str.MCD} + I_{str.MCC})} \cdot di \cdot dSOC$$

$$I_{str.MCD} = \frac{P_{MMESS.MCD}}{N_{string} \cdot V_{MMESS}}$$
$$I_{str.MCC} = \frac{P_{MMESS.MCC}}{N_{string} \cdot V_{MMESS}}$$

where, SOC_{mx} and SOC_{mn} are the maximum and minimum SOC for the MM-ESS, $\text{USR}_{\text{MMESS}}$ is the MM-ESS Usable SOC Range ($\text{USR}_{\text{MMESS}} = SOC_{mx} - SOC_{mn}$), $I_{str.MCD}$ and $I_{str.MCC}$ are the maximum continuous discharge and charge string current, respectively, and all other variables as previously defined.

4.5 Battery Energy Storage sub-module

The battery energy storage sub-module is mainly composed by three parts: Battery cell array, heatsink and battery management system (BMS).

The cell array composed by $n_{sCell} \cdot n_{pCell}$ battery cells (n_{pCell} parallel connected cell strings each with n_{sCell} series connected cells), which mainly define the battery module nominal electrical properties (voltage V_{mod}, current I_{mod} and energy E_{mod}):.

$$V_{mod} = n_{sCell} \cdot V_{cell}$$
$$I_{mod} = n_{pCell} \cdot I_{cell}$$
$$E_{mod} = n_{sCell} \cdot n_{pCell} \cdot E_{cell}$$

Where, V_{cell} is the cell voltage, I_{cell} is the cell current and E_{cell} is the cell energy capacity. Battery cell thermal management is based on water cooling. The water cooled heatsink is designed/sized to keep cell temperature within a safe range for worst case operating conditions. The model of the battery module water-cooled heatsink developed within this work is described in [4].

The BMS compress all electronics and measurements (temperature and voltage sensors) of the battery module to ensure the correct and balance operation of all battery cells as well as communication with external components.

4.5.1 Battery cells

The considered battery cell technologies are NMC, LFP and LTO (Anode), as they are the most common used in marine applications. Table 2 shows an example of the relevant battery cell properties for different battery cells considered within this work.

The battery cell voltage (V_{cell}) is modelled based on the Open Circuit Voltage (OCV) and the internal series resistance (R_{cell}):

$$V_{cell} = OCV_{cell} - R_{cell} \cdot I_{cell}$$

Where I_{cell} as the cell output current, so $I_{cell} > 0$ when the cell is discharging and $I_{cell} < 0$ when the cell is charging.

Table 2 Reference Battery cells main properties.

General	Chemistry	NMC	NMC	LTO	LFP	NMC	LTO	NMC
	Manufacturer	Kokam	Kokam	Altair-nano	CATL	Samsung-SDI	Toshiba-SCiB	REPT
	Reference	SLPB160460330	SLPB130255255P	70AhNanoLTO	302Ah-LFP	94Ah-NMC	23Ah-LTO	155Ah-NMC
Mechanical	Shape	Pouch			Prismatic			
	Width [mm]	462	268	256	173	173	115	97
	Length [mm]	327	265	263	204	125	103	148
	Thickness [mm]	15.8	13.7	12.4	71.6	45	22	79
	Weight [kg]	4.510	1.830	1.870	5.5	2.1	0.55	2.65
Electrical (@ 25°C)	Capacity [Ah] (@Crate)	240 (0.2C)	75 (0.2C)	68.5 (1C)	302 (1C)	94 (0.3 C)	23 (1C)	155 (1C)
	Nominal Energy [Wh]	888	277.5	151	995	345	53	566
	Average Voltage [V]	3.7	3.7	2.21	3.22	3.68	2.3	3.65
	Lower Limit Voltage[V]	2.7	2.7	1.5	2.7	2.7	1.5	2.8
	Upper Limit Voltage[V]	4.2	4.2	2.9	4.15	4.15	2.7	4.3
	Max. Cont. Charge Current [A]	240 (1C)	300 (4C)	500 (~7C)	604 (2C)	72 (~0.8C)	92 (4C)	186 (1.2C)
	Max. Cont. Discharge Current [A]	480 (2C)	600 (8C)	500 (~7C)	906 (3C)	150 (~1.6C)	92 (4C)	310 (2C)
	Max. Peak Dch. Current [A] (10s, SOC≥50%)	720 (3C)	1125 (15C)	900 (~13C)	--	409 (~4.35C)	184 (8C)	465 (3C)
	Internal resistance Ch./Dch. [mΩ] (@SOC)	0.5/0.5 (30%)	0.4/0.4 (30%)	0.4/0.4 (50%)	0.45/0.45 (50%)	0.79/0.79 (50%)	1.17/1.17 (50%)	0.6/0.6 (50%)
Thermal	Rapid Charging Temperature [°C]	10 ~ 35	10 ~ 35	-50 ~ 65	0 ~ 65	~ 60	-30 ~ 55	-20 ~ 55
	Discharge temperature [°C]	-20 ~ 55	-20 ~ 55	-50 ~ 65	-35 ~ 65	-40 ~ 60	-30 ~ 55	-30 ~ 55
	Thermal conduct. [W/mK] Parallel to layers (κ_{Cellx})	0.3566	0.7	0.85	--	1.7	0.8	1.7
	Thermal conduct. [W/mK] Across layers (κ_{Celly})	30	40	50	--	30	31	30
Others	Cycle life: Cycles	6000	6000	25000	1500	4255	11756	1400
	Cycle life: DoD [%]	90	90	100	100	100	100	80
	Cycle life: Charge/Discharge	1C/1C	1C/1C	2C/2C	1C/1C	0.5C/1C	1C/1C	1C/1C
	Cycle life: Temperature [°C]	25	25	25	25	25	25	25
	Cycle life: EOL capacity [%]	70	70	80	80	80	80	80
	Calendar life: Capacity loss per year [%]	2	2	0.8	1	1	1	1
	Unit price [EUR]	802	251	172	210	250	57	103

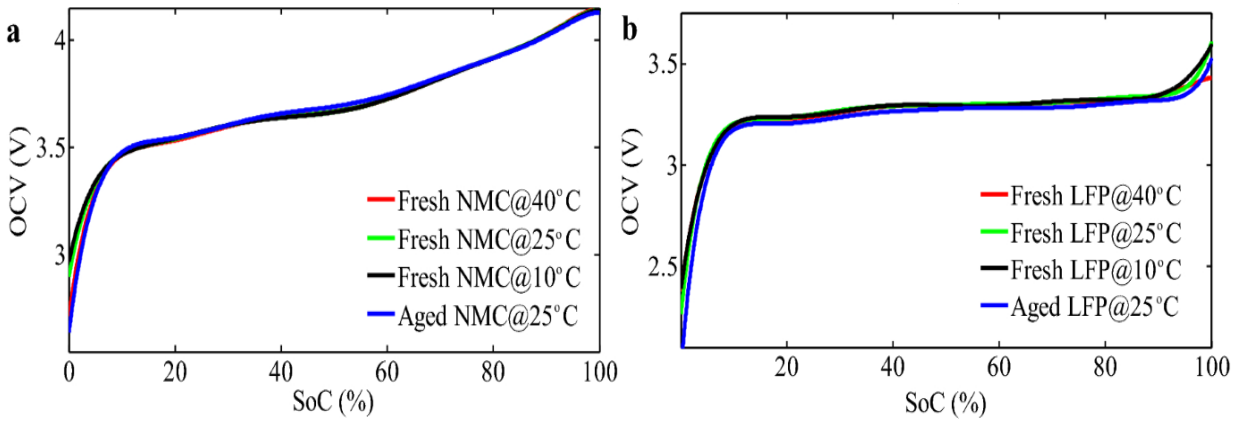
4.5.1.1 Open Circuit Voltage (OCV)

The cell OCV is a function of SOC and cell temperature. OCV also change as the cell is aged. Figure 4-2 shows examples of OCV-SOC and temperature relationship for different battery cells as reported in other studies.
Regarding the OCV-Temperature relationship, the following observations can be done for cell temperatures higher than 10°C:

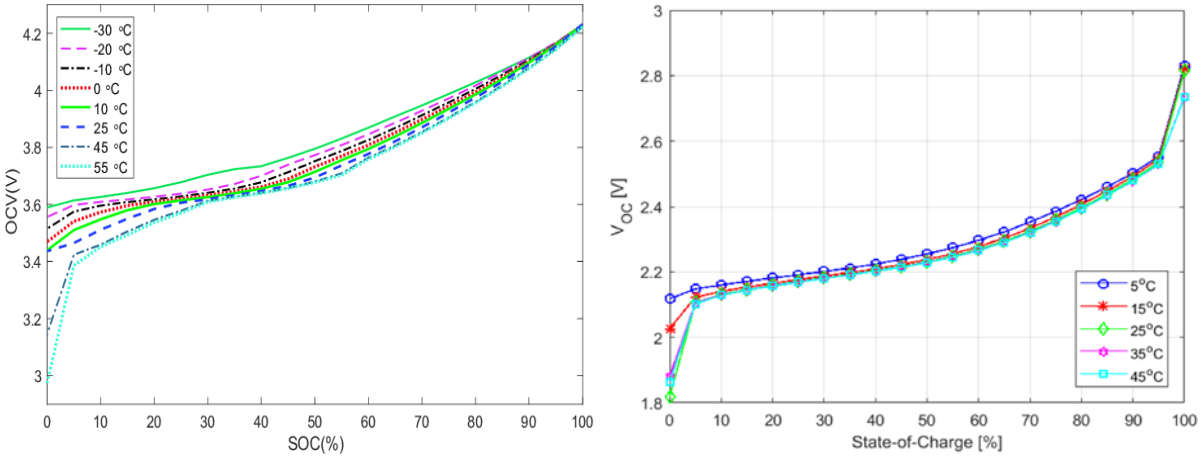
- For NMC cell technology: OCV reduces as temperature increases, more drastically for SOC<40%.
- For LFP cells: OCV for SOC >70% increases as temperature increases and OCV for SOC<30% reduces as temperature increases.

It can be observed that OCV versus SOC dependency is more significant compared with temperature dependency. Therefore, OCV-temperature dependency has been neglected within this study.

OCV-SOC curve may be provided by cell manufacturer, however, in case this information is not available for a given cell, then it is assumed that the OCV-SOC relationship is similar for cells with



a) NMC cell – (Fresh vs aged) (source: [23]) b) LFP cell – (Fresh vs aged) source: [23]



c) NMC cell (source: [22]) d) LTO cell (source [24])

Figure 4-2 Example of OCV-SOC-Temperature for the considered cell technologies

same chemistry/technology, so a normalized OCV is considered for each cell technology which is estimated based on the SOC-OCV model proposed in [5]:

$$\frac{OCV}{V_{cell.avg}} = \left(k_{aOCV} + k_{bOCV} \cdot (-\log SOC)^{k_{mOCV}} + k_{cOCV} \cdot SOC + k_{dOCV} \cdot \exp\left(k_{nOCV} \cdot (SOC - 1)\right)\right)$$

$$0 \leq SOC \leq 1$$

The OCV-SOC parameters for the NMC, LFP and LTO cell technologies are presented in Table 3. Figure 4-3 shows a comparison of normalized OCV-SOC curves for the considered battery cell technologies based on the previous model and parameters in Table 3.

Table 3 OCV-SOC model parameters for considered battery cell technologies (reference cell temperature 25°C).

Battery type	k_{aOCV}	k_{bOCV}	k_{cOCV}	k_{dOCV}	k_{mOCV}	k_{nOCV}
NMC	0.9393	-0.0090	-0.0284	0.1986	1.4030	2
LFP	0.9533	-0.2083	-0.4081	0.5273	0.4780	0.4
*LTO**	0.9332	-0.0005512	-0.1463	0.2861	2.9640	1.6

*Cathode: LNMCO+LMO

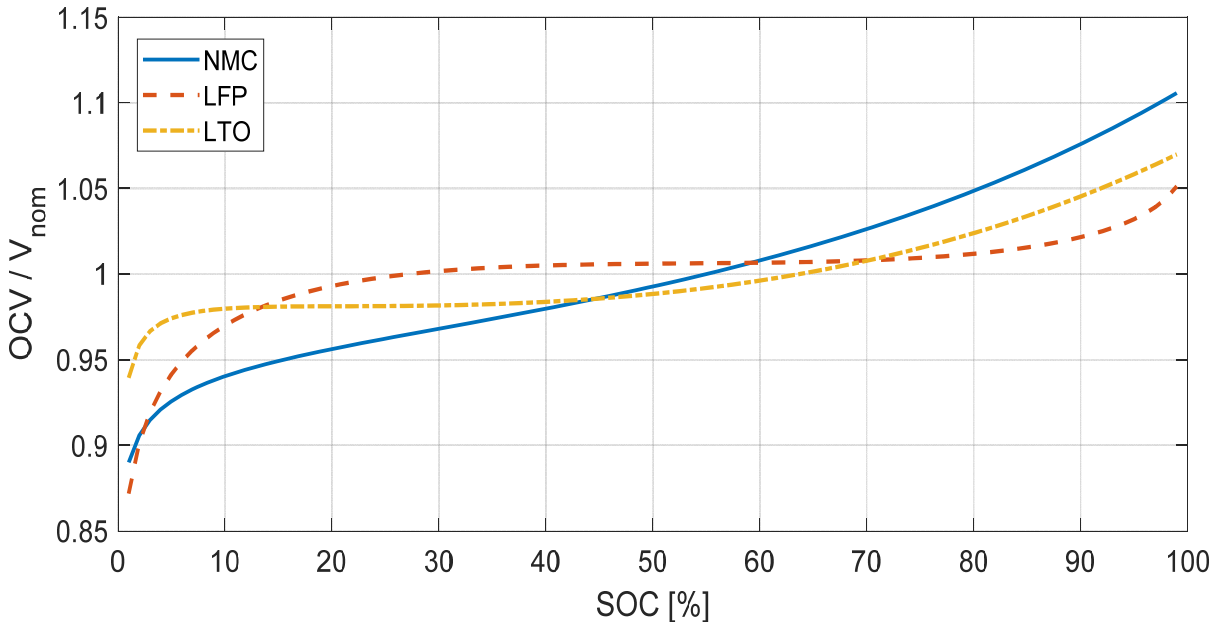


Figure 4-3 Normalized OCV-SOC curves for the considered battery cell technologies.

4.5.1.2 Internal cell resistance

Internal cell resistance mainly changes as function of temperature, SOC, and State of Health (SOH)/aging. Figure 4-4 shows an example of cell resistance versus SOC curves for the considered cell technologies.
Cell resistance vs SOC/temperature may be provided by the cell manufacturer, however, in case that information is not available, the manufacturer normally provided a reference cell resistance value ($R_{cellREF}$) at reference conditions, then the following model is proposed to model the cell resistance:

$$R_{cell} = fun(T, SOC, SOH) \approx R_{cellREF} \cdot R_{nT}(T_{cell}, SOH) \cdot R_{nSOC}(SOC, SOH)$$

$$R_{cellREF} = R_{Cell}(T_{CellREF}, SOC_{REF}, SOH = 100\%)$$

$$R_{nT}(T_{cell}, SOH) \approx \frac{R_{cell}(T_{cell}, SOC_{REF}, SOH)}{R_{CellREF}} = \frac{k_{RnT}}{\exp\left(-\frac{E_a(SOH)}{R_{gas} \cdot T_{cell}}\right)}$$

$$R_{nSOC}(SOC, SOH) \approx \frac{R_{cell}(T_{REF}, SOC, SOH)}{R_{cellREF}} = k_{Rsoc0}(SOH) + k_{Rsoc1}(SOH) \cdot (SOC - k_{Rsoc2})^{k_{Rsoc3}}$$

$$0 \leq SOC \leq 1$$

R_{nT} normalized cell resistance -temperature dependency, which follows the Arrhenius equation [6].
R_{nSOC}: normalized cell resistance-SOC dependency.
R_{gas} gas constant (8.314 J /(mol K))
E_a: Activation energy [J/mol] (for NMC range 50-60 kJ/mol new cell, for LFP 25-35 kJ/mol; for NCA 41kJ/mol (new cell) and 44kJ/mol aged cell). E_a increases as cell ageing.
T_{cell}: cell temperature [K]
k_{Rsoc0}: used to fit equation for the $R_{cellREF}$ when SOC_{REF} different that k_{Rsoc2}. It increases as cell ageing.

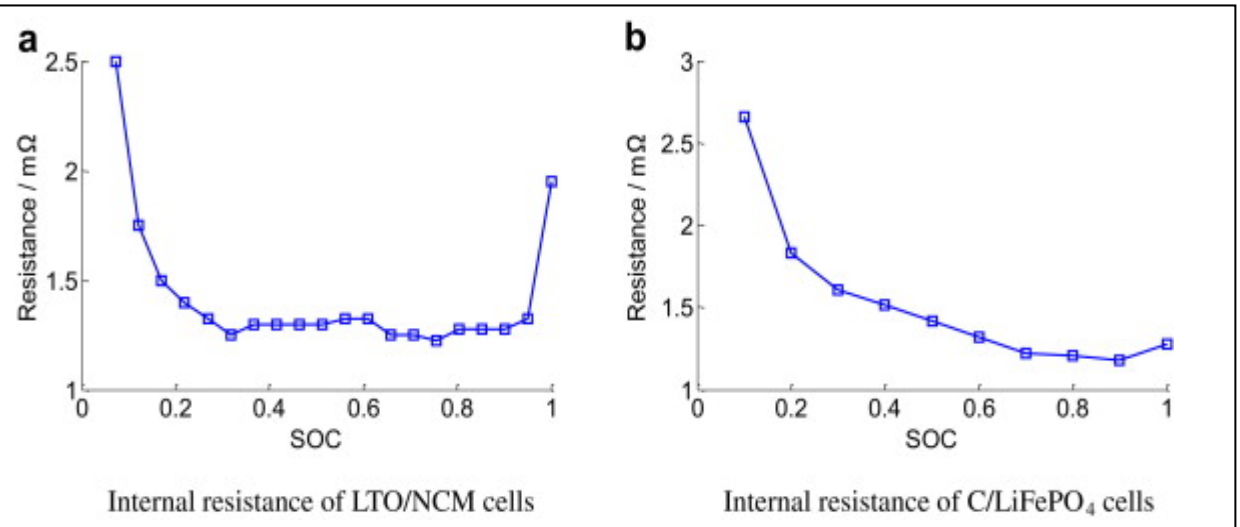


Figure 4-4 Example of cell resistance versus SOC curve for the considered cell technologies (source: [25]). a) LTO/NMC cells, b) LFP cells

k_{Rsoc1}: increases as cell ageing.
k_{Rsoc2}: around 0.5 for NMC/LTO, around 0.8 for LFP
k_{Rsoc3}: even number (4-8 for NMC/LTO), 2-4 for LFP, and >12 for constant R_{cell} vs SOC relationship.

For the scope of this study, the temperature dependency has been neglected, so $R_{nT} = 1$.
Figure 4-5 shows an example of R_{nSOC} evaluated with the proposed model fitted to the curves in Figure 4-4. Figure 4-6 shows an example of modelled NMC cell voltage including a comparison of influence of cell resistance-SOC variations versus constant cell resistance.

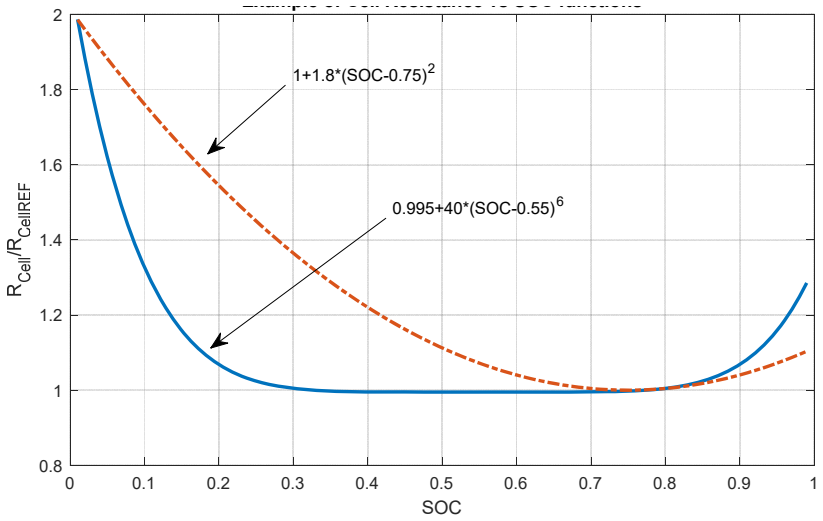


Figure 4-5 Normalized cell resistance-SOC dependency evaluated with the proposed model. Blue curve fitted for NMC/LTO cells; red curve fitted for LFP cells.

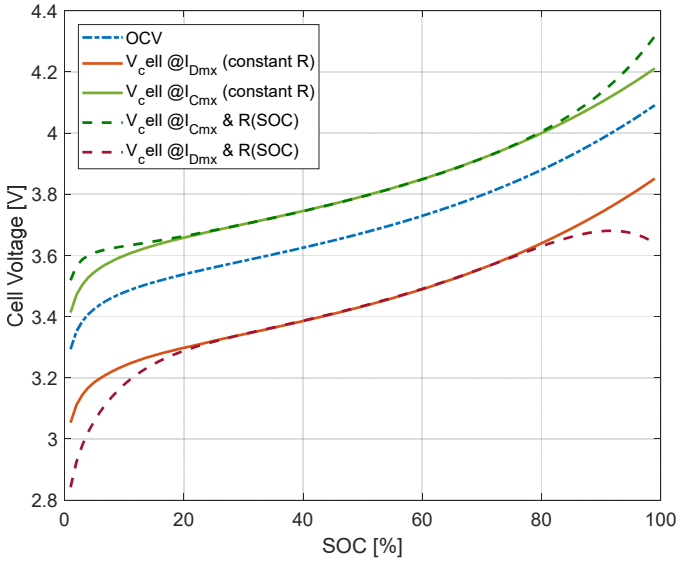


Figure 4-6 Example of modelled NMC cell voltage. Comparison of influence of cell resistance-SOC variations versus constant cell resistance.

4.5.2 Module voltage

Considering the previous battery cell model, then the battery module voltage can be estimated by:

$$V_{mod}(SOC, I_{mod}) = OCV_{mod}(SOC) - R_{mod}(SOC) \cdot I_{mod}$$

$$OCV_{mod}(SOC) = n_{sCell} \cdot OCV_{cell}(SOC)$$

$$R_{mod}(SOC) = \frac{n_{sCell}}{n_{pCell}} \cdot R_{cell}(SOC)$$

where, OCV_{mod} is the equivalent module OCV and R_{mod} is the module internal resistance.

4.5.3 Thermal management

As previously commented in section 3.4, the battery cell thermal management is based on a water-cooling architecture with thermal conductive fins and cold plates as illustrated in Figure 3-2. The model, design methodology and implementation of the battery module water-cooled heatsink developed within this work is described in [4]. Here, a summary is included for the sake of completeness.

Figure 4-7 shows a simplified thermal model for the water-cooling system based on conductive thermal fins and cold plates. The average thermal resistance per cell of the fin-cooling system ($R_{thHS.FIN}$) can be estimated as follows:

$$R_{thHS.FIN} = \frac{\left(R_{thCellx} + R_{thTPx} + \frac{R_{thFin}}{2} + R_{thBi}\right) \cdot \left(R_{thCelly} + R_{thTPy} + R_{thB}\right)}{R_{thCellx} + R_{thTPx} + \frac{R_{thFin}}{2} + R_{thBi} + 2 \cdot (R_{thCelly} + R_{thTPy} + R_{thB})} + \frac{R_{thTPCPi}}{2}$$

where $R_{thCellx}$ and $R_{thCelly}$ are the in-plane and trough-plane cell thermal resistance (from centre of the cell to the cell surface), respectively, R_{thFin} is the fin thermal resistance, R_{thB} is the base thermal resistance, R_{thBi} is the fin-base thermal resistance (equivalent for the fin path), $R_{thTPx/y}$ are the thermal pad thermal resistances (between cell and fin/base) and $R_{thTPCPi}$ is the portion of cold plate thermal resistance (R_{thCP}) and thermal pad (between base and cold plate) thermal resistance (R_{thTPcp}) per cell assuming uniform heat distribution along the cold plate surface ($R_{thTPCPi} = n_{cell} \cdot (R_{thCP} + R_{thTPcp})$).

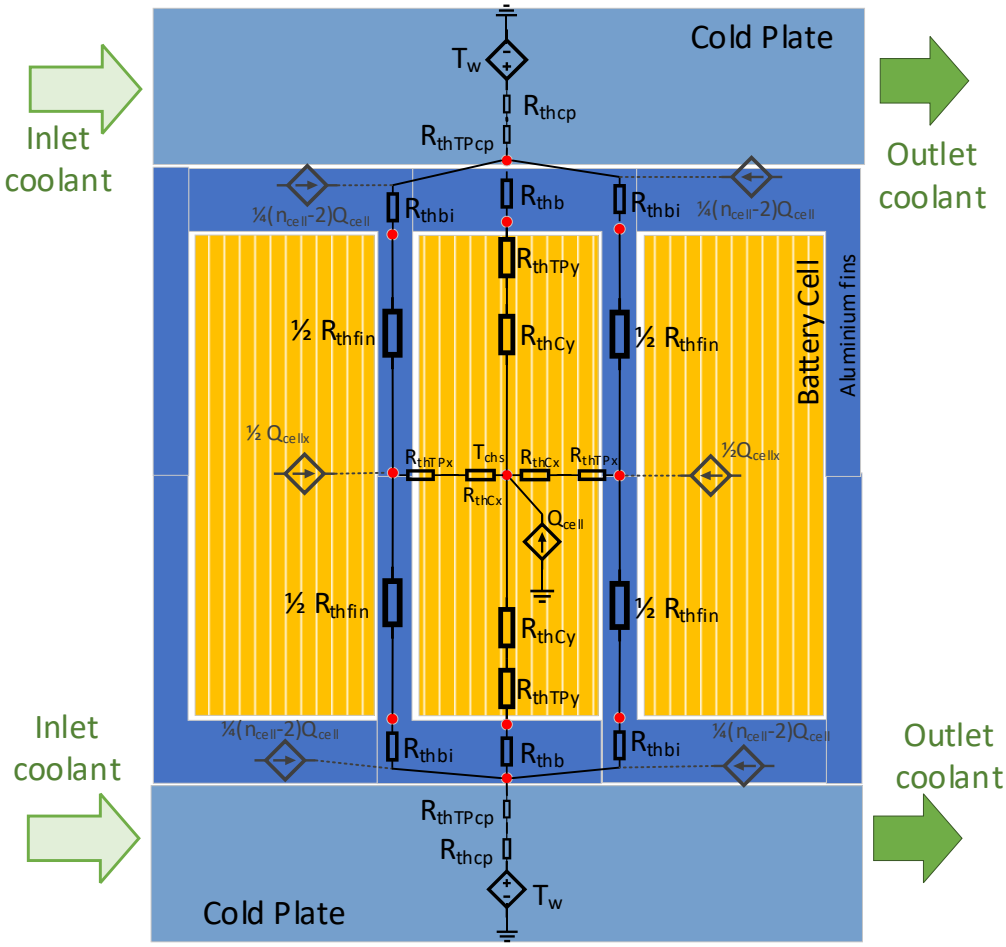


Figure 4-7 Simplified thermal model for water cooling system based on conductive thermal fins and cold plates.

The cell thermal resistances are estimated based on the cell dimensions W_{cell} (width), L_{cell} (length), t_{cell} (thickness) and the equivalent/average in-plane and trough-plane cell thermal conductivities (κ_{Cellx} and κ_{Celly}), by

$$R_{thCellx} = \frac{t_{cell}}{2 \cdot \kappa_{Cellx} \cdot L_{cell} \cdot W_{cell}}$$

$$R_{thCelly} = \frac{W_{cell}}{2 \cdot \kappa_{Celly} \cdot L_{cell} \cdot t_{cell}}$$

The fin thermal resistance (R_{thFin}) is calculated based on the fin thickness (t_{Fin}) and the thermal conductivity of the fin material (typically Al but Cu could be considered to get better thermal resistance to volume trade-off):

$$R_{thFin} = \frac{L_{cell}}{\kappa_{Fin} \cdot W_{cell} \cdot t_{Fin}}$$

The base thermal resistances are calculated as follows:

$$R_{thBi} = \frac{t_{base}}{\kappa_{Fin} \cdot L_{cell} \cdot (t_{Fin} + 2 \cdot t_{base} \cdot \tan(\alpha_{Fin}))}$$

$$R_{thB} = \frac{t_{base}}{\kappa_{Fin} \cdot L_{cell} \cdot (t_{Fin} + t_{cell})}$$

where t_{base} is the fin base thickness and α_{Fin} is the thermal spreading angle for the thermal conductor material [7].

The pad thermal resistances (R_{thTPx} , R_{thTPy} and R_{thTPcp}) are calculated based on the thermal pad thickness (t_{TP}) and its thermal conductivity (κ_{TP}):

$$R_{thTPx} = \frac{t_{TP}}{\kappa_{TP} \cdot W_{cell} \cdot L_{Cell}}$$
$$R_{thTPy} = \frac{t_{TP}}{\kappa_{TP} \cdot t_{cell} \cdot L_{Cell}}$$
$$R_{thTPcp} = \frac{t_{TP}}{\kappa_{TP} \cdot W_{CP} \cdot L_{CP}}$$

The thermal resistance of a cold plate can be estimated by:

$$R_{thCP}(A_{BCP}, t_{CP}, V_{FR}) = \frac{K_{CPR0}}{A_{BCP}^{k_{CPRA}} \cdot t_{CP}^{k_{CPRt}} \cdot V_{FR}^{k_{CPRFR}}}$$

where A_{BCP} is the cold plate base surface, t_{CP} is the cold plate thickness, V_{FR} is the inlet water flow rate (dm3/min), and K_{CPR0}, K_{CPRA}, K_{CPRt} and K_{CPRFR} are proportionality regression coefficients (meta-parameters) found by taking data from the different cold plate technologies (see appendix A). Then, the cold plate thermal resistance per cell ($R_{thTPCPi}$) can be calculated as follows:

$$R_{thTPCPi} = n_{cell} \cdot \left(R_{thCP}(W_{CP} \cdot L_{CP}, t_{CP}, V_{FR}) + R_{thTPcp}\right)$$

$$W_{CP} = n_{Cell} \cdot (t_{cell} + 2 \cdot t_{TP}) + (n_{Cell} + 1) \cdot t_{Fin}$$

$$L_{CP} = L_{Cell}$$

where $(W_{CP} \cdot L_{CP})$ is the total base area of the top and bottom cold plates. Table 4 reports the

Table 4 Fin cooling parameters

	Parameter	**Value**
Thermal Pad Reference material: H48-6 / TG-AH486 @ T-Global Technology	Thermal Conductivity (κ_{TP})	3.4 [W/mK]
	Thickness (t_{TP})	0.3 [mm]
	Density (ρ_{TP})	2420 [kg/m3]
	Cost density ($Cost_{TP1}$)	60 [EUR/kg]
Thermal conductive fin Reference material: • 6063 aluminium alloy • Cooper	Thermal Conductivity (κ_{Fin})	Al: 210 [W/mK] Cu: 386 [W/mK]
	Thermal spreading angle (α_{Fin}):	Al: 40° Cu: 45°
	Density (ρ_{Fin})	Al: 2690 [kg/m3] Cu: 8940 [kg/m3]
	Cost density ($Cost_{FIN1}$)	Al: 3.2 [EUR/kg] [21] Cu: 6 [EUR/kg]
	Cost per unit ($Cost_{FIN0}$)	0.1 [EUR] [21]
	Minimum Thickness	0.5 [mm]
	Maximum Thickness	0.5*t_{Cell}

considered fin cooling parameters within this study.

4.5.4 Cost

The cost of the battery energy storage sub-module ($Cost_{ESM}$) is evaluated considering its three main components, as following:

$$Cost_{ESM} = n_{scell} \cdot n_{pcell} \cdot Cost_{cell} + Cost_{HSBC} + Cost_{BMS}$$

where $Cost_{cell}$ is the cost of a single battery cell, $Cost_{HSBC}$ is the cost of the battery heatsink system, and $Cost_{BMS}$ is the BMS cost.

The battery heatsink total cost can be estimated as the sum of cost for its main components (thermal pads, cooling fins and cold plates):

$$Cost_{HSBC} = Cost_{TP} + Cost_{Fin} + Cost_{CP}$$

$$Cost_{TP} = Cost_{TP1} \cdot Weight_{TP}$$

$$Cost_{Fin} = Cost_{Fin0} \cdot (n_{Cell} + 1) + Cost_{Fin1} \cdot Weight_{Fin}$$

where $Cost_{TP1}$ is the cost per kg for the thermal pad material, $Cost_{Fin1}$ is the cost per kg of the fin material (Al or Cu), $Cost_{Fin0}$ is the unit cost per fin, and $Cost_{CP}$ is the cost of the cold plate, which can be evaluated following the methodology introduced in appendix A.

The module battery management system cost ($Cost_{BMS}$) is calculated according to

$$Cost_{BMS} = Cost_{BMS0} \cdot n_{scell} \cdot n_{pcell} + Cost_{Tsensor} \cdot \frac{n_{scell} \cdot n_{pcell}}{4}$$

where $Cost_{BMS0}$ is the average BMS cost per cell, and $Cost_{Tsensor}$ is the cost of temperature sensor (assuming installation of one sensor for every four cells in the module). The considered values for these parameters are reported in Table 1.

4.5.5 Weight

The weight of the energy storage sub-module is mainly defined by the battery array and the heatsink, so it is evaluated by

$$Weight_{ESM} = n_{scell} \cdot n_{pcell} \cdot Weight_{cell} + Weight_{HSBC}$$

where, $Weight_{cell}$ is the weight of a single battery cell and $Weight_{HSBC}$ is the total weight of the battery heatsink, which is calculated by:

$$Weight_{HSBC} = Weight_{Fin} + Weight_{TP} + Weight_{CP}$$

$$Weight_{Fin} = \rho_{Fin} \cdot (W_{Cell} \cdot t_{Fin} \cdot L_{Cell} \cdot (n_{Cell} + 1) + 2 \cdot W_{CP} \cdot L_{CP} \cdot t_{Base})$$

$$Weight_{TP} = 2 \cdot \rho_{TP} \cdot t_{TP} \cdot (n_{Cell} \cdot L_{Cell} \cdot (W_{Cell} + t_{Cell}) + W_{CP} \cdot L_{CP})$$

where $Weight_{Fin}$ is the total weight of the thermal conductive fin and base, $Weight_{TP}$ is the total weight of the thermal pad material between cell and fin/base and cold plate, ρ_{Fin}, and ρ_{TP}, are the densities of the thermal conductive fin material (Al or Cu) and thermal pad material, respectively, and $Weight_{CP}$ is the cold plates weight, which can be evaluated following the methodology introduced in appendix A.

4.5.6 Volume

The volume of the energy storage sub-module (Vol_{ESM}) is determined by the total number of cells per module and the designed heatsink for the battery cells. Considering Figure 3-2, it can be estimated as follows:

$$Vol_{ESM} = (W_{CP} + 2 \cdot \Delta X_{HS}) \cdot (L_{CP} + 2 \cdot \Delta X_{HS}) \cdot \left(W_{Cell} + 2 \cdot (t_{Base} + t_{TP} + t_{CP} + \Delta X_{HS})\right)$$

where ΔX_{HS} is a delta space for module/heatsink volume evaluation accounting cold plate supports, insulation, terminals along others. A module configuration with one row of $n_{Cell} (= n_{scell} \cdot n_{pcell})$ battery cells is assumed to simplify the heatsink design evaluation, however, alternatively the number of rows can be vary placing double side cold plates between cell rows in case maximum module dimension constraint need to be considered.

4.5.7 Power losses

The power losses of the energy storage submodule are mainly determined by the internal resistance of the battery cells; therefore, it is evaluated as follows:

$$P_{LossESM}(SOC, I_{mod}) = R_{mod}(SOC) \cdot I_{mod}^2$$

with the cell internal resistance modelled as function of SOC following section 4.5.1.2.

When the battery sub-module is connected to the string, the module current is equal to the string current (I_{str}), therefore the power losses can be approximated by:

$$P_{LossESM}(SOC, I_{str}) = R_{mod}(SOC) \cdot \left(I_{str}^2 + \left(\frac{f_{sw} \cdot (OCV_{mod}(SOC) - R_{mod}(SOC) \cdot I_{str})}{8 \cdot \sqrt{3} \cdot L_{str}} \right)^2 \right)$$

4.6 DC/DC Power Converter Sub-module

The DC/DC power converter sub-module is based on a half bridge topology which is shown in Figure 3-5. The Power converter is modelled based on the power cell board layout presented in Figure 3-7, and following the design rules presented in section 3.5.

4.6.1 Capacitor bank

The capacitor bank is modelled as N_{cdc} parallel connected capacitors with single discrete capacitance C_{DCi}, so the total capacitance C_{DC} is

$$C_{DC} = N_{cdc} \cdot C_{DCi}$$

The DC capacitors are modelled following the meta-models presented in appendix A.1.
The capacitor bank in this application is mainly considered for snubber function but not DC-link energy buffer. Film capacitors are considered for this propose. The MKP film capacitors series B3265x from EPCOS manufacturer has been considered as reference capacitor technology. Meta-parameters for this technology are introduced in appendix A.1.

N_{cdc} is determine by the maximum energy of a discrete capacitor (E_{Cmax}), which depends on the selected technology:

$$N_{cdc} = ceil\left(\frac{0.5 \cdot C_{DC} \cdot V_{mod.max}^2}{E_{Cmax}}\right)$$

Then, C_{DCi} is calculated to fulfil the two design guidelines introduced in section 3.5.3.1:

$$C_{DCi} \geq \frac{1}{N_{cdc}} \cdot \frac{L_{\delta BC} \cdot I_{mod.max}^2}{(\delta V_{dc} \cdot V_{mod.max})^2}$$

$$\frac{dV_c}{dt}_{MAX} \geq \frac{I_{mod.max}}{C_{DC}}$$

The maximum allowed dV/dt for a discrete capacitor $\left(\frac{dV_c}{dt}_{MAX}\right)$ is estimated by:

$$\frac{dV_c}{dt}_{MAX} = k_{Cdv0} \cdot \left(C_{DCi}\right)^{k_{CdvC}} \cdot \left(V_{mod.max}\right)^{k_{CdvV}}$$

where, k_{Cdv0}, k_{CdvC}, k_{CdvV} are the capacitor meta-parameters for $\frac{dV_c}{dt}_{MAX}$ estimation of the considered capacitor technology.

The total bank capacitor volume (Vol_{Cdc}) and weight ($Weight_{Cdc}$) is calculated by:

$$Vol_{Cdc} = KS_{Cdc} \cdot N_{cdc} \cdot Vol_{Cdci}$$

$$Weight_{Cdc} = N_{cdc} \cdot Weight_{Cdci}$$
$$Vol_{Cdci} = k_{Cvol0} \cdot (C_{DCi})^{k_{CvolC}} \cdot (V_{mod.max})^{k_{CvolV}}$$

$$Weight_{Cdci} = k_{Cp0} \cdot (Vol_{Cdci})^{k_{CpVol}}$$

where, KS_{Cdc} is a space factor to consider the space between discrete capacitors, Vol_{Cdci} is the volume of a discrete capacitor, and k_{Cvol0}, k_{CvolC}, k_{CvolV} and k_{Cp0}, k_{CpVol} are the capacitor meta-parameters for volume and weight estimation, respectively.

The height of the single discrete capacitors composing the capacitor bank (H_{Cdci}) is estimated by

$$H_{Cdci} = k_{Ch0} \cdot (C_{DCi})^{k_{ChC}} \cdot (V_{mod.max})^{k_{ChV}}$$

where, k_{Ch0}, k_{ChC}, k_{ChV} are the capacitor meta-parameters for single capacitor high estimation of the considered capacitor technology.

The capacitor bank losses are neglected for this topology.

Finally, the total cost of the capacitor bank is calculated by:

$$Cost_{Cdc} = N_{cdc} \cdot (Cost_{Cdc0} + k_{Ccost0} \cdot (C_{DCi})^{k_{CcostC}} \cdot (V_{mod.max})^{k_{CcostV}})$$

where, $Cost_{Cdc0}$, k_{Ccost0}, k_{CcostC}, k_{CcostV} are the capacitor meta-parameters for cost estimation of single capacitor C_{DCi} and for the considered capacitor technology.

4.6.2 Power Switch Device (PSD)

A PSD is modelled as n_{pMOS} semiconductor devices parallel connected with the Power MOSFET as core technology. StrongIRFET Power MOSFETs from Infineon has been considered as core semiconductor technology. The half bridge topology has two paired PSDs, so the power converter sub-module has in total $2 \cdot n_{pMOS}$ Power MOSFET devices.

The total cost of power switch devices ($Cost_{PSD}$) is calculated as follows:

$$Cost_{PSD} = 2 \cdot n_{pMOS} \cdot (Cost_{PSD0} + Cost_{MOSFET})$$

where,

$Cost_{MOSFET}$: is the Power MOSFET device cost, which depends on blocking voltage and chip area:

$$Cost_{MOSFET} = Cost_{MOS0} + k_{MOS.cost0} \cdot (V_{block})^{k_{MOS.cost1}} \cdot \left(A_{chip}\right)^{k_{MOS.cost2}}$$

$Cost_{PSD0}$: is other PSD component cost. This includes the external gate resistances R_{gON} and R_{gOFF}, RC snubbers and Ferrite bead. Constant value ($Cost_{PSD0} \approx 0.3\ Euro$)

The weight of the PSDs is estimated by:

$$Weight_{PSD} = 2 \cdot n_{pMOS} \cdot N_{cPSD} \cdot Weigth_{CompAVG}$$

$Weigth_{CompAVG}$: average electronic component weight.

N_{cPSD}: number of discrete components per MOSFET in the PSD.

The power losses in a power MOSFET operating in the switch-mode can be divided into conduction losses, switching losses and gate losses. The MOSFET losses models are introduced in the following sub-sections.

4.6.2.1 Conduction Losses

Conduction losses in the power MOSFET are calculated using the drain-source on-state resistance approximation (R_{DS}):

$$v_{DS} = R_{DS}(i_D, V_{GS}, T_j) \cdot i_D$$

where v_{DS} and i_D are the drain-source voltage and the drain current, respectively. The on-state resistance depends on junction temperature (T_{jMOS}), gate-source voltage (V_{GS}) and drain current, and their relationships can be typically found in the device datasheet. For switch-mode operation, V_{GS} is normally set so that the on-state MOSFET v_{DS} vs. i_D characteristic is as lineal as possible (R_{DS} invariant with i_D), then neglecting the T_{jMOS} variations in the period (T), the average MOSFET conduction losses ($P_{condMOSi}$) can be found by [8]:

$$P_{condMOSi} = \frac{1}{T} \cdot \int_0^T v_{DS}(t) \cdot i_D(t) \cdot dt = \frac{1}{T} \cdot \int_0^T R_{DS}(T_{jMOS}) \cdot i_D^2(t) \cdot dt = R_{DS}(T_{jMOS}) \cdot I_{MOS,rms}^2$$

where $I_{MOS,rms}$ is the rms value of the MOSFET on-state current. To calculate the on-state resistance thermal dependency, the following formula is used [9]:

$$R_{DS}(T_{jMOS}) = R_{DS.REF} \cdot \left(1 + \frac{\alpha_{R_{DS}}}{100}\right)^{T_{jMOS} - T_{jREF}}$$

where $\alpha_{R_{DS}}$ is the thermal coefficient of the on-state resistance, which can be calculated from the typical data reported in the device datasheet, and $R_{DS.REF}$ is the on-state resistance at reference junction temperature T_{jREF}. Based on the analysis presented in appendix A.2, the Power MOSFET conduction parameters are evaluated as function of equivalent chip area (A_{chip}) and blocking voltage (V_{Block}):

$$R_{DS.REF} = \frac{k_{MOS.RD0} + k_{MOS.RD1} \cdot (V_{block})^{k_{MOS.RD2}}}{A_{chip}}$$

$$\alpha_{R_{DS}} = k_{MOS.\alpha 0} \cdot (V_{block})^{k_{MOS.\alpha 1}}$$

Where, $k_{MOS.RD0}, k_{MOS.RD1}, k_{MOS.RD2}, k_{MOS.\alpha 0}$ and $k_{MOS.\alpha 1}$ are the meta-parameters for on-state resistance evaluation of single Power MOSFET.

4.6.2.2 Switching Losses

The switching losses can be estimated based on the energy loss during each switching action:

$$P_{swMOSi} = P_{swON} + P_{swOFF}$$
$$P_{swON} = E_{on}(V_{DD}, I_{Don}) \cdot f_{sw}$$
$$P_{swOFF} = E_{off}(V_{DD}, I_{Doff}) \cdot f_{sw}$$

For the turn-on energy loss calculation, the reverse-recovery of the free-wheeling diode of paired PSD in the half bridge need to be considered, so the total energy loss related with turn-on process can be estimated by:

$$E_{on} = \frac{1}{2} \cdot V_{DD} \cdot I_{Don} \cdot \left(t_{rc} + t_{rr} + t_{fv}\right) + \frac{5}{4} \cdot Q_{rr} \cdot V_{DD}$$

where, V_{DD} is the blocked voltage before turn-on action, I_{Don} is the conducted current after turn-on action, t_{rc} is the current rise time at turn on, t_{rr} is the reverse-recovery time of free-wheeling diode turn-off process, t_{fv} is the voltage fall time at turn on, and Q_{rr} is the reverse-recovery charge of the free-wheeling diode.

The current rise time at turn on (t_{rc}) can be approximated by

$$t_{rc} = \tau_{Gon} \cdot \left(-\log\left(1 - \frac{V_{pl}}{V_{Dr}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{Dr}}\right)\right),$$

where τ_{Gon} is the time constant for gate turn-on process, assumed proportional to the total gate circuit resistance for turn-on process and input capacitance of the power MOSFET; V_{pl} is the gate-source plateau voltage (Miller effect), $V_{GS(th)}$ is the gate-source threshold voltage and V_{Dr}: driver voltage. Since τ_{Gon} is a parameter difficult to estimate, alternatively t_{rc} can be estimated by

$$t_{rc} \approx t_{rc0} \cdot \frac{R_{Gon}}{R_{GonREF}} \cdot \frac{\left(-\log\left(1 - \frac{V_{pl}}{V_{Dr}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{Dr}}\right)\right)}{\left(-\log\left(1 - \frac{V_{pl}}{V_{DrREF}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{DrREF}}\right)\right)}$$

where t_{rc0} is the reference current rise time, which is a given value in the device datasheet for reference conditions R_{GonREF} (reference total gate circuit resistance for turning on process) and V_{DrREF} (reference driver voltage). Based on the analysis presented in appendix A.2, V_{pl} and $V_{GS(th)}$ can be considered as constant parameters for a given technology and t_{rc0} can be estimated by:

$$t_{rc0} = \frac{k_{MOS.tr0} \cdot A_{chip}^{k_{MOS.tr2}}}{V_{block}^{k_{MOS.tr1}}}$$

Where, $k_{MOS.tr0}, k_{MOS.tr1}, k_{MOS.tr2}$ are the meta-parameters for current rise time estimation.

The parameters related to diode reverse recovery process can be estimated by

$$I_{RR} = k_{IQt} \cdot \frac{Q_{rr}}{t_{rr}}$$

$$\frac{di_F}{dt} \approx \frac{I_{Don}}{t_{rc}}$$

$$I_{RR} = I_{RR0} \cdot \left(\frac{I_F}{I_{FREF}}\right)^{k_{MOS.IRIF}} \cdot \left(\frac{\frac{di_F}{dt}}{\left(\frac{di_F}{dt}\right)_{REF}}\right)^{k_{MOS.IRdiF}}$$

$$I_{RR} \approx I_{RR0} \cdot \left(\frac{I_{Don}}{I_{FREF}}\right)^{k_{MOS.IRIF}} \cdot \left(\frac{\frac{I_{Don}}{t_{rc}}}{\left(\frac{di_F}{dt}\right)_{REF}}\right)^{k_{MOS.IRdiF}}$$

$$t_{rr} \approx 2 \cdot \frac{I_{RR}}{\frac{di_F}{dt}} = \frac{2 \cdot I_{RR} \cdot t_{rc}}{I_{Don}}$$

$$Q_{rr} = I_{RR} \cdot \frac{t_{rr}}{k_{IQt}}$$

where I_{RR0} is the reference peak reverse-recovery current, which normally can be found in the device datasheet for reference conditions I_{FREF} (reference diode conduction current before turn-off) and $\left(\frac{di_F}{dt}\right)_{REF}$ (reference rate of change of diode current during turn-off process); and $k_{MOS.IRIF}$, $k_{MOS.IRdiF}$ are meta-parameters for the diode reverse recovery parameters which can be calculated from $I_{RR}\ vs\ I_F\ vs \frac{di_F}{dt}$ relationships normally found in the device datasheet. The parameter k_{IQt} can be calculated from reference reverse recovery values ($I_{RR0}, t_{rr0}, Q_{rr0}$) found in the device datasheet; in the literature this value is normally approximated to 2, however it has been found that k_{IQt} varies mainly with device blocking voltage for the considered reference MOSFET technology:

$$k_{IQt} = k_{MOS.IQt0} \cdot V_{block}^{k_{MOS.IQt1}} \cdot A_{chip}^{k_{MOS.IQt2}}$$

Other alternatively is to assume $\frac{di_F}{dt} \approx 2 \cdot \frac{I_{RR}}{t_{rr}}$, then

$$Q_{rr} = \frac{2}{k_{MOS.IQt}} \cdot \frac{I_{RR}^2}{\frac{di_F}{dt}} \approx \frac{2}{k_{IQt}} \cdot I_{RR0}^2 \cdot \left(\frac{I_{Don}}{I_{FREF}}\right)^{2 \cdot k_{MOS.IRIF}} \cdot \left(\frac{\frac{I_{Don}}{t_{rc}}}{\left(\frac{di_F}{dt}\right)_{REF}}\right)^{2 \cdot k_{MOS.IRdiF} - 1}$$

$$t_{rr} \approx \sqrt{\frac{2 \cdot k_{MOS.IQt} \cdot Q_{rr} \cdot t_{rc}}{I_{Don}}}$$

The R_{Gon} is limited by maximum allowed $\frac{di_F}{dt}$ for the application:

$$R_{Gon} > \frac{I_{DonMX} \cdot R_{GonREF}}{\frac{di_F}{dt} \cdot t_{rc0}} \cdot \frac{\left(-\log\left(1 - \frac{V_{pl}}{V_{DrREF}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{DrREF}}\right)\right)}{\left(-\log\left(1 - \frac{V_{pl}}{V_{Dr}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{Dr}}\right)\right)}$$

The voltage fall time at turn on (t_{fv}) can be approximated by

$$t_{fv} = V_{DD} \cdot R_{Gon} \cdot \frac{C_{rss}^*}{V_{Dr} - V_{pl}}$$

$$C_{rss}^* = \frac{C_{rss}(V_{DD}) + C_{rss}(R_{DS} \cdot I_{Don})}{2} \approx \frac{C_{rss0}}{2}$$

$$C_{rss0} = \frac{k_{cr00} \cdot A_{chip}^{k_{cr02}}}{V_{block}^{k_{cr01}}}$$

t_{fv} is limited by the maximum allowed diode voltage rate of change $\left(\frac{dv_{FMAX}}{dt}\right)$ which is a property of the MOSFET device technology:

$$\frac{V_{DD}}{t_{fv}} < \frac{dv_{FMAX}}{dt}$$

Therefore, the minimum R_{Gon} is also limited by:

$$R_{Gon} > \frac{2 \cdot (V_{Dr} - V_{pl})}{C_{rss0} \cdot \frac{dv_{FMAX}}{dt}}$$

On the other hand, no reverse recovery takes place during turn-off process, and the turn-off energy loss can be approximated by

$$E_{off} = \frac{1}{2} \cdot V_{DD} \cdot I_{Doff} \cdot (t_{fc} + t_{rv})$$

The voltage rise time at turn-off (t_{rv}) can be approximated by

$$t_{rv} = V_{DD} \cdot R_{Goff} \cdot \frac{C^*_{rss}}{V_{pl}}$$

The current falling time (t_{fc}) can be estimated by:

$$t_{fc} = \tau_{Goff} \cdot \log\left(\frac{V_{pl}}{V_{G(th)}}\right)$$

τ_{Goff} time constant for gate turn-off process, assumed proportional to gate resistance and MOSFET input capacitance, and therefore t_{fc} can be approximated by:

$$t_{fc} = t_{fc0} \cdot \frac{R_{Goff}}{R_{GoffREF}}$$

Where, t_{fc0} is the current falling time at reference total gate circuit resistance for turning on process ($R_{GoffREF}$), and it can be estimated by:

$$t_{fc0} = \frac{k_{MOS.tfc0} \cdot A_{chip}^{k_{MOS.tfc2}}}{V_{block}^{k_{MOS.tfc1}}}$$

In a half bridge topology, the negative dV/dt at turn-on process of one of the MOSFET devices will be seen as a positive dV/dt by the paired MOSFET device in the half bridge. High dV/dt across the turned-off power device will generate a displacement current through the miller capacitor ($C_{GD} = C_{rss}$), which through the gate resistor (R_{Goff}, as device is turned-off), this current will generate a voltage drop across R_{Goff} and will lift the gate voltage of the power device and if it is higher than the threshold voltage of the power device, then the parasitic turn-on happens, therefore R_{Goff} need to be limited:

$$V_G = C_{GD} \cdot R_{Goff} \cdot \frac{dV_{DS}}{dt} < V_{G(th)}$$

$$\frac{dV_{DS}}{dt} \approx \frac{V_{DD}}{t_{fv}}$$

$$R_{Goff} < \frac{V_{G(th)}}{C_{GD}} \cdot \frac{C^*_{rss}}{V_{Dr} - V_{pl}} \cdot R_{Gon}$$

$$R_{Goff} < \frac{V_{G(th)}}{V_{Dr} - V_{pl}} \cdot R_{Gon}$$

The ON and OFF gate resistors are selected as the minimum values which fulfil all previous constraints for the considered MOSFET technology.

4.6.2.3 Gate losses

The Power MOSFET gate losses (P_{QGMOSi}) are approximated by:

$$P_{QGMOSi} = Q_{GMOS} \cdot (2 \cdot V_{Dr}) \cdot f_{sw}$$

where, V_{Dr} is the gate driver voltage, and Q_{GMOS} is the total gate charge, which can be estimated by the meta-parameters $k_{MOS.QG0}$, $k_{MOS.QG1}$ and $k_{MOS.QG2}$ for the reference MOSFET technology, as following:

$$Q_{GMOS} = k_{MOS.QG0} \cdot V_{block}^{k_{MOS.QG1}} \cdot A_{chip}^{k_{MOS.QG2}}$$

4.6.3 Heatsink

Based on the wide design range of converter current/voltage ratings, different heatsink technologies have been considered to find the most cost-effective PSD design.
The required heatsink thermal resistance ($R_{th.Req}$) for each case has been introduced in section 3.5.3.2. The effective thermal resistance as function of the contact surface area with power semiconductors is modelled as follows:

$$R_{thHSe} = R_{thHS} \cdot \frac{k_{\delta A} + (1 - k_{\delta A}) \cdot \delta A_{HS}}{\delta A_{HS}}$$

$$\delta A_{HS} = \frac{2 \cdot n_{pMOS} \cdot A_{MOS.Pack}}{A_{Base.HS}}$$

where, $A_{MOS.Pack}$ is the Power MOSFET package area ($A_{MOS.Pack}$=310 cm^2 for TO-247 package), $k_{\delta A}$ is a regression coefficient found by taking available data of heatsink structures in the market. ($k_{\delta A} = 0.711$), R_{thHS} is the thermal resistance of the heatsink when the heat source is uniform distributed along the base area of the heatsink structure $A_{Base.HS}$, which is estimated to be at least the area of the PSDs in the PCB:

$$A_{Base.HS} \geq A_{PSD.P} = 2 \cdot n_{pMOS} \cdot k_{spMOS} \cdot A_{MOS.Pack}$$

Then, given $A_{Base.HS}$ and $R_{th.Req}$, the thermal resistance of the heatsink needs to be as lower as:

$$R_{thHS} = R_{th.Req} \cdot \frac{\delta A_{HS}}{k_{\delta A} + (1 - k_{\delta A}) \cdot \delta A_{HS}}$$

4.6.3.1 Natural convection Heatsink

In this case an aluminium heatsink structure is placed on top of the MOSFET devices and only natural convection applies ($R_{thHS} = R_{thN}$). Stamping and extrusion heatsink technologies have been considered. Meta-models and meta-parameters for these heatsink technologies are reported in appendix A.4.
The cost, overall volume, and weight of the heatsink are calculated as follows:

$$Cost_{HS} = Cost_{HSN} = n_{HSN} \cdot k_{HSNCost0} \cdot (A_{Basei})^{k_{HSNCostA}} \cdot (n_{HSN} \cdot R_{thN})^{k_{HSNCostR}}$$

$$Vol_{HS} = Vol_{HSN} = n_{HSN} \cdot k_{HSNVol0} \cdot (A_{Basei})^{k_{HSNVolA}} \cdot (n_{HSN} \cdot R_{thN})^{k_{HSNVolR}}$$

$$Weight_{HS} = Weight_{HSN} = \rho_{HSN} \cdot Vol_{HSN}$$

$$n_{HSN} = \begin{cases} 1 & A_{Base.HS} \leq A_{BaseiMX} \\ ceil\left\{\dfrac{A_{Base.HS}}{A_{BaseiMX}}\right\} & A_{Base.HS} > A_{BaseiMX} \end{cases}$$

$$A_{Basei} = \begin{cases} A_{Base.HS} & A_{BaseiMN} \leq A_{Base.HS} \leq A_{BaseiMX} \\ \dfrac{A_{Base.HS}}{n_{HSN}} & A_{Base.HS} > A_{BaseiMX} \\ A_{BaseiMN} & A_{Base.HS} < A_{BaseiMN} \end{cases}$$

$$A_{BaseiMN} = k_{HSNAMN} \cdot (R_{thN})^{k_{HSNAR}}$$
$$A_{BaseiMX} = k_{HSNAMX} \cdot (R_{thN})^{k_{HSNAR}}$$

It has been assumed that if the target heatsink area ($A_{Base.HS}$) is major than the maximum base area of the considered heatsinks structures ($A_{BaseiMX}$) then n_{HSN} heatsink structures with base area A_{Basei} are used and the heat is uniformly distributed between them, so the required thermal resistance per structure is $n_{HSN} \cdot R_{thN}$.
The power converter heatsink height is estimated by:

$$H_{HS.PCM} = \frac{Vol_{HSN}}{A_{Base.HS}}$$

4.6.3.2 Air Forced Heatsink

In this case an aluminium heatsink structure with fan system is placed on top of the MOSFET devices. Stamping and extrusion heatsink technologies have been considered for the aluminium structures. Square tube axial 12Vdc fans have been considered as reference fan system technology. Meta-models and meta-parameters for these technologies are reported in appendix A.4.

The cost, overall volume, and weight of the air-forced heatsink are calculated as summation of the heatsink aluminium structure and fan system components, as follows:

$$Cost_{HS} = Cost_{HSN} + Cost_{HSFan}$$

$$Vol_{HS} = Vol_{HSN} + Vol_{HSFan}$$

$$Weight_{HS} = Weight_{HSN} + Weight_{HSFan}$$

The heatsink structure is modelled as in previous section, and the fan system is evaluated by:

$$Cost_{HSFan} = Cost_{HSFan0} + k_{HSFanCost0} \cdot (A_{Fan})^{k_{HSFanCostA}} \cdot (AFR_{FanMX})^{k_{HSFanCostAFR}}$$

$$Vol_{HSFan} = k_{HSFanVol0} \cdot (A_{Fan})^{k_{HSFanVolA}} \cdot (AFR_{FanMX})^{k_{HSVolAFR}}$$

$$Weight_{HSFan} = \rho_{HSFan} \cdot (Vol_{HSFan})^{k\_HSFanWV}$$

$$A_{Fan} \approx \frac{Vol_{HSN}}{\sqrt{A_{Base.HS}}}$$
$$AFR_{FanMX} = 2 \cdot AFR_{HS}$$

A_{Fan}: Required fan area, which is the area where the air will flow through the heatsink structure. It is approximated considering a square base heatsink area ($A_{Base.HS}$)
AFR_{FanMX}: Maximum fan air flow rate, which is approximated to be twice the nominal air flow rate of the heatsink (AFR_{HS}).

The total heatsink thermal resistance can be evaluated by adding the thermal resistance of the base plate and the thermal resistance of the structure fins, which is a function of AFR_{HS}:

$$R_{thHS} = R_{thB} + \frac{R_{thN} - R_{thB}}{1 + k_{AFR} \cdot AFR_{HS}}$$
$$R_{thB} = \frac{\max\{k_{BFin} \cdot H_{HSFin},\ H_{HSBaseMN}\}}{\kappa_{AL} \cdot A_{Base.HS}}$$
$$H_{HSFin} \approx \frac{Vol_{HSN}}{A_{Base.HS}}$$

The thermal resistance of the aluminium structure (R_{thN}) is considered as free design parameter and selected to minimize the heatsink cost:

$$\min_{R_{thN}}\{Cost_{HS}\}$$
$$\left(\frac{A_{Base.HS}}{k_{HSNAMN}}\right)^{\frac{1}{k_{HSNAR}}} \leq R_{thN} \leq R_{thHS} \cdot (1 + k_{AFR} \cdot AFR_{Max})$$

The power converter heatsink height is estimated by:

$$H_{HS.PCM} = \frac{Vol_{HSN}}{A_{Base.HS}}$$

4.6.3.3 Cold plate

In this case a cold plate is placed on top of the MOSFET devices. Different cold plates technologies have been considered. Meta-models and meta-parameters for these heatsink technologies are reported in appendix A.4.
The cost, overall volume, and weight of the heatsink are calculated as follows:

$$Cost_{HS} = n_{CP} \cdot Cost_{CPi} = n_{CP} \cdot \left(Cost_{CPC0} + \frac{k_{CPC0} \cdot Vol_{CPi}^{k_{CPCV}} \cdot WFR_{CP}^{k_{CPCFR}}}{R_{thCPi}^{k_{CPCR}}} \right)$$

$$Vol_{HS} = n_{CP} \cdot Vol_{CPi} = n_{CP} \cdot A_{BCPi} \cdot t_{CP}$$

$$Weight_{HS} = n_{CP} \cdot Weight_{CPi} = n_{CP} \cdot k_{CPM0} \cdot Vol_{CPi}^{k_{CPMV}}$$

$$R_{thHS} = \frac{R_{thCPi}}{n_{CP}} = \frac{K_{CPR0}}{n_{CP} \cdot A_{BCPi}^{k_{CPRA}} \cdot t_{CP}^{k_{CPRt}} \cdot WFR_{CP}^{k_{CPRFR}}}$$

$$n_{CP} = \begin{cases} 1 & A_{Base.HS} \leq A_{BCPiMX} \\ ceil\left\{\frac{A_{Base.HS}}{A_{BCPiMX}}\right\} & A_{Base.HS} > A_{BaseiMX} \end{cases}$$

$$A_{BCPi} = \begin{cases} A_{Base.HS} & A_{BCPiMN} \leq A_{Base.HS} \leq A_{BCPiMX} \\ \frac{A_{Base.HS}}{n_{CP}} & A_{Base.HS} > A_{BCPiMX} \\ A_{BCPiMN} & A_{Base.HS} < A_{BCPiMN} \end{cases}$$

It has been assumed that if the target heatsink area ($A_{Base.HS}$) is major than the maximum cold plate area of the considered technologies (A_{BCPiMX}) then n_{CP} cold plates with base area A_{BCPi} are used and the heat is uniformly distributed between them, so the required thermal resistance per cold plate (R_{thCPi}) is $n_{CP} \cdot R_{thHS}$.

There are two degrees of freedom in the selection of the cold plate, the cold plate thickness (t_{CP}) and the water flow rate of the cold plate (WFR_{CP}), which has been approximated as function of t_{CP} based on the analysis presented in appendix A.4, then, t_{CP} is selected to minimize the heatsink cost:

$$\min_{t_{CP}}\{Cost_{HS}\}$$

$$WFR_{CP} = k_{CPFR0} \cdot t_{CP}^{k_{CPFRt}}$$

The power converter heatsink height is approximated by:

$$H_{HS.PCM} \approx t_{CP}$$

4.6.4 Driver Power supply

The total cost of driver power supply is modelled by:

$$Cost_{DPS} = 2 \cdot C4W_{DPS} \cdot P_{DPS}$$

Where, two DPSs are needed per module, one DPS for each PSD, P_{DPS} is the required DPS power (calculated as in section 3.5.3.3), and $C4W_{DPS}$ is the DPS cost per watt. A value of $C4W_{DPS}$= 6.7 EUR/W has been estimated based on a reference DPS cost of 20 Euro for a +-15VDC/3W power supply.

4.6.5 Printed Circuit Board

PCB cost is evaluated following methodology reported in [10]. The total PCB cost is evaluated by adding the power PCB cost and the control PCB cost:

$$Cost_{PCB} = Cost_{PCB.Power} + Cost_{PCB.Control}$$

$$Cost_{PCB.Power} = (k_{APCB0} + k_{APCB1} \cdot A_{PCB.Power}) \cdot (k_{dPCB0} + k_{dPCB1} \cdot d_{PCB.Power}) \cdot (k_{nPCB0} + k_{nPCB1} \cdot N_{layerPCB.Power} + k_{nPCB2} \cdot N_{layerPCB.Power}^2)$$

$$Cost_{PCB.Control} = (k_{APCB0} + k_{APCB1} \cdot A_{PCB.Control}) \cdot (k_{dPCB0} + k_{dPCB1} \cdot d_{PCB.Control}) \cdot (k_{nPCB0} + k_{nPCB1} \cdot N_{layerPCB.Control} + k_{nPCB2} \cdot N_{layerPCB.Control}^2)$$

$A_{PCB.Power}$: Area of the power PCB, which is evaluated following section 3.5.3.4
$d_{PCB.Power}$: copper thickness of the power PCB considering all PCB layers. A 105µm copper thickness for the power PCB has been considered for all the designs.
$N_{layerPCB.Power}$: number of layers of the power PCB. A 4-layer power PCB has been considered for all the designs.
$A_{PCB.Control}$: Area of the control PCB, which is evaluated following section 3.5.3.4.
$d_{PCB.Control}$: copper thickness of the control PCB considering all PCB layers. A 35µm copper thickness for the control PCB has been considered for all the designs.
$N_{layerPCB.Control}$: number of layers of the control PCB. A 2-layer power PCB has been considered for all the designs.

The considered PCB cost function parameters are reported in Table 5, which follows the reported values in [10].

Table 5 Considered PCB cost function meta-parameters

	k_{xPCB0}	k_{xPCB1}	k_{xPCB2}
A_{PCB}	0.407 €$^{1/3}$	3.240 €$^{\frac{1}{3}}/dm^2$	--
d_{PCB}	8.489 €$^{1/3}$	$67.947 \cdot 10^{-3}$ €$^{\frac{1}{3}}/\mu m$	--
$N_{layerPCB}$	$29.409 \cdot 10^{-3}$ €$^{1/3}$	$-2.779 \cdot 10^{-3}$ €$^{1/3}$	$1.829 \cdot 10^{-3}$ €$^{1/3}$

The PCB weight is approximated by:

$$Weight_{PCB} = \rho_{PCB} \cdot (A_{PCB.Power} + A_{PCB.Control}) \cdot t_{PCB}$$

t_{PCB}: PCB thickness approximated as constant for both PCBs.
ρ_{PCB}: PCB density.

The inductance of a track on a PCB can be calculated by [11]

$$L = 2 \cdot l_{track} \cdot \left(\log\left(\frac{2 \cdot l_{tack}}{w_{track} + t_{track}}\right) + 0.5 + 0.2235 \cdot \frac{w_{track} + t_{track}}{l_{track}}\right) nH$$

Where l_{track}, w_{track} and t_{track} are the length, width and thickness of the PCB track in cm.

4.6.6 Cost

The power converter module cost is calculated by

$$Cost_{PCM} = \frac{1}{1 - \Xi_{PCM}} \cdot \left(Cost_{mat,PCM} + Cost_{House,PCM} + Cost_{lab,PCM}\right)$$

Where Ξ_{PCM} is the PCM supplier gross margin, (Ξ_{PCM}=0.2 (20%) has been assumed), $Cost_{mat,PCM}$ is the total cost of power converter components, $Cost_{House,PCM}$ is the cost of converter housing, and $Cost_{lab,PCM}$ is the converter labour cost.

The Housing cost is estimated by:

$$Cost_{House,PCM} = Cost_{HouseREF} \cdot \left(\frac{Vol_{PCM}}{Vol_{PCMREF}}\right)^{\frac{2}{3}} \cdot \sqrt{\frac{Weight_{PCM}}{Weight_{PCMREF}}}$$

Where, Vol_{PCM} and $Weight_{PCM}$ are the overall volume and weight of the power converter module, respectively, and $Cost_{HouseREF}$ is the housing cost of a reference power converter module with volume Vol_{PCMREF} and weight $Weight_{PCMREF}$. The model is based on two main assumptions:

- Housing cost scales with the module size, but more precisely the housing material scales with the module outer area. Approximating the module to be a cube, then $A_{PCM} \propto (Vol_{PCM})^{\frac{2}{3}}$.
- Housing cost scales with module components weight as housing components needs to be sized to support module components without bending/deforming. Considering that the moment capacity of a metal plate is proportional to the square of its thickness and the moment applied by the module is proportional to its weight, then $\frac{Weight_{PCM}}{Weight_{PCMREF}} = \left(\frac{thickness_{House}}{thickness_{HouseREF}}\right)^2$.

The converter labour cost is estimated by

$$Cost_{lab,PCM} = \Sigma_{LabComp} \cdot (2 \cdot \boldsymbol{N_{cPSD}} \cdot n_{pMOS} + \boldsymbol{N_{cdc}} + \boldsymbol{N_{occ}})$$

Where, $\Sigma_{LabComp}$ is the labour cost per component, N_{cPSD} is the number of components per MOSFET in the PSD (N_{cPSD} =8), N_{cdc} is the number of discrete capacitors, and N_{occ} is the number of other common components including Driver Power Supply, controller, measurements & protections, heatsink, Driver circuit IC. (N_{occ}=30 has been assumed for the half bridge topology).

The converter components cost is defined by:

$$Cost_{mat,PCM} = Cost_{CDC} + Cost_{PSD} + Cost_{HS} + Cost_{DPS} + Cost_{PCB} + Cost_{OCC}$$

Where, $Cost_{CDC}$ is the DC capacitor bank cost, $Cost_{PSD}$ is the total cost of power switch devices, $Cost_{HS}$ is the converter heatsink cost, $Cost_{DPS}$ is the driver power supply cost, $Cost_{PCB}$ is the printed circuit board cost, and $Cost_{OCC}$ is the cost of other common components in the power converter (This includes the driver ICs, controller, communications elements, measurement and protection circuit components.). Significant savings can be expected if the DC-DC control and BMS functions are merged on the same physical controller.

4.6.7 Overall Volume and Mass

The overall power converter volume can be approximated by

$$Vol_{PCM} = \left(\sqrt{(A_{PCB})} + \Delta X_{PCM}\right)^2 \cdot \max(H_{HS.PCM}, H_{Cdc})$$

A_{PCB}: Total PCB area, which is evaluated following section 3.5.3.4.
ΔX_{PCM}: delta space for overall volume evaluation ($\Delta X_{PCM} = 1cm$ has been assumed)
$H_{HS.PCM}$: power converter Heatsink height
H_{Cdc}: height of the discrete capacitor in the capacitor bank.

The main converter weight is approximated by the sum of heaviest converter components:

$$Weight_{PCM} = Weight_{Cdc} + Weight_{PSD} + Weight_{HS} + Weight_{PCB} + Weight_{OCC}$$

$Weight_{Cdc}$: total weight of the capacitor bank
$Weight_{HS}$: heatsink weight
$Weight_{PSD}$: total PSD weight
$Weight_{PCB}$: PCB weight
$Weight_{OCC}$: Weight of other common components in the PCM, which approximated by:

$$Weight_{OCC} = N_{occ} \cdot Weigth_{CompAVG}$$

$Weigth_{CompAVG}$: average electronic component weight.

4.6.8 Power losses

The PCM power losses are mainly determined by the conduction and switching losses of the power MOSFETs.
All modules connected to the string are always conducting the string current, either by connecting the battery energy storage sub-module to the string or by passing it. However, only one module per string is under PWM operation, and therefore it has switching losses.

The PCM conduction losses are estimated by:

$$P_{LossPCM.Cond} = n_{pMOS} \cdot R_{DS}\left(k_{T_j} \cdot T_{jmx}\right) \cdot \left(\frac{I_{mod}}{n_{pMOS}}\right)^2$$

The MOSFET on-state resistance is evaluated for the maximum designed MOSFET junction temperature ($k_{T_j} \cdot T_{jmx}$). This approximation overestimated losses at low power operation but simplifies the MOSFET loss evaluation by neglecting the junction temperature and conduction loss interdependency from the thermal model. Furthermore, considering the string current ripple, then the conduction losses can be evaluated as:

$$P_{LossPCM.Cond} = \frac{R_{DS}\left(k_{T_j} \cdot T_{jmx}\right)}{n_{pMOS}} \cdot \left(I_{str}^2 + \left(\frac{f_{sw} \cdot (OCV_{mod}(SOC) - R_{mod}(SOC) \cdot I_{str})}{8 \cdot \sqrt{3} \cdot L_{str}} \right)^2 \right)$$

The PCM switching loss are evaluated by:

$$P_{LossPCM.SW} = 2 \cdot n_{pMOS} \cdot f_{sw} \cdot \left(E_{ON}\left(V_{mod}, \frac{I_{str}}{n_{pMOS}}\right) + E_{OFF}\left(V_{mod}, \frac{I_{str}}{n_{pMOS}}\right) + 2 \cdot V_{Dr} \cdot Q_{GMOS} \right)$$

Where E_{ON} and E_{OFF} are the non-linear functions for turn On and Off energy, respectively, defined in the section 4.6.2.2.

4.7 String DC inductors

The DC string inductor designs are evaluated following the methodology described in appendix A.3. The 4EM & 4ET iron-core smoothing reactors have been considered as reference inductor technology.

The string inductor cost is estimated based on the model proposed in [19], briefly described here for the sake of completeness:

$$Cost_{Lstr} = \frac{1}{1 - \Xi_L} \cdot \left(\text{Cost}_{mat,L} + \text{Cost}_{lab,L}\right)$$

$$\text{Cost}_{mat,L} = \sigma_{core,L} \cdot W_{cL} + \sigma_{wdg,L} \cdot W_{wdg} + Cost_{mat0,L}$$

$$\text{Cost}_{lab,L} = \sigma_{lab,L} \cdot W_{wdg} + Cost_{lab0,L}$$

Where $\sigma_{core,L}$, $\sigma_{wdg,L}$ and $\sigma_{lab,L}$ are the specific cost per weight of the core and winding, which depends on the employed core and winding type; W_{cL}, W_{wdg} are the core and winding weight, respectively, $Cost_{mat0,L}$ and $Cost_{lab0,L}$ are fixed material and labour cost, and Ξ_L is the supplier gross margin.

For the considered reference inductor technology: $\sigma_{core,L} = 8\ €/kg$, $\sigma_{wdg,L} = 10\ €/kg$, $\sigma_{lab,L} = 7€/kg$, $Cost_{mat0,L} = 1€/unit$ and $Cost_{lab0,L} = 2€/unit$. A supplier gross margin of 25% has been assumed.

Given the required string inductor nominal current ($I_{L.N}$), as specified in section 3.6, and the string inductor inductance (L_{str}), following guidelines introduced in section 2.2.6, the total string inductor weight and overall volume are estimated by:

$$Weight_{Lstr} = k_{LWt0} \cdot I_{L.N}^{k_{LWtI0}} + k_{LWt1} \cdot E_L^{k_{LWtE}} \cdot I_{L.N}^{k_{LWtI1}}$$

$$Vol_{Lstr} = k_{LVt0} \cdot I_{L.N}^{k_{LVtI0}} + k_{LVt1} \cdot E_L^{k_{LVtE}} \cdot I_{L.N}^{k_{LVtI1}}$$

$$E_L = \frac{1}{2} \cdot L_{str} \cdot I_{L.N}^2$$

The core and winding weights are estimated by:

$$W_{cL} = k_{LWc0} \cdot Weight_{Lstr}^{k_{LWcWt}}$$

$$W_{wdg} = k_{LWw0} \cdot Weight_{Lstr}^{k_{LWwWt}}$$

The inductor losses (P_{LossL}) are estimated by the summation of winding (P_{wL}) and core losses (P_{coreL}):

$$P_{wL} = ESR_L \cdot \left(I_{str}^2 + \left(1 + \frac{6 \cdot (F_{rLref} - 1)}{\pi^2} \cdot \left(\frac{f_{sw}}{f_{Lhref}} \right)^2 \right) \cdot \left(\frac{f_{sw} \cdot V_{mod}(SOC_{MMESS})}{8 \cdot \sqrt{3} \cdot L_{str}} \right)^2 \right)$$

$$ESR_L = \frac{k_{LPw0} \cdot I_{L.N}^{k_{LPwI0}-1} + k_{LPw1} \cdot E_L^{k_{LPwE}} \cdot I_{L.N}^{k_{LPwI1}-1}}{\left(1 + F_{rLref} \cdot \delta_{iLref}\right)}$$

$$P_{coreL} = \left(\frac{2 \cdot \sqrt{3} \cdot f_{sw}}{\pi \cdot f_{Lhref}} \right)^{\alpha_L} \cdot \left(\frac{\frac{f_{sw} \cdot V_{mod}(SOC_{MMESS})}{8 \cdot L_{str}}}{\sqrt{2} \cdot \delta_{iLref} \cdot I_{L.N}} \right)^{\beta_L} \cdot k_{\rho c0} \cdot (W_{cL})^{k_{\rho cWc}}$$

5 Design examples

This chapter shows some results with design examples for different core cell types. Table 6 reports the general module and string reference design constants considered within this chapter. Also, Table 7 reports the reference design constants/parameters for power converter sub-module design. All other design constants have been set as previously described in chapters 3 and 4, unless otherwise indicated. Main cost parameters are reported in Table 1, and the main battery cell properties are reported in Table 2.

Table 6 General module and string reference design constants

Parameter/constant	Value	Parameter/constant	Value
$T_{cell.max}$	35 °C	$Weight_{C4M.max}$	75 kg
T_{watmx}	25 °C	$V_{ModMN4D}$	10 V
F_{sw}	3 kHz	$V_{ModMX4D}$	150 V
k_{Ucab}	70%	$\alpha I_{Bmx.MN}$	20 %
K_{Viso}	2	$N_{\alpha IBmx}$	9
$\delta i_{LstrRMS}$	15 %	Δx_{conv}	1 cm

Table 7 Power converter sub-module - reference design constants

	Parameter/constant	Value		Parameter/constant	Value
PSD & heatsink	n_{PMOSmx}	20	**Capac. Bank**	KS_{Cdc}	1.6
	$A_{ChipMOS}$	50 mm^2		δV_{Cdc}	5%
	k_{Vblock}	0.5		L_{dBC}	300 nH
	KSF_{IMOSmx}	0.5	**PCB**	A_{PCB0}	100 cm^2
	k_{Tjmx}	0.7143		$N_{layerPCBP}$	4
	V_{Dr}	15		d_{cuPCBP}	105µm
	T_{airmx}	30 °C		$N_{layerPCBC}$	2
	T_{ambmx}	40 °C		d_{cuPCBC}	35µm
	KSF_{RgON}	2		ρ_{PCB}	2700 kg/m^3
	$\left(\frac{di_F}{dt}\right)_{Max}$	800 A/µs		t_{PCB}	2.36mm
	$Cost_{PSD0}$	0.3 EUR	**Housing**	$\rho_{ConvHousing}$	3000 kg/m^3
	$N_{CompPSD}$	8		$Cost_{HousingREF}$	50 EUR
Other	$Cost_{OCCPC}$	60 EUR		$Vol_{HousingREF}$	4.7 dm^3
	$C4C_{ConvLab}$	50/60		$Weight_{HousingREF}$	1.3 kg
	$N_{CompOCC}$	30		$t_{HousingREF}$	2.49mm
	Ξ_{PCM}	0.2		$Weight_{comp}$	6 g

5.1 Module design

There are three global free design parameters that directly set the module design within the MM-ESS design algorithm: the number of series (n_{sCell}) and parallel (n_{pCell}) connected cells per module and the maximum battery cell utilization ratio αI_{Bmx}, as previously defined in section 3.3. This section explores how these three free design parameters affect the cost, weight, volume, and nominal losses at module level, it means without a specific MM-ESS target defined (total system energy, power, and voltage) but just the module relative performance is analysed.

5.1.1 Module Cost

First, the influence of the free design parameters on the relative module cost is analysed for different core cells. The module cost per unit energy (CpE) and the module cost per unit power (CpP) are considered. The reference module power is taken as the product between the average module voltage and the maximum continuous discharge current of the module.

Figure 5-1, Figure 5-2, Figure 5-3, and Figure 5-4 show the module cost versus the main free design parameters for the prismatic core battery cells NMC 94Ah from Samsung-SDI, NMC 155Ah from REPT, LTO 23Ah from Toshiba-SCiB, and LFP 302Ah from CATL, respectively. The main properties of these battery cells are reported in Table 2.

Table 8 shows the module designs with minimum relative module cost for different core cells. Three designs per core cell are reported in Table 8, which correspond to three design targets: to minimize CpE, to minimize CpP and to minimize $C^2EP = CpE \cdot CpP$.

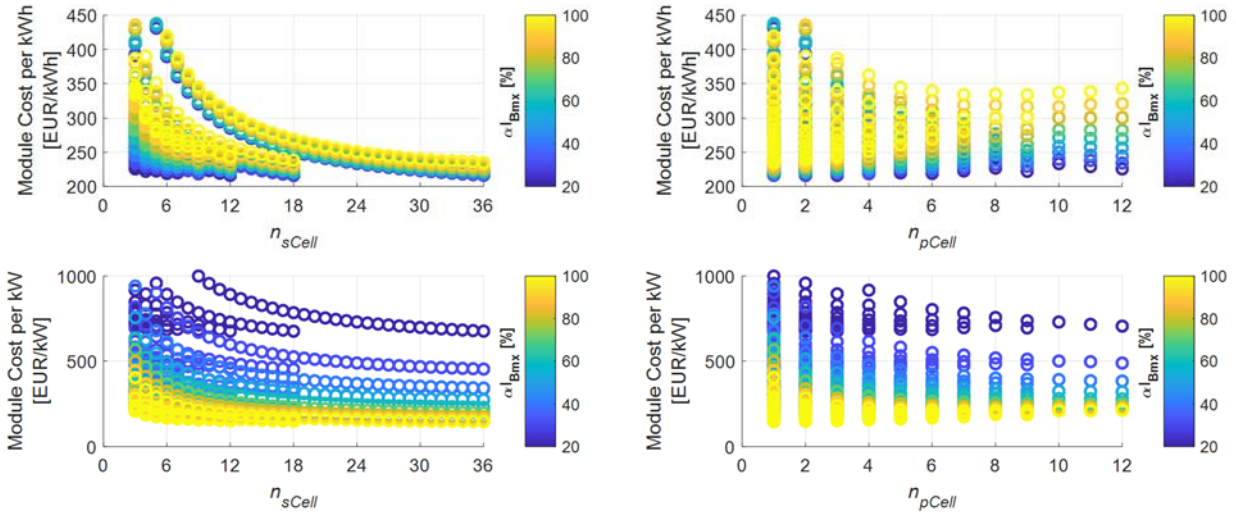


Figure 5-1 Module Cost versus main free design parameters for core battery cell prismatic NMC 94Ah from Samsung-SDI. Top: Module cost per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module cost per unit Power versus n_{sCell} (left) and n_{pCell} (right). The colour mark represents the cell derating (αI_{Bmx}) for each module design.

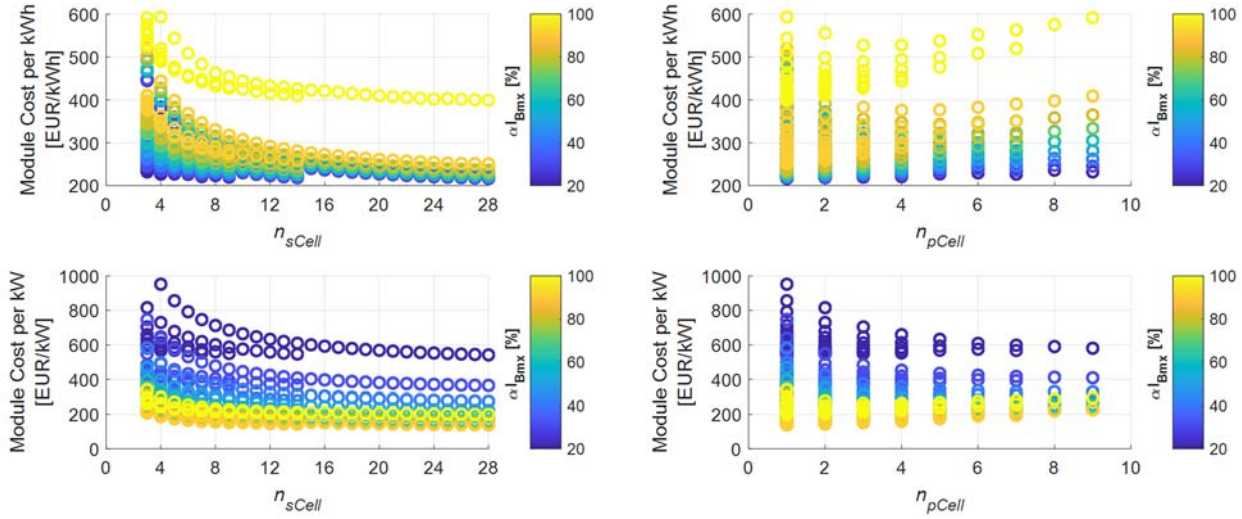


Figure 5-2 Module Cost versus main free design parameters for core battery cell prismatic NMC 155Ah from REPT. Top: Module cost per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module cost per unit Power versus n_{sCell} (left) and n_{pCell} (right). The colour mark represents the cell derating (αI_{Bmx}) for each module design.

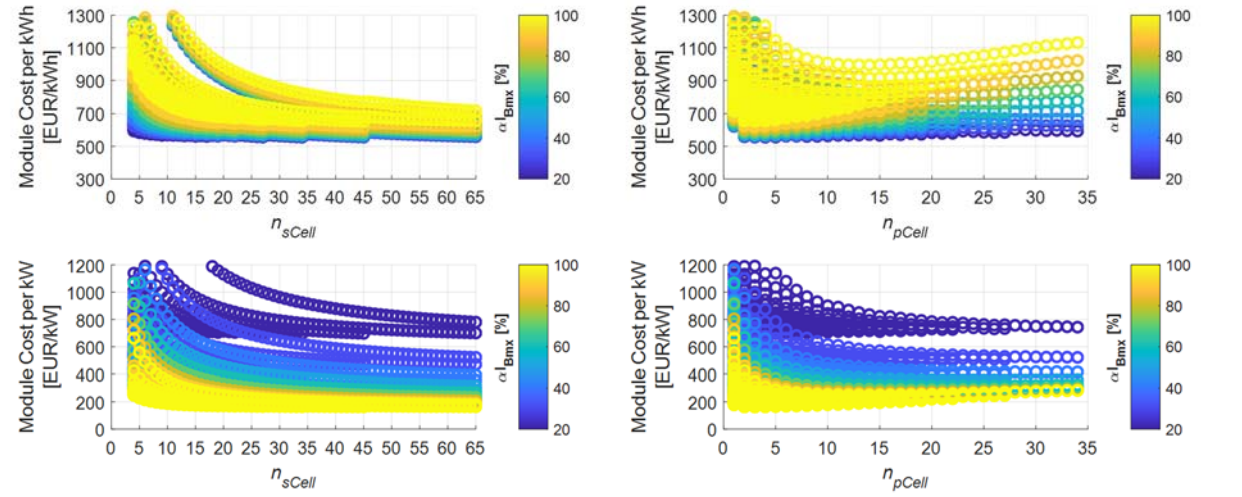


Figure 5-3 Module Cost versus main free design parameters for core battery cell prismatic LTO 23Ah from Toshiba-SCiB. Top: Module cost per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module cost per unit Power versus n_{sCell} (left) and n_{pCell} (right). The colour mark represents the cell derating (αI_{Bmx}) for each module design.

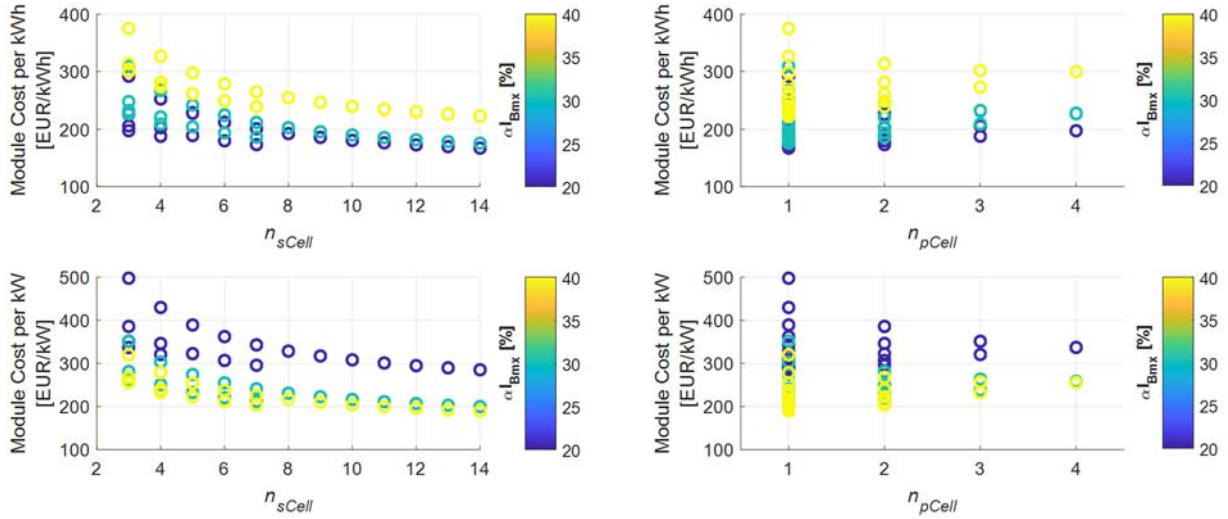


Figure 5-4 Module Cost versus main free design parameters for core battery cell prismatic LFP 302Ah from CATL. Top: Module cost per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module cost per unit Power versus n_{sCell} (left) and n_{pCell} (right). The colour mark represents the cell derating (αI_{Bmx}) for each module design.

Table 8 Module designs with minimum relative module cost for different core cells

Core Cell	NMC 94Ah @Samsung-SDI			NMC 155Ah @REPT			LTO 23Ah @Toshiba-SCiB			LFP 302Ah @CATL		
Optimization Target	CpE	CpP	C²EP	CpE	CpP	C²EP	CpE	CpP	C²EP	CpE	CpP	C²EP
n_{sCell}	18	36	36	28	28	28	34	45	45	14	14	14
n_{pCell}	2	1	1	1	1	1	4	3	3	1	1	1
αI_{Bmx} [%]	20	100	100	20	90	80	20	100	90	20	40	30
$V_{mod.AVG}$ [V]	66	132	132	102	102	102	78	104	104	45	45	45
$I_{mod.MCD}$ [A]	60	150	150	62	279	248	74	276	248	181	362	271
$P_{mod.nom}$[kW]	4.0	20.0	20.0	6.3	28.5	25.3	5.8	28.6	25.7	8.2	16.3	12.3
E_{mod} [kWh]	12.4	12.4	12.4	15.8	15.8	15.8	7.2	7.16	7.16	13.9	13.9	13.9
$\frac{Cost_{mod}}{E_{mod}}\left[\frac{EUR}{kWh}\right]$	216	235	235	217	251	236	556	653	618	167	222	176
$\frac{Cost_{mod}}{P_{mod.nom}}\left[\frac{EUR}{kW}\right]$	676	147	147	542	139	148	697	164	172	285	190	200
$\frac{Vol_{mod}}{E_{mod}}\left[\frac{dm^3}{kWh}\right]$	4.7	5.2	5.2	4.4	5.5	4.9	8.9	13.2	11.4	4.3	7.3	4.6
$\frac{Weight_{mod}}{E_{mod}}\left[\frac{kg}{kWh}\right]$	7.8	8.5	8.5	7.8	8.6	8.1	13.3	18.1	15.7	7.7	12.2	8.0
$P_{loss.MCD}$[%]	1.33	5.23	5.23	2.39	6.24	5.95	1.87	6.22	5.98	3.24	5.90	4.57

5.1.2 Module Volume

Figure 5-5, Figure 5-6, Figure 5-7, and Figure 5-8 show the module volume versus the main free design parameters for the prismatic core battery cells NMC 94Ah from Samsung-SDI, NMC 155Ah from REPT, LTO 23Ah from Toshiba-SCiB, and LFP 302Ah from CATL, respectively.

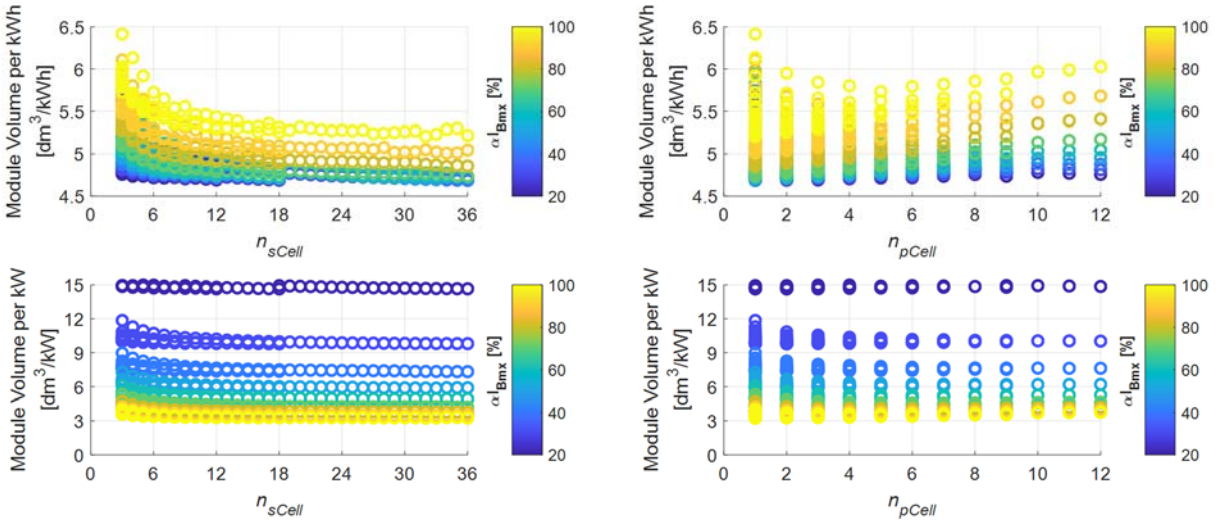


Figure 5-5 Module volume versus main free design parameters for core battery cell prismatic NMC 94Ah from Samsung-SDI. Top: Module volume per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module volume per unit Power versus n_{sCell} (left) and n_{pCell} (right).

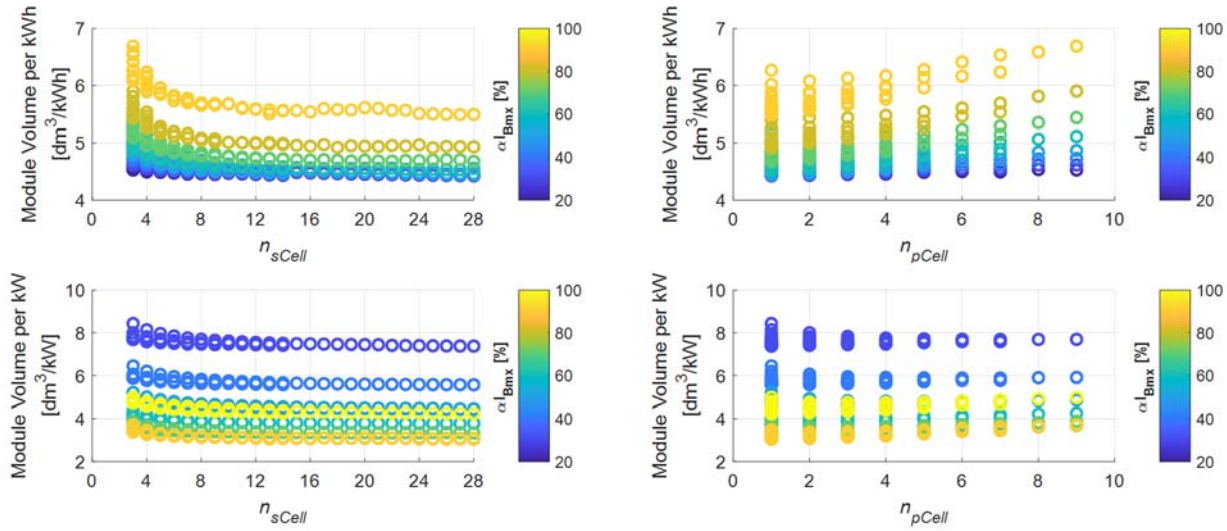


Figure 5-6 Module volume versus main free design parameters for core battery cell prismatic NMC 155Ah from REPT. Top: Module volume per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module volume per unit Power versus n_{sCell} (left) and n_{pCell} (right).

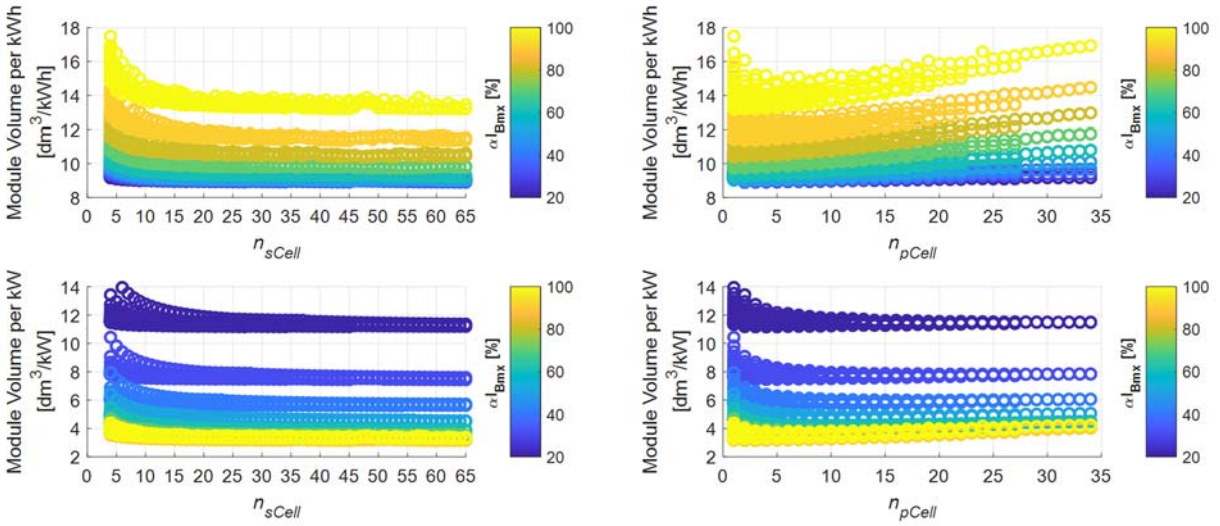


Figure 5-7 Module volume versus main free design parameters for core battery cell prismatic LTO 23Ah from Toshiba-SCiB. Top: Module volume per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module volume per unit Power versus n_{sCell} (left) and n_{pCell} (right).

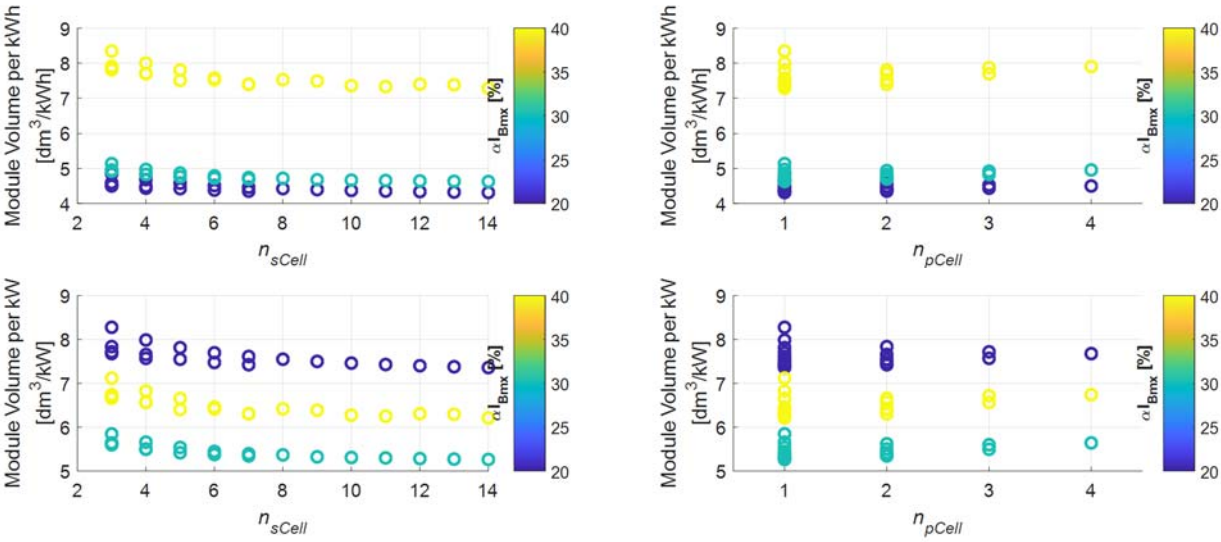


Figure 5-8 Module volume versus main free design parameters for core battery cell prismatic LFP 302Ah from CATL. Top: Module volume per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module volume per unit Power versus n_{sCell} (left) and n_{pCell} (right).

5.1.3 Module Weight

Figure 5-9, Figure 5-10, Figure 5-11, and Figure 5-12 show the module weight versus the main free design parameters for the prismatic core battery cells NMC 94Ah from Samsung-SDI, NMC 155Ah from REPT, LTO 23Ah from Toshiba-SCiB, and LFP 302Ah from CATL, respectively.

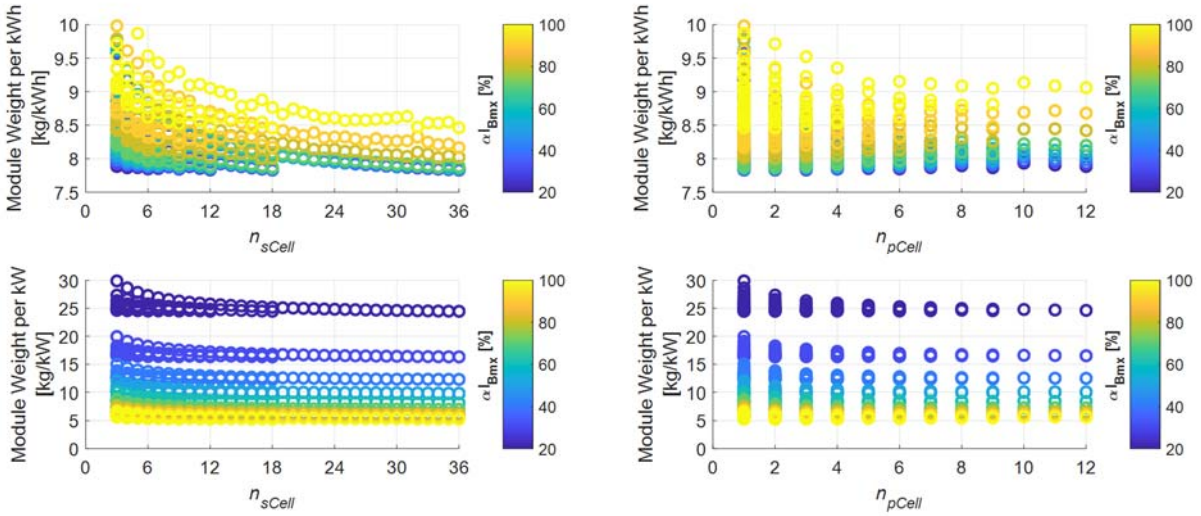


Figure 5-9 Module weight versus main free design parameters for core battery cell prismatic NMC 94Ah from Samsung-SDI. Top: Module weight per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module weight per unit Power versus n_{sCell} (left) and n_{pCell} (right).

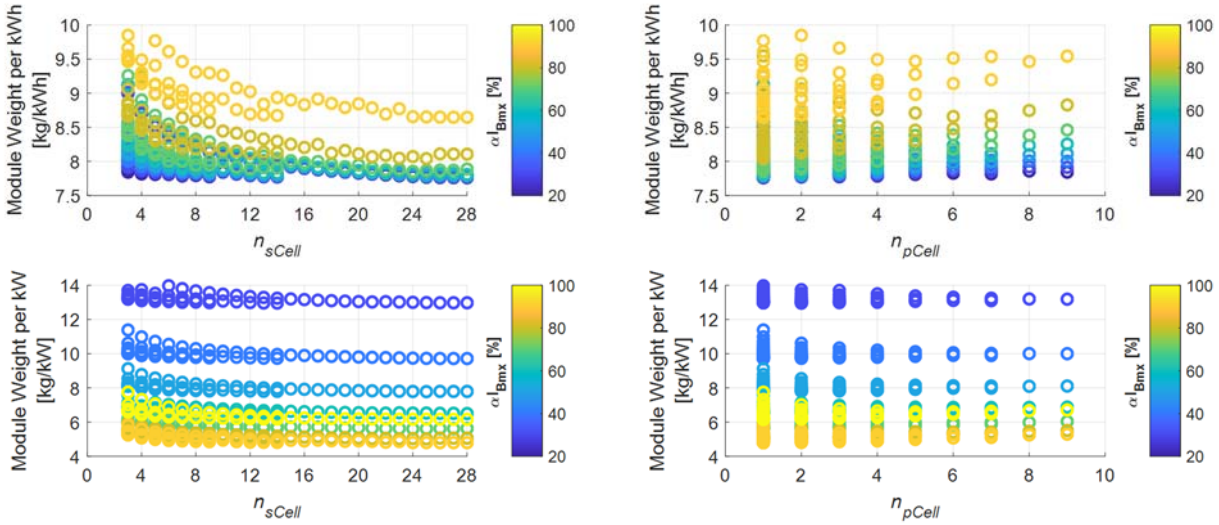


Figure 5-10 Module weight versus main free design parameters for core battery cell prismatic NMC 155Ah from REPT. Top: Module weight per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module weight per unit Power versus n_{sCell} (left) and n_{pCell} (right).

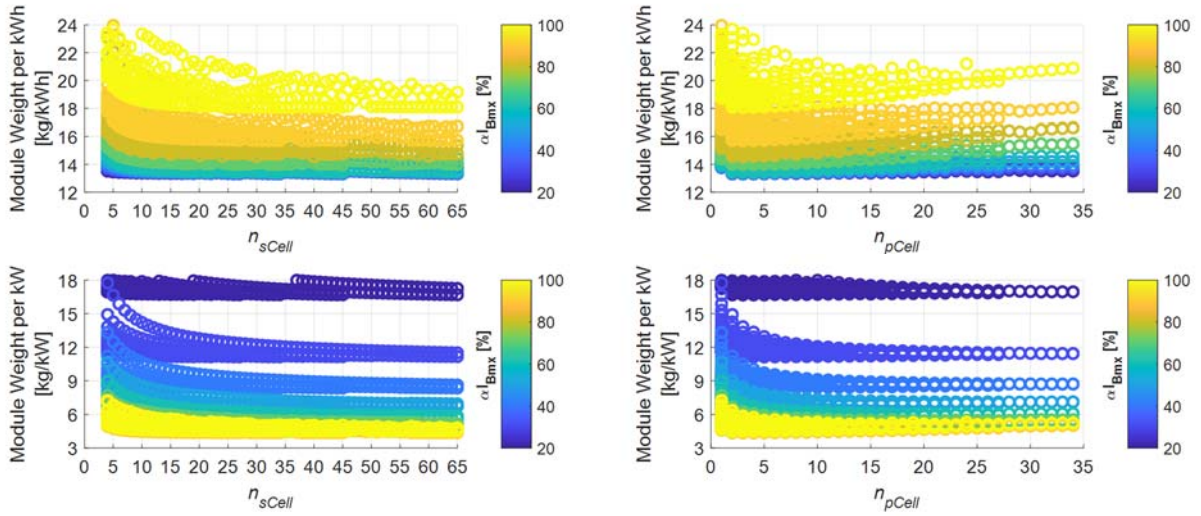


Figure 5-11 Module weight versus main free design parameters for core battery cell prismatic LTO 23Ah from Toshiba-SCiB. Top: Module weight per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module weight per unit Power versus n_{sCell} (left) and n_{pCell} (right).

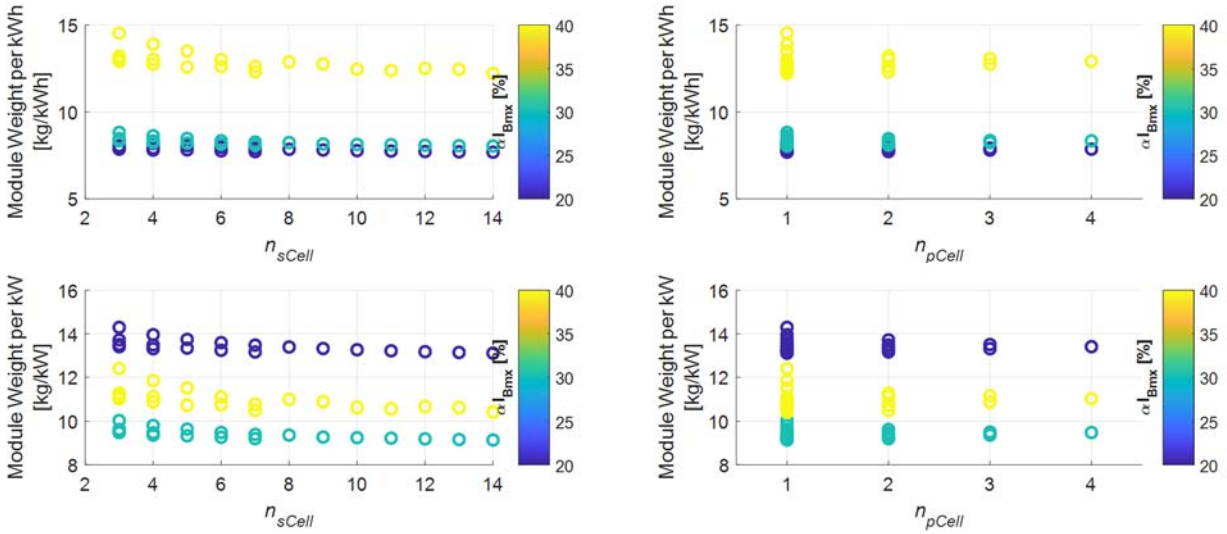


Figure 5-12 Module weight versus main free design parameters for core battery cell prismatic LFP 302Ah from CATL. Top: Module weight per unit Energy versus n_{sCell} (left) and n_{pCell} (right). Bottom: Module weight per unit Power versus n_{sCell} (left) and n_{pCell} (right).

5.1.4 Module nominal losses

Figure 5-13, Figure 5-14, Figure 5-15, and Figure 5-16 show the module nominal power losses versus the main free design parameters for the prismatic core battery cells NMC 94Ah from Samsung-SDI, NMC 155Ah from REPT, LTO 23Ah from Toshiba-SCiB, and LFP 302Ah from CATL, respectively.

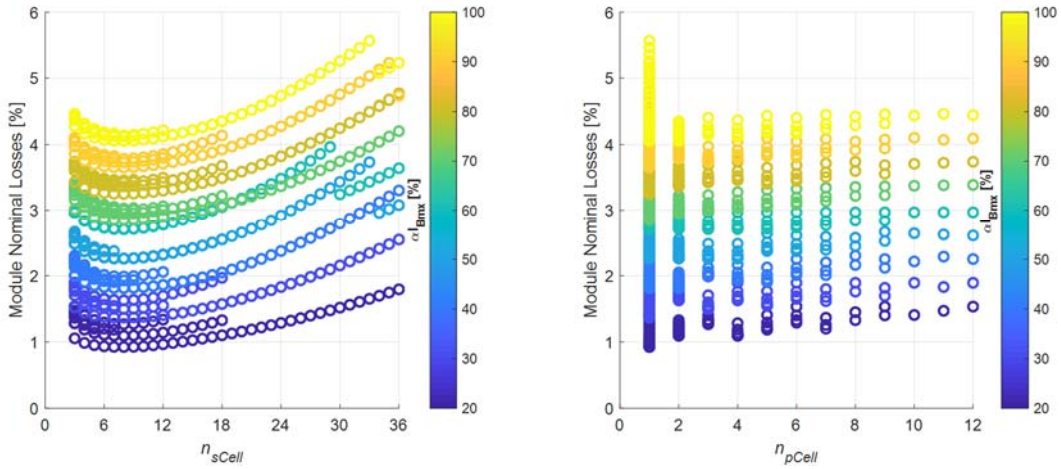


Figure 5-13 Module nominal losses versus n_{sCell} (left) and n_{pCell} (right) for core battery cell prismatic NMC 94Ah from Samsung-SDI.

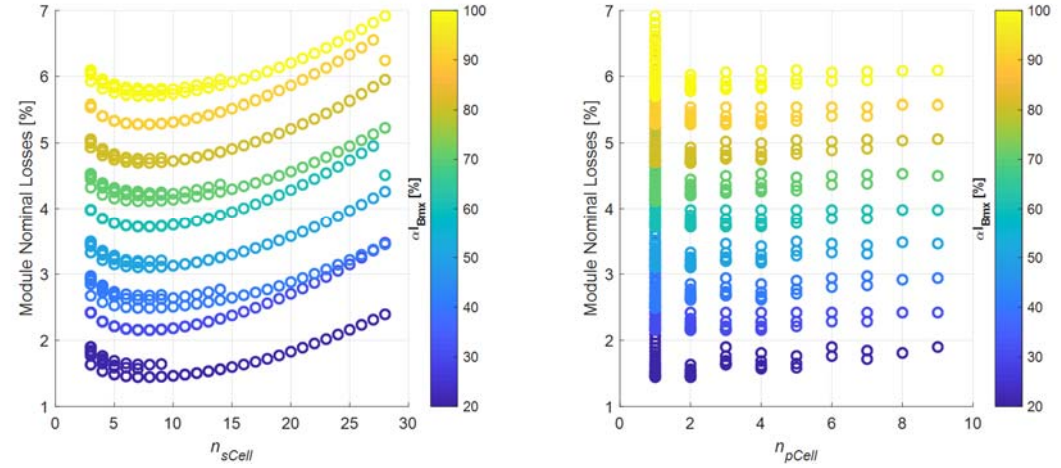


Figure 5-14 Module nominal losses versus n_{sCell} (left) and n_{pCell} (right) for core battery cell prismatic NMC 155Ah from REPT.

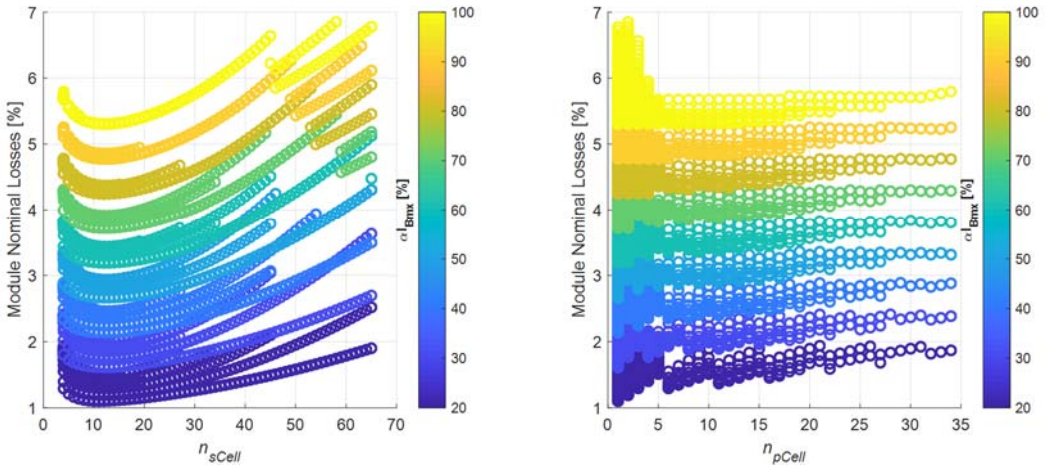


Figure 5-15 Module nominal losses versus n_{sCell} (left) and n_{pCell} (right) for core battery cell prismatic LTO 23Ah from Toshiba-SCiB.

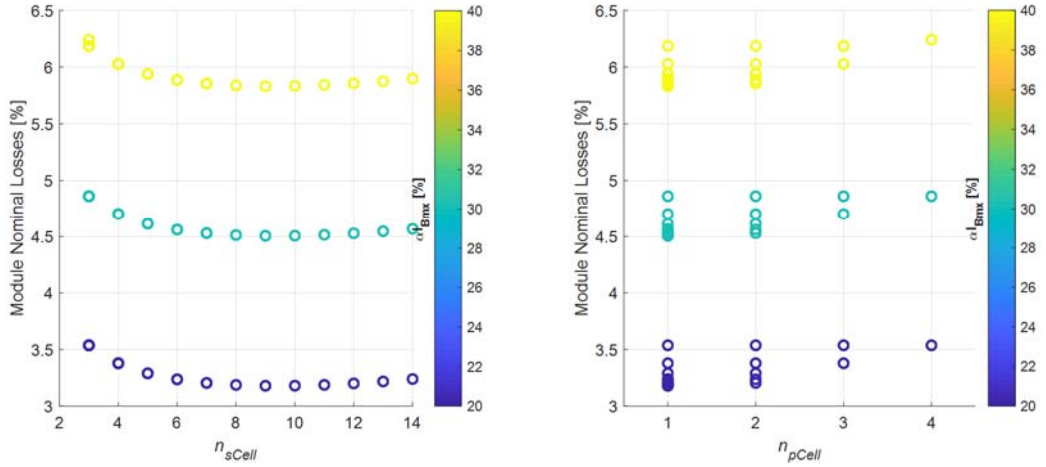


Figure 5-16 Module nominal losses versus n_{sCell} (left) and n_{pCell} (right) for core battery cell prismatic LFP 302Ah from CATL.

5.1.5 Module performance trade-off

Figure 5-17, Figure 5-18, Figure 5-19, and Figure 5-20 show the module performance space trade-off for the prismatic core battery cells NMC 94Ah from Samsung-SDI, NMC 155Ah from REPT, LTO 23Ah from Toshiba-SCiB, and LFP 302Ah from CATL, respectively.

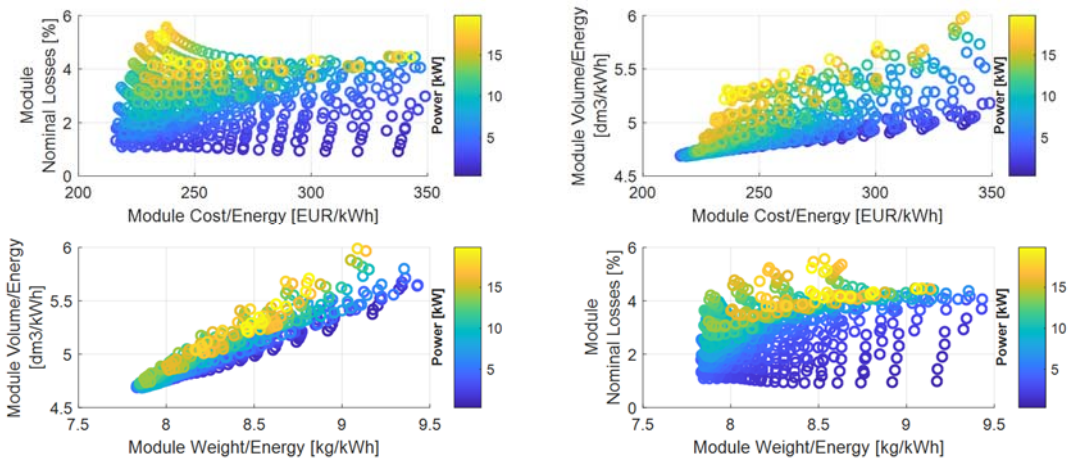


Figure 5-17 Module performance space trade-off for core battery cell prismatic NMC 94Ah from Samsung-SDI.

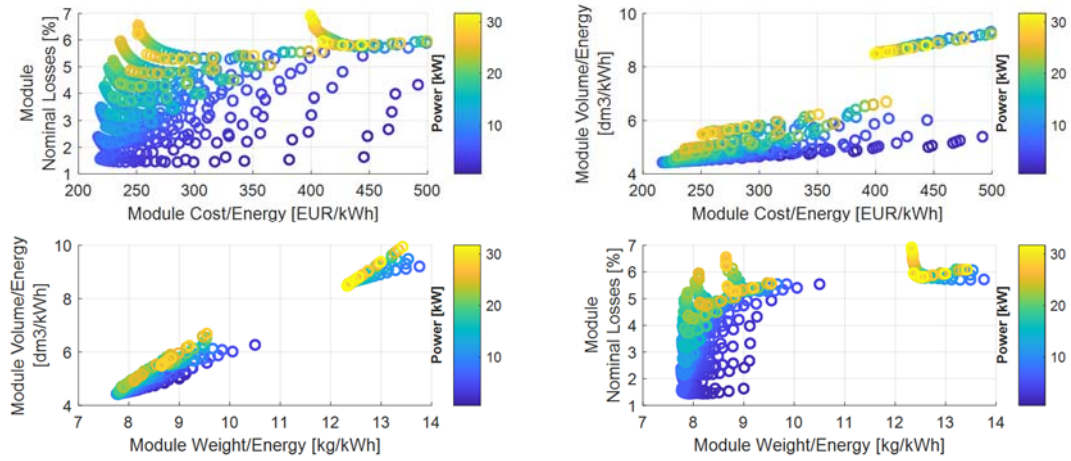


Figure 5-18 Module performance space trade-off for core battery cell prismatic NMC 155Ah from REPT.

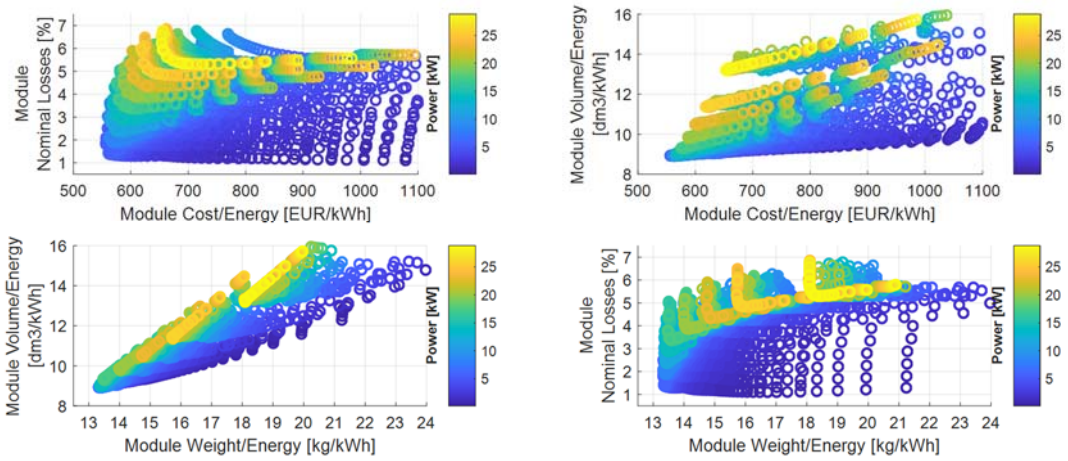


Figure 5-19 Module performance space trade-off for core battery cell prismatic LTO 23Ah from Toshiba-SCiB.

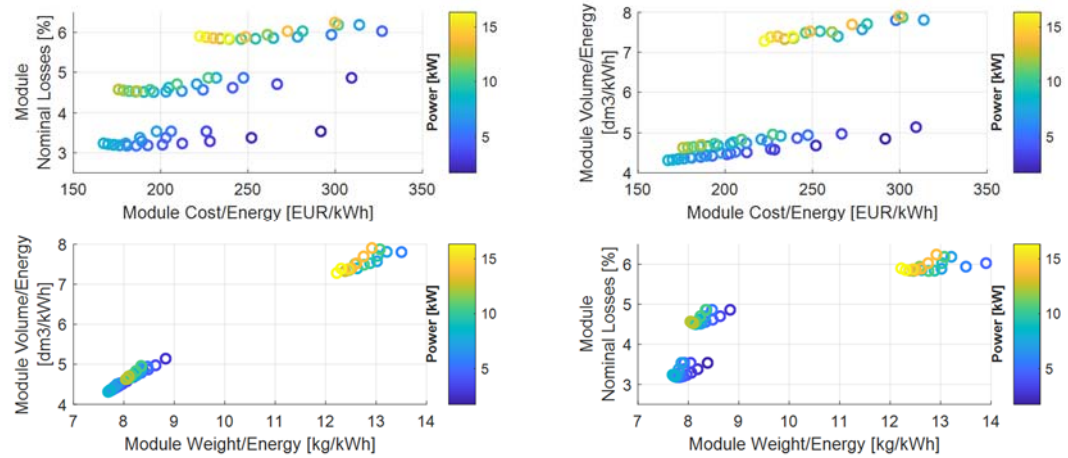


Figure 5-20 Module performance space trade-off for core battery cell prismatic LFP 302Ah from CATL.

5.2 String design

The string design is linked to a specific string voltage and consequently, one additional free design parameter (respect to the module design) needs to be considered, the number of modules per string (or the number of redundant modules per string). A string voltage of 1000 Vdc is considered in this section for the shown design examples.

Figure 5-21 shows the string performance space per unit energy trade-off for 1000V string voltage and core battery cell prismatic NMC 94Ah from Samsung-SDI. The colour mark represents the maximum continuous discharge power for each string design.

Figure 5-22 shows the string performance space per unit power (MCD) trade-off for 1000V string voltage and core battery cell prismatic NMC 94Ah from Samsung-SDI. In this case, the colour mark represents the installed energy capacity for each string design.

Figure 5-21 and Figure 5-22 also show three string designs, which correspond to three design targets: to minimize CpE, to minimize CpP and to minimize $C^2EP = CpE \cdot CpP$.

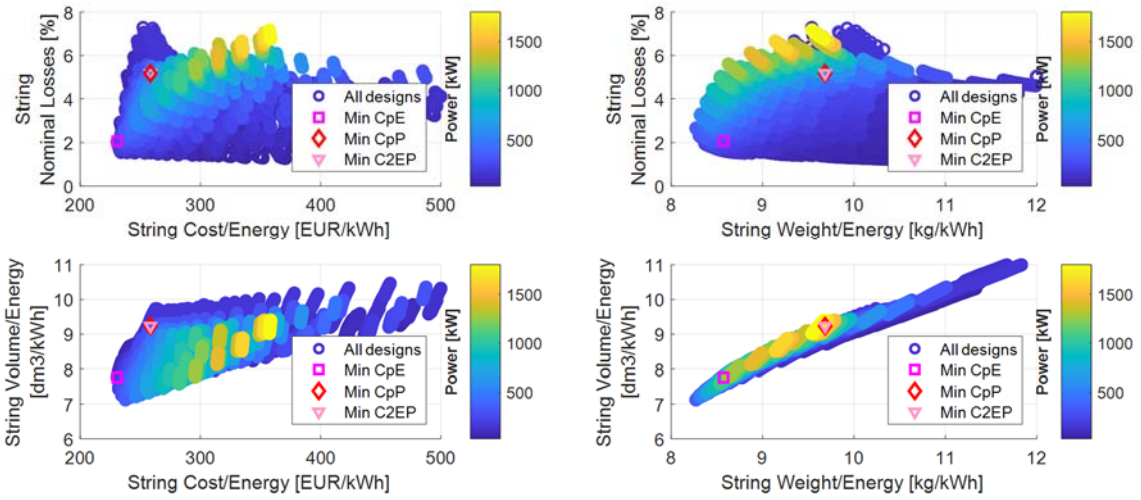


Figure 5-21 String performance space per unit energy trade-off for 1000V string voltage and core battery cell prismatic NMC 94Ah from Samsung-SDI. The colour mark represents the maximum continuous discharge power for each string design.

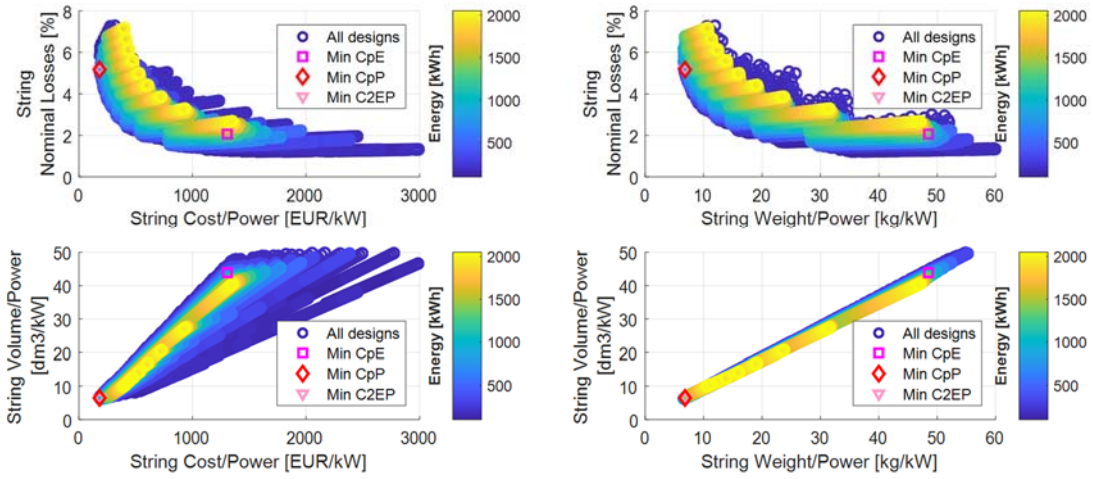


Figure 5-22 String performance space per unit power trade-off for 1000V string voltage and core battery cell prismatic NMC 94Ah from Samsung-SDI. The colour mark represents the installed energy capacity for each string design

Figure 5-23 shows the string cost, installed energy and maximum continuous discharge power trade-off for 1000V string voltage and core battery cell prismatic NMC 94Ah from Samsung-SDI. Figure 5-23 (left side) shows the string cost per unit energy versus string cost per unit power trade-off with the colour marks showing the installed string energy for each string design.
Figure 5-23 (right side) shows the string installed energy versus string max. continuous discharge power for all possible single string designs, and with the colour marks showing the string cost per unit energy for each design.

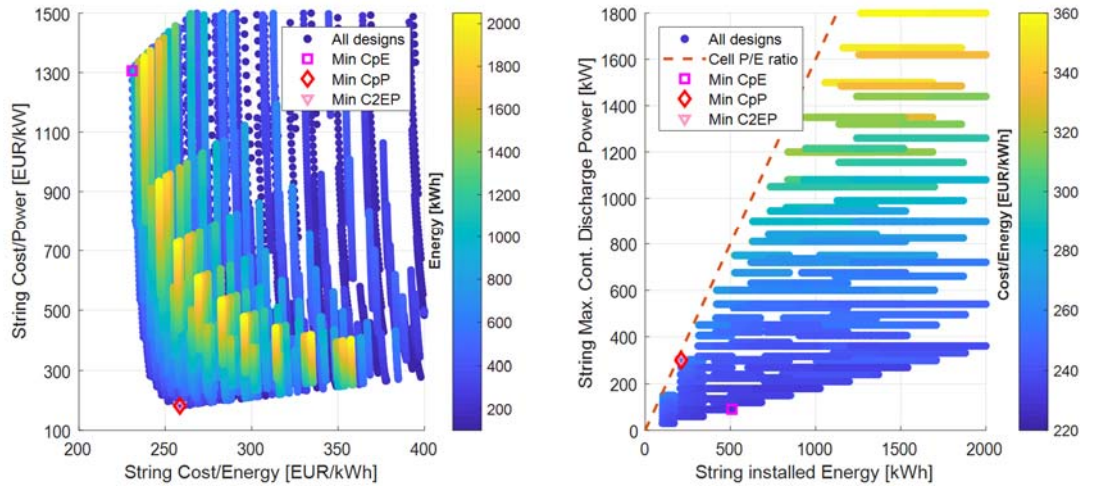


Figure 5-23 String Cost, Energy and Power trade-off for 1000V string voltage and core battery cell prismatic NMC 94Ah from Samsung-SDI. Left side: String cost per unit Energy versus string cost per unit power versus installed string energy. Right side: String installed energy versus string max. continuous discharge power versus string cost per unit energy

Table 9 shows the string designs with minimum relative string cost for 1000V string voltage and different core cells. Three designs per core cell are reported in Table 9, which correspond to three design targets: to minimize CpE, to minimize CpP and to minimize $C^2EP = CpE \cdot CpP$.

Table 9 String designs with minimum relative string cost for 1000V string voltage and different core cells

Core Cell	NMC 94Ah @Samsung-SDI			NMC 155Ah @REPT			LTO 23Ah @Toshiba-SCiB			LFP 302Ah @CATL		
Optimization Target	CpE	CpP	C^2EP	CpE	CpP	C^2EP	CpE	CpP	C^2EP	CpE	CpP	C^2EP
N_{mod}	41	17	17	34	11	11	29	12	15	42	24	24
N_{Redmod}	16	0	0	13	0	0	11	0	0	19	0	0
n_{sCell}	12	18	18	14	28	28	27	42	34	14	14	14
n_{pCell}	3	2	2	2	1	1	5	3	4	1	1	1
αI_{Bmx} [%]	20	100	100	20	90	80	20	100	90	20	40	30
$V_{mod.AVG}$ [V]	44	66	66	51	102	102	62	97	98	45	45	45
$I_{mod.MCD}$ [A]	90	300	300	124	279	248	92	276	331	181	362	271
$P_{str.MCD}$[kW]	90	300	300	124	279	248	92	276	331	181	362	271
E_{String} [kWh]	509	211	211	538	174	174	207	80	108	585	334	334
$\frac{Cost_{String}}{E_{String}}\left[\frac{\text{EUR}}{\text{kWh}}\right]$	231	258	258	232	273	257	586	705	663	180	244	192
$\frac{Cost_{String}}{P_{Str.MCD}}\left[\frac{\text{EUR}}{\text{kW}}\right]$	1306	182	182	1008	170	180	1322	205	216	583	225	236
$\frac{Vol_{String}}{E_{String}}\left[\frac{\text{dm}^3}{\text{kWh}}\right]$	7.76	9.23	9.23	7.33	9.76	8.83	15.0	23.3	19.9	7.11	12.1	7.92
$\frac{Weight_{Str}}{E_{String}}\left[\frac{\text{kg}}{\text{kWh}}\right]$	8.57	9.68	9.68	8.47	10.1	9.42	14.9	21.3	18.3	8.35	13.4	8.95
$P_{loss.MCD}$[%]	2.06	5.17	5.17	2.35	7.26	6.95	2.74	7.25	6.39	4.09	6.67	5.22

5.3 MM-ESS design

Finally, the results for a full battery system design example are presented in this section. The target is a battery system to be connected to a strong DC grid with 1000Vdc nominal voltage, 1% maximum peak voltage ripple, with at least 500kWh installed energy capacity, and a power capability of at least 500kW/250kW maximum continuous discharge/charge power.

Figure 5-24 shows the MM-ESS performance space trade-off for a target 1000V battery system with at least 500kWh installed capacity, 500kW/250kW continuous discharge/charge power and the prismatic NMC 94Ah from Samsung-SDI as core battery cell. The MM-ESS designs with the global minimum cost, minimum volume and minimum nominal losses are highlighted in Figure 5-24.

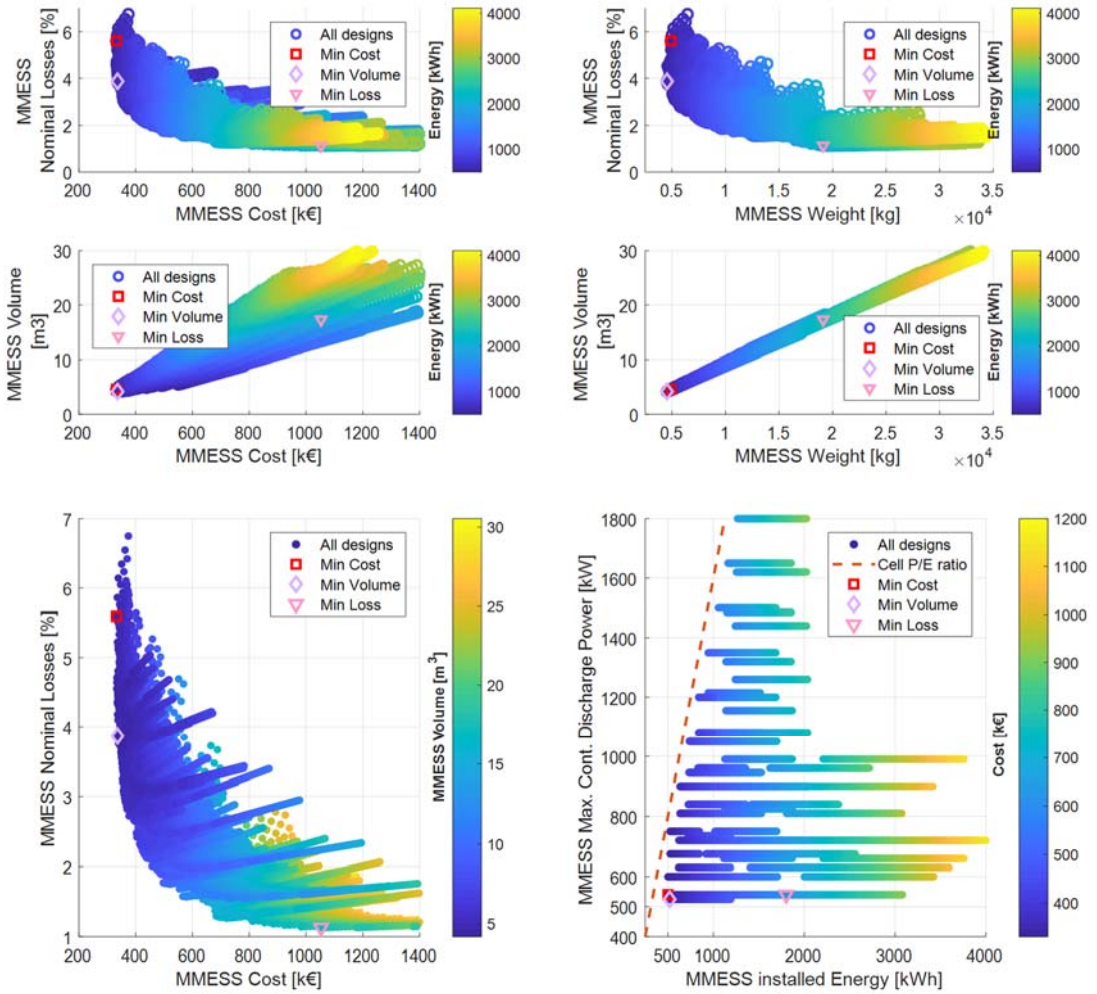


Figure 5-24 MM-ESS performance space trade-off for a target 1000V battery system with at least 500kWh installed capacity, 500kW/250kW continuous discharge/charge power and core battery cell prismatic NMC 94Ah from Samsung-SDI.

Figure 5-25 shows the MM-ESS design performance (Cost, Volume and Nominal Losses) versus the free design parameters for the considered target battery system and using the prismatic NMC 94Ah from Samsung-SDI as core battery cell. The MM-ESS designs with the global and relative minimum cost, minimum volume and minimum nominal losses are highlighted in Figure 5-25.

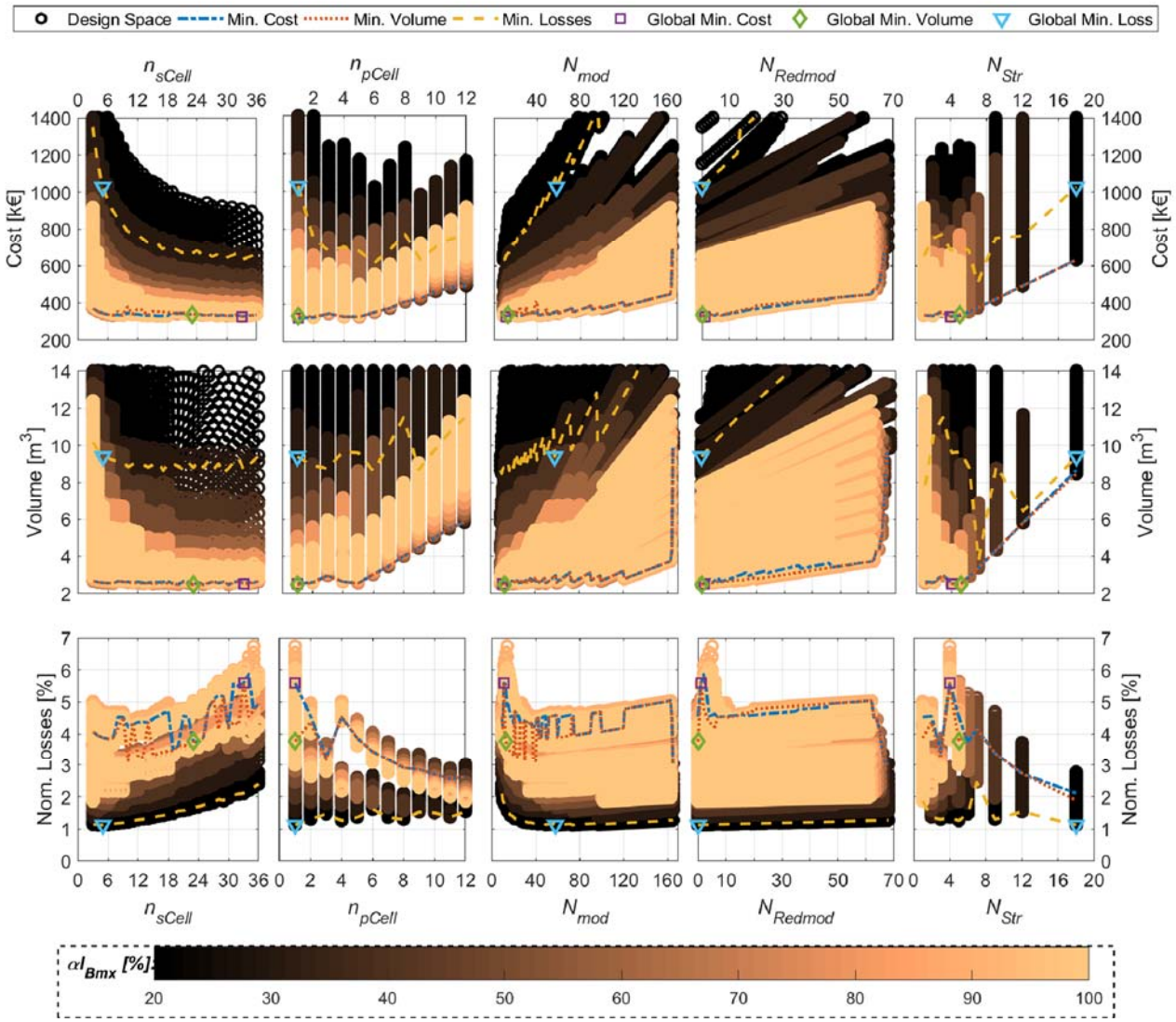


Figure 5-25 MM-ESS design performance (Cost, Volume and Nominal Losses) versus free design parameters for a target 1000V battery system with at least 500kWh installed capacity, 500kW/250kW continuous discharge/charge power and core battery cell prismatic NMC 94Ah from Samsung-SDI.

Table 10 shows the MM-ESS designs for different design targets (minimum total cost, volume, and nominal losses), considering different core cells and targeting a 1000V battery system with at least 500kWh installed capacity, and at least 500kW/250kW maximum continuous discharge/charge power.

Table 10 MM-ESS designs for different design targets (minimum total cost, volume, and nominal losses), considering different core cells and targeting a 1000V battery system with at least 500kWh installed capacity, 500kW/250kW continuous discharge/charge power.

Core Cell	NMC 94Ah @Samsung-SDI			NMC 155Ah @REPT			LTO 23Ah @Toshiba-SCiB			LFP 302Ah @CATL		
Optimization Target	Cost	Vol.	Loss	Cost	Vol.	Loss	Cost	Vol.	Loss	Cost	Vol.	Loss
N_{String}	4	1	18	3	1	2	5	1	2	2	1	2
N_{mod}	11	43	58	11	43	98	14	71	72	24	47	46
N_{Redmod}	1	0	0	0	0	0	3	2	0	0	0	0
n_{sCell}	33	7	5	28	7	3	45	7	7	14	7	7
n_{pCell}	1	5	1	1	3	8	3	19	18	1	2	2
αI_{Bmx} [%]	90	70	20	60	60	20	40	30	100	30	30	20
$V_{mod.AVG}$ [V]	121	26	18	102	25.6	11	104	16	16	45	23	23
$I_{mod.MCD}$ [A]	135	525	30	186	558	496	110	524	1656	272	544	362
E_{MMESS} [kWh]	500	519	1800	523	511	2661	501	500	962	669	655	1282
$P_{MMESS.MCD}$[kW]	540	525	540	558	558	992	552	524	3312	544	544	725
$P_{MMESS.MCC}$[kW]	259	252	259	335	334	595	552	524	3312	362	362	483
$Cost_{MMESS}$[k€]	**332**	336	1053	**332**	339	864	505	511	1038	**332**	335	443
$Vol_{MMESS}[m^3]$	4.59	4.19	17.3	4.28	3.97	18.7	7.98	7.25	21.9	5.30	5.03	9.15
$Weight_{MMESS}[t]$	4.90	4.54	19.1	4.73	4.44	22.2	7.83	7.29	19.8	5.99	5.74	10.7
$P_{loss.MCD}$[%]*	5.59	3.86	1.13	4.80	4.23	1.36	3.72	2.89	1.15	4.81	5.04	2.70

*Nominal losses evaluated at 500kW discharge power

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APPENDICES

A Component Models and Meta-parameters

A.1 DC capacitors

Following the reasoning developed in [1], the main parameters of a given DC capacitor can be estimated based on its capacitance (C_{DC}) and nominal/maximum voltage (V_{Cdc}). Figure A- 1 shows the reference parameter data for the considered DC capacitor technology, MKP DC snubber capacitors series B32665x from EPCOS-TDK Electronics, as function of the capacitance and for different nominal capacitor voltages, along with the fitted considered meta-models.

The capacitor overall volume (Vol_{Cap}) can be estimated by:

$$Vol_{Cap} = k_{Cvol0} \cdot C_{DC}^{k_{CvolC}} \cdot V_{Cdc}^{k_{CvolV}}$$

Where, k_{Cvol0}, k_{CvolC}, k_{CvolV} are the capacitor meta-parameters for volume estimation of the considered capacitor technology.

The capacitor height (H_{Cap}) is approximated by

$$H_{Cap} = k_{Ch0} \cdot C_{DC}^{k_{ChC}} \cdot V_{Cdc}^{k_{ChV}}$$

Where, k_{Ch0}, k_{ChC}, k_{ChV} are the capacitor meta-parameters for height estimation of the considered capacitor technology. Then, the capacitor area (A_{Cap}) can be calculated as

$$A_{Cap} = \frac{Vol_{Cap}}{H_{Cap}}$$

The capacitor overall weight ($Weight_{Cap}$) is estimated as functions of its volume by

$$Weight_{Cap} = k_{Cp0} \cdot (Vol_{Cdc})^{k_{CpVol}}$$

Where, k_{Cp0}, k_{CpVol}, capacitor meta-parameters for weight estimation of the considered capacitor technology.

The maximum allowed dV/dt for a discrete capacitor within a selected capacitor technology is approximated by:

$$\left.\frac{dV_c}{dt}\right|_{MAX} = k_{Cdv0} \cdot C_{DC}^{k_{CdvC}} \cdot V_{Cdc}^{k_{CdvV}}$$

k_{Cdv0}, k_{CdvC}, k_{CdvV} capacitor meta-parameters for $\left.\frac{dV_c}{dt}\right|_{MAX}$ estimation of the considered capacitor technology.

The cost of the discrete capacitor ($Cost_{Cap}$) can be estimated by:

$$Cost_{Cap} = Cost_{Cdc0} + k_{Ccost0} \cdot C_{DC}^{k_{CcostC}} \cdot V_{Cdc}^{k_{CcostV}}$$

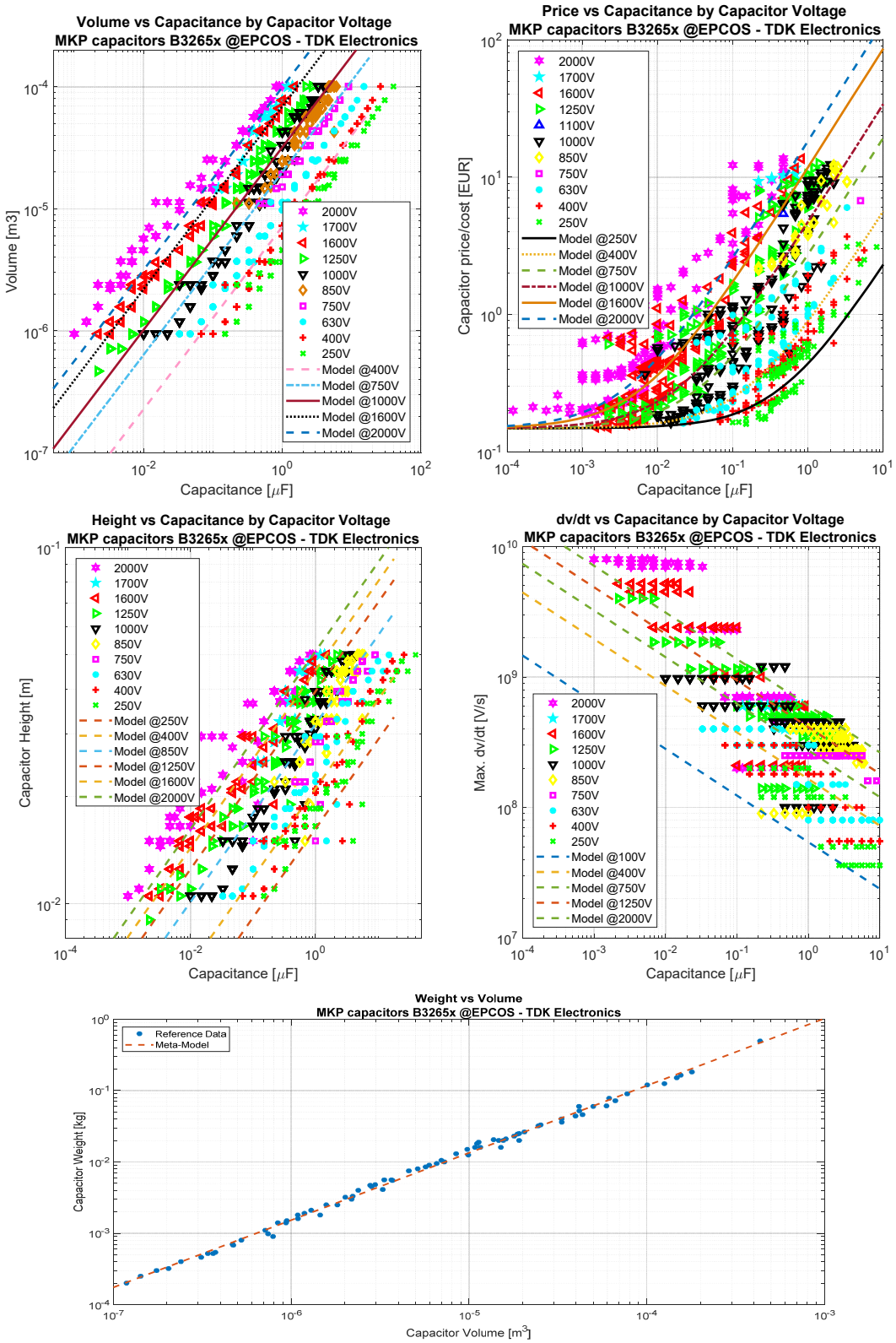

Figure A- 1 Capacitor parameters versus capacitance versus nominal voltage for MKP capacitor N3265x from EPCOS TDK Electronics.

where, $Cost_{Cdc0}, k_{Ccost0}, k_{CcostC}, k_{CcostV}$ are the capacitor meta-parameters for cost estimation of single capacitor C_{DC} and for the considered capacitor technology.

Table A- 1 summarizes the fitted/calculated meta-parameters of the previously introduced meta-models for the MKP DC snubber capacitors series B32665x from EPCOS-TDK Electronics, which is the reference DC capacitor technology considered within this work.

Table A- 1 Parameters and Meta-parameters for the considered DC capacitor reference technology MKP DC snubber capacitors series B32665x from EPCOS-TDK Electronics.

Parameter	Meta-parameter	Value	Parameter	Meta-parameter	Value
Volume (Vol_{Cap}) [m³]	k_{Cvol0}	1.2339e-5	$\frac{dV_c}{dt}_{MAX}$ **[kV/s]**	k_{Cdv0}	9.5789
	k_{CvolC}	0.7481		k_{CdvC}	-0.3576
	k_{CvolV}	1.6340		k_{CdvV}	0.8037
Height (H_{Cap}) [cm]	k_{Ch0}	2.43	**Cost [EUR] ($Cost_{Cap}$)**	$Cost_{Cdc0}$	0.1477
	k_{ChC}	0.2497		k_{Ccost0}	0.8175
	k_{ChV}	0.5519		k_{CcostC}	0.8678
Weight [kg] ($Weight_{Cap}$)	k_{Cp0}	689.717		k_{CcostV}	1.9851
	k_{CpVol}	0.9426	E_{Cmax} **[J]**		3.57

A.2 Power semiconductors

Meta-models and identified meta-parameters for estimation of relevant power semiconductor parameters are presented in this section. The reference power semiconductor technology is the StrongIRFET Power MOSFET family from Infineon, which are devices optimized for low on-state resistance and high current capability, ideal for low frequency applications. Figure A- 2 shows an overview of available power semiconductor devices, maximum continuous drain current versus blocking voltage, for the StrongIRFET Power MOSFET family from Infineon. The maximum continuous drain current is a performance figure of power semiconductor devices which is given at reference temperature conditions, and for the StrongIRFET devices it is given for a case temperature of 25°C, so it can be estimated by

$$I_{D25}^2 = \frac{T_{jmx} - 25°C}{R_{DS}(T_{jmx}) \cdot R_{thJC}}$$

where, T_{jmx} is the maximum junction temperature, R_{thJC} is the junction to case thermal resistance of the device, and R_{DS} is the on-state resistance of the device, which is temperature dependent.

Normally, the power semiconductor is selected based on the required blocking voltage and current capability, so parameters estimation based on those two requirements could be beneficial from the practical point of view. However, current capability itself is not a MOSFET parameter as it depends on the selected thermal management of the device and therefore difficult to determine beforehand.

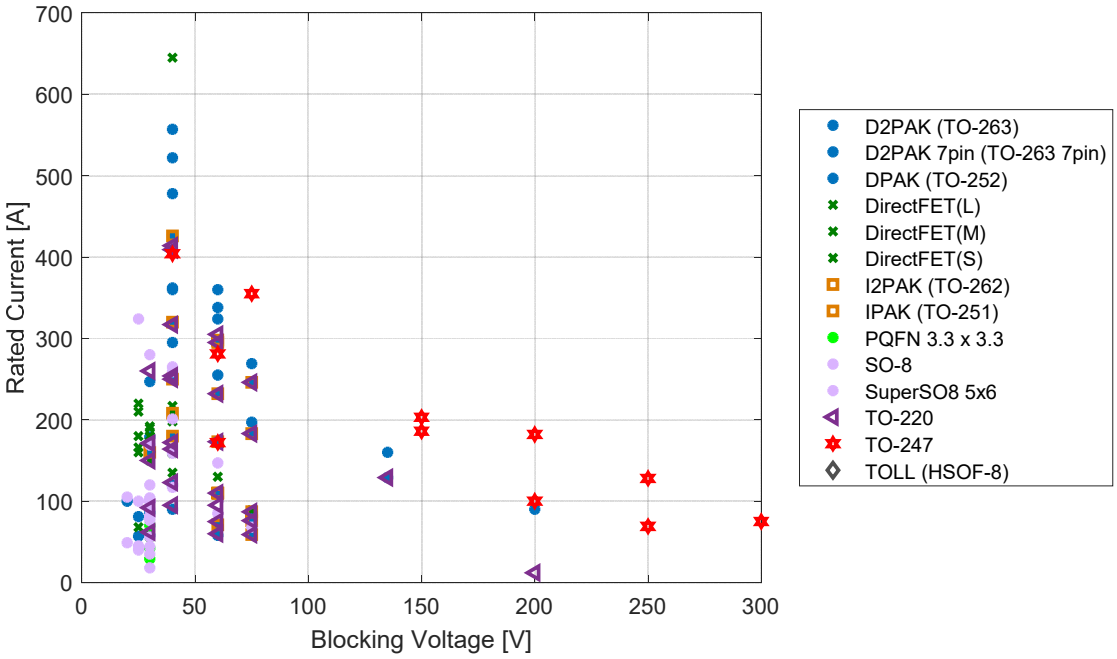

Figure A- 2 Overview of available power semiconductor devices from Infineon StrongIRFET Power MOSFET family. Rated Current at 25°C reference temperature and maximum blocking voltage for different packages.

Instead of the current capability, the die area seems to be more appropriated for parametrization of power MOSFETs as it is a fix parameter for the given device and many of device properties/parameters depends on it. However, the die area is not normally given in the device datasheet.
The proposed meta-models for power MOSFET parameter estimation are based on blocking voltage (V_{Block}) and equivalent die area (A_{chip}). The equivalent die area is a calculated value, which has been estimated based on the data available provided in the datasheet of the device. As some of the Power MOSFET parameters depends on the packing (especially the thermal parameters), then the TO-247 package has been considered as reference package and only data for that package has been used for the relevant package dependent parameters.

To estimate the parameters and the equivalent die area, first, the devices with equal and lower thermal resistance (larger die area) have been considered, so the equivalent die area keeps constant. Figure A- 3 shows the ratio $\frac{R_{DS.REF}}{R_{thJC}}$ for the power MOSFET with TO-247 package. It can be observed that the ratio $\frac{R_{DS.REF}}{R_{thJC}}$ scales with the blocking voltage when the die are keeps constant, therefore:

$$\frac{R_{DS.REF}(A_{chipREF})}{R_{thJC}(A_{chipREF})} \propto V_{Block}^{k_{MOS.RD2}}$$

then $k_{MOS.RD2}$ has been estimated from that ratio for constant die area.
For all the considered devices, the equivalent die area has been estimated as the average value from:

- Reference on-state resistance value with meta-parameters fitted for a reference die area of 50mm2.
- Junction to case thermal resistance, with meta-parameters fitted using equivalent die area estimated from reference on-state resistance
- Reference maximum continuous drain current, with maximum junction temperature of 175°C, the meta-parameters estimated as in the two previous cases, and calculated from the following expression:

$$I_{D25}^2 = \frac{T_{jmx} - 25°C}{\left(k_{MOS.RD0} + k_{MOS.RD1} \cdot V_{Block}^{k_{MOS.RD2}}\right) \cdot \left(1 + \frac{k_{MOS.\alpha0} \cdot V_{Block}^{k_{MOS.\alpha1}}}{100}\right)^{T_{jmx}-25°C} \cdot k_{MOS.Rth0}} \cdot A_{chip}^{1+k_{MOS.Rth1}}$$

Figure A- 4 shows the calculated equivalent die area versus blocking voltage for the considered TO-247 Power MOSFET devices.

Once the equivalent die area had been calculated for all reference devices, then the relevant power MOSFET parameter have been analysed against the different blocking voltage (V_{Block}) and equivalent die area (A_{chip}) values within the considered family. Table A- 2 summarizes the Power MOSFET parameters and Meta-parameters for the StrongIRFET Power MOSFET family from Infineon with TO-247 package. The meta-models for power MOSFET parameter estimation are presented in the following subsections.

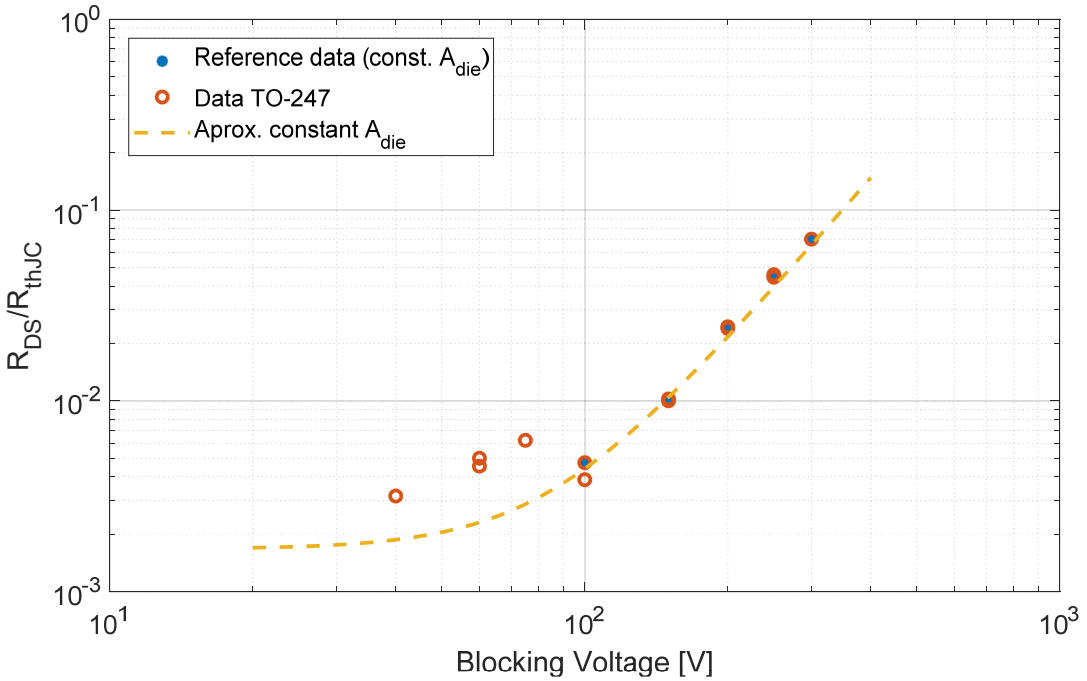

Figure A- 3 Ratio of on-state resistance to thermal resistance as function of blocking voltage.

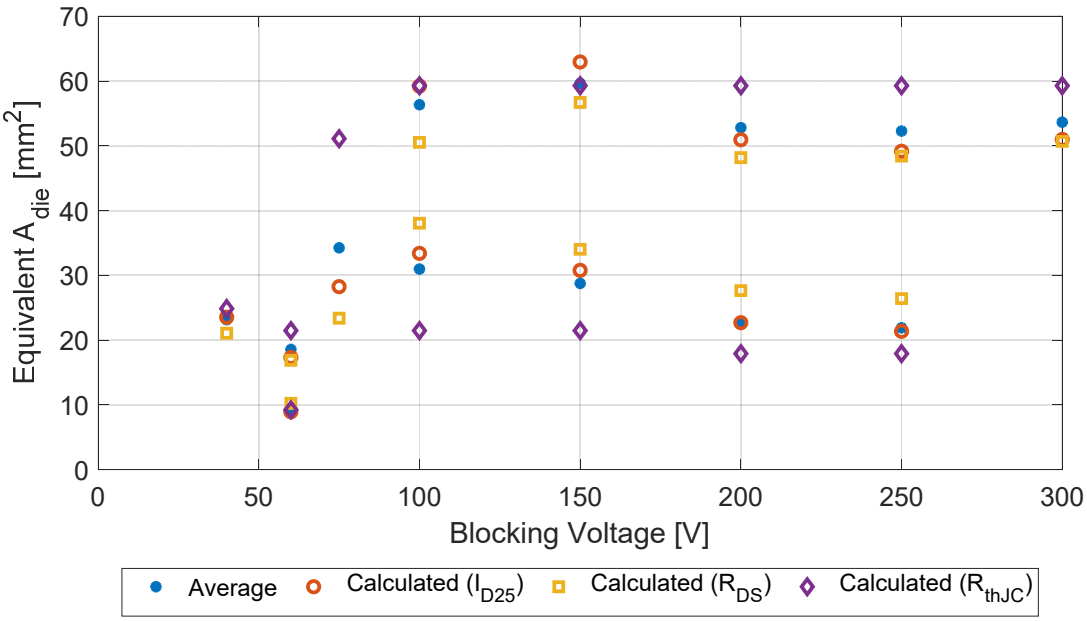

Figure A- 4 Equivalent die area versus blocking voltage for the considered TO-247 Power MOSFET devices.

Table A- 2 Power MOSFET parameters and Meta-parameters for StrongIRFET Power MOSFET family from Infineon with TO-247 package.

	Parameter	Meta-Parameter	Value		Parameter	Meta-Parameter	Value
Conduction	$R_{DS.REF}$ [Ω]	$k_{MOS.RD0}$	2.4466e-8	Cost	$Cost_{MOSFET}$ [EUR]	$Cost_{MOS0}$	0.2
		$k_{MOS.RD1}$	7.4049e-14			$k_{MOS.cost0}$	2.7368e4
		$k_{MOS.RD2}$	2.8674			$k_{MOS.cost1}$	0.3378
	$\alpha_{R_{DS}}$ [--]	$k_{MOS.\alpha0}$	0.1777			$k_{MOS.cost2}$	1.0707
		$k_{MOS.\alpha1}$	0.2335	Other	$Mass_{MOS}$ [g]		8
Thermal	R_{thJC} [°C/W]	$k_{MOS.Rth0}$	0.0025		$A_{MOS.Pack}$ [cm^2]		3.10
		$k_{MOS.Rth1}$	0.4806		$I_{MOSpackMX}$[A]		195
	R_{thCS} [°C/W]		0.24	Diode reverse recovery process	$\frac{dv_{FMAX}}{dt}$ [V/ns]	$k_{MOS.dVF0}$	4.188e-4
	R_{thJA} [°C/W]		40			$k_{MOS.dVF1}$	0.8504
	T_{jmx} [°C]		175			$k_{MOS.dVF2}$	-0.5713
Reference Values	T_{jREF} [°C]		25		$k_{MOS.IQt}$ [--]	$k_{MOS.IQt0}$	0.4958
	R_{GonREF}[Ω]		5.4			$k_{MOS.IQt1}$	0.1275
	$R_{GoffREF}$[Ω]		5.4			$k_{MOS.IQt2}$	-0.0512
	V_{DrREF} [V]		10		$k_{MOS.IRIF}$ [--]	$k_{MOS.IRIF0}$	0.0078
	$\left(\frac{di_F}{dt}\right)_{REF}$[A/µs]		100			$k_{MOS.IRIF1}$	0.4827
	I_{FREF} [A]		41			$k_{MOS.IRIF2}$	-0.0458
	Range V_{Block} [V]		{40, 300}		$k_{MOS.IRdiF}$ [--]	$k_{MOS.IRdiF0}$	0.7561
	Range A_{Chip} [mm^2]		{10, 60}			$k_{MOS.IRdiF1}$	0.0813
Switching	t_{rc0} [ns]	$k_{MOS.trc0}$	5.8531e5			$k_{MOS.IRdiF2}$	0.0319
		$k_{MOS.trc1}$	-0.6653		I_{RR0} [A]	$k_{MOS.IRR0}$	2.3853
		$k_{MOS.trc2}$	0.5124			$k_{MOS.IRR1}$	0.6790
	t_{fc0} [ns]	$k_{MOS.tfc0}$	7.1488e6			$k_{MOS.IRR2}$	0.2444
		$k_{MOS.tfc1}$	-0.8182	Gate	Q_{GMOS} [nC]	$k_{MOS.QG0}$	7.7621e7
		$k_{MOS.tfc2}$	0.6984			$k_{MOS.QG1}$	-1.03
	C_{rss0} [ns]	$k_{MOS.Crss0}$	1.8237e11			$k_{MOS.QG2}$	0.7832
		$k_{MOS.Crss1}$	-1.7408		V_{pl} [V]		4.8154
		$k_{MOS.Crss2}$	0.9825		$V_{GS(th)}$[V]		3.1038

A.2.1 Reference values

Some of the reference Power MOSFET parameters are given for specific reference conditions, which may vary between the different devices within the MOSFET family. To provide a general frame for the MOSFET parameter estimation, specific reference values have been defined to the MOSFET technology and the individual MOSFET parameters have been scaled according to its reference values and the technology reference values. The reference values are reported in Table A-2, and are listed as following:

- Reference Junction temperature (T_{jREF}): normally the electrical parameters are given for 25°C reference temperature, and that has been the selected value for T_{jREF}.
- Reference total gate circuit resistance for turning on process (R_{GonREF}): The switching parameters are given for reference conditions, which includes along other the total gate resistance. R_{GonREF} has been selected as the maximum gate resistance for switching reference conditions along all the considered devices within the MOSFET technology.
- Reference total gate circuit resistance for turning off process ($R_{GoffREF}$): It has been selected as the maximum gate resistance for turn-off switching reference conditions along all the considered devices within the MOSFET technology.
- Reference drive voltage (V_{DrREF}): It has been selected as the minimum drive voltage reported for the switching parameters along all the considered devices within the MOSFET technology.
- Reference diode conduction current before turn-off (I_{FREF}): It has been selected as the minimum value along the reported values in the device datasheet for switching conditions within the MOSFET technology.
- Reference rate of change of diode current during turn-off process $\left(\left(\frac{di_F}{dt}\right)_{REF}\right)$: It has been selected as the minimum value along the reported values in the device datasheet for switching conditions within the MOSFET technology.
- Blocking voltage range: The analysed parameters and obtained meta-parameters are for Power MOSFET with blocking voltage between 40V and 300V.
- Equivalent die area range: The analysed parameters and obtained meta-parameters are for Power MOSFETs with a calculated equivalent die area between 10mm^2 and 60mm^2.

A.2.2 On-state resistance

The on-state resistance can be modelled as function of the MOSFET junction temperature (T_{jMOS}) by:

$$R_{DS}(T_{jMOS}) = R_{DS.REF} \cdot \left(1 + \frac{\alpha_{R_{DS}}}{100}\right)^{T_{jMOS} - T_{jREF}}$$

where $\alpha_{R_{DS}}$ is the thermal coefficient of the on-state resistance, which can be calculated from the typical data reported in the device datasheet, and $R_{DS.REF}$ is the on-state resistance at reference junction temperature T_{jREF}. The MOSFET electrical parameters are provided in the datasheet for a reference temperature of 25°C, and therefore all the analysed reference parameters within this study have been considered/scaled to $T_{jREF} = 25°C$.

Based on the analysed data for the considered Power MOSFET technology, the on-state resistance parameters can be estimated as function of the device equivalent chip area and blocking voltage as follows:

$$R_{DS.REF} = \frac{k_{MOS.RD0} + k_{MOS.RD1} \cdot V_{Block}^{k_{MOS.RD2}}}{A_{chip}}$$

$$\alpha_{R_{DS}} = k_{MOS.\alpha 0} \cdot V_{Block}^{k_{MOS.\alpha 1}}$$

Where, $k_{MOS.RD0}, k_{MOS.RD1}, k_{MOS.RD2}, k_{MOS.\alpha 0}$ and $k_{MOS.\alpha 1}$ are the meta-parameters for on-state resistance evaluation of the Power MOSFET. Figure A- 5 shows the thermal coefficient of the on-state resistance as function of the device blocking voltage as well as the calculated value based on the proposed meta-model ($k_{MOS.\alpha 0}$ and $k_{MOS.\alpha 1}$).

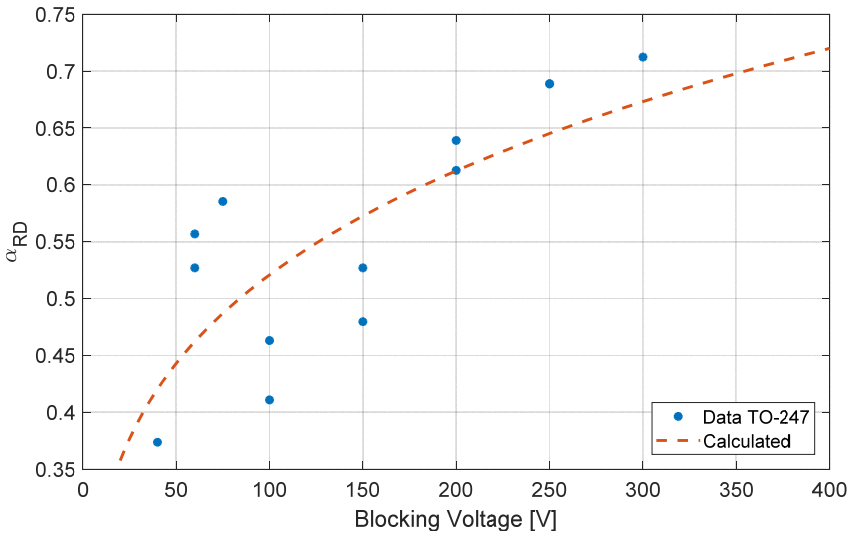

Figure A- 5 Thermal coefficient of the MOSFET on-state resistance versus device blocking voltage

Figure A- 6 shows the reference on-state resistance (at 25°C) versus the device blocking voltage. The reference data as taken from device datasheet is plotted in red circles (blue dots for the considered reference data with fix die area), and the estimation based on meta-model is plotted with cross in cyan colour. Evaluation of the meta-model with two fixed equivalent die areas are also plotted in Figure A- 6.

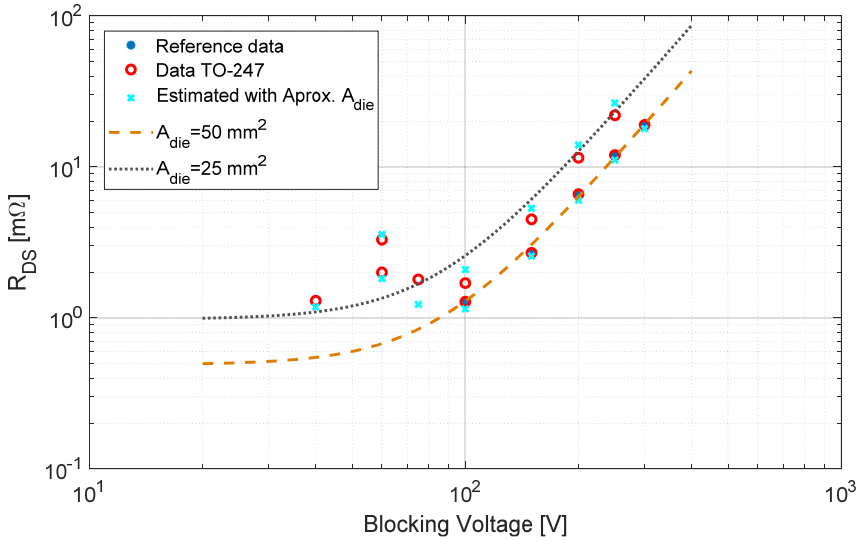

Figure A- 6 Reference on-state resistance (@25°C) versus blocking voltage.

A.2.3 Thermal parameters

The junction to case thermal resistance has been assumed to be independent on blocking voltage and it is estimated by:

$$R_{thJC} = \frac{k_{MOS.Rth0}}{A_{chip}^{k_{MOS.Rth1}}}$$

Figure A- 7 shows the junction-to-case thermal resistance as function of blocking voltage and equivalent chip area. The fitted meta-parameters $k_{MOS.Rth0}$ and $k_{MOS.Rth1}$ for the considered technology can be found in Table A- 2.

The case to sink thermal resistance (R_{thCS}) is a constant parameter along the considered devices with TO-247 package, with a value of 0.24 [°C/W]. Similarly, a junction to ambient thermal resistance (R_{thJA}) of 40 [°C/W] has been found to be constant value for all the devices.

The maximum junction temperature (T_{jmx}) for the power MOSFET is constant value along the StrongIRFET family, and it is 175 °C.

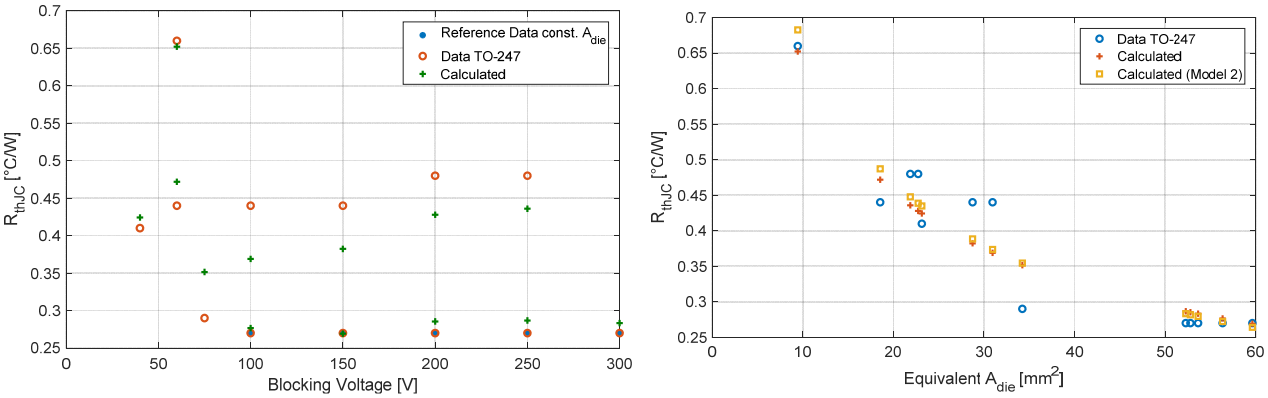

Figure A- 7 Junction-to-case thermal resistance for different blocking voltage (left) and equivalent die area (right)

A.2.4 Maximum continuous drain current

As previously defined, the maximum continuous current is a performance index which is estimated based on the on-state resistance, the thermal resistance, and the junction temperature. The maximum continuous drain current for a case temperature of 25°C is a reference value found in the device datasheet, based on the proposed meta-models, it can be estimated by:

$$I_{D25}^2 = \frac{T_{jmx} - 25°C}{\left(k_{MOS.RD0} + k_{MOS.RD1} \cdot V_{Block}^{k_{MOS.RD2}}\right) \cdot \left(1 + \frac{k_{MOS.\alpha0} \cdot V_{Block}^{k_{MOS.\alpha1}}}{100}\right)^{T_{jmx}-25°C} \cdot k_{MOS.Rth0}} \cdot A_{chip}^{1+k_{MOS.Rth1}}$$

Figure A- 8 shows the maximum continuous drain current versus blocking voltage, including data as reported in the device datasheet and the calculated values considering the meta-models and fitted meta-parameters. It can be observed that estimated values agree well with reported values in the datasheet.

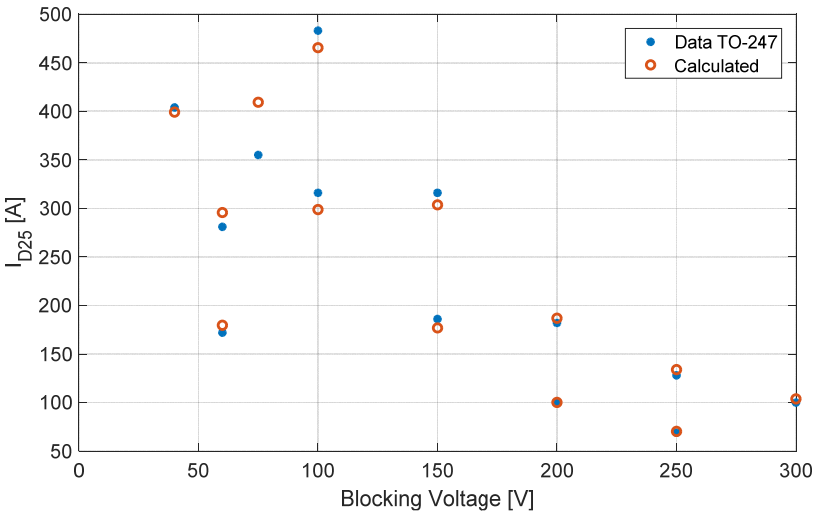

Figure A- 8 Maximum continuous drain current. Data as reported in the device datasheet versus calculated value considering the meta-models and fitted meta-parameters.

A.2.5 Turn-on energy parameters

The total energy loss related with turn-on process can be estimated by:

$$E_{on} = \frac{1}{2} \cdot V_{DD} \cdot I_{Don} \cdot \left(t_{rc} + t_{rr} + t_{fv}\right) + \frac{5}{4} \cdot Q_{rr} \cdot V_{DD}$$

where, V_{DD} is the blocked voltage before turn-on action, I_{Don} is the conducted current after turn-on action, t_{rc} is the current rise time at turn on, t_{rr} is the reverse-recovery time of free-wheeling diode turn-off process, t_{fv} is the voltage fall time at turn on, and Q_{rr} is the reverse-recovery charge of the free-wheeling diode.

The current rise time at turn on (t_{rc}) can be approximated by

$$t_{rc} = \tau_{Gon} \cdot \left(-\log\left(1 - \frac{V_{pl}}{V_{Dr}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{Dr}}\right)\right),$$

where τ_{Gon} is the time constant for gate turn-on process, assumed proportional to the total gate circuit resistance for turn-on process and input capacitance of the power MOSFET; V_{pl} is the gate-source plateau voltage (Miller effect), $V_{GS(th)}$ is the gate-source threshold voltage and V_{Dr}: driver voltage. Since τ_{Gon} is a parameter difficult to estimate, alternatively t_{rc} can be estimated by

$$t_{rc} \approx t_{rc0} \cdot \frac{R_{Gon}}{R_{GonREF}} \cdot \frac{\left(-\log\left(1 - \frac{V_{pl}}{V_{Dr}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{Dr}}\right)\right)}{\left(-\log\left(1 - \frac{V_{pl}}{V_{DrREF}}\right) + \log\left(1 - \frac{V_{GS(th)}}{V_{DrREF}}\right)\right)}$$

where t_{rc0} is the reference current rise time, which is a given value in the device datasheet for reference conditions R_{GonREF} (reference total gate circuit resistance for turning on process) and V_{DrREF} (reference driver voltage).

Figure A- 9 shows V_{pl} and $V_{GS(th)}$ versus blocking voltage for the StrongIRFET Power MOSFET family. It can be observed minor variations on these parameters along the blocking voltage range for the considered technology, therefore these parameters have been considered as constant parameters for a given technology.

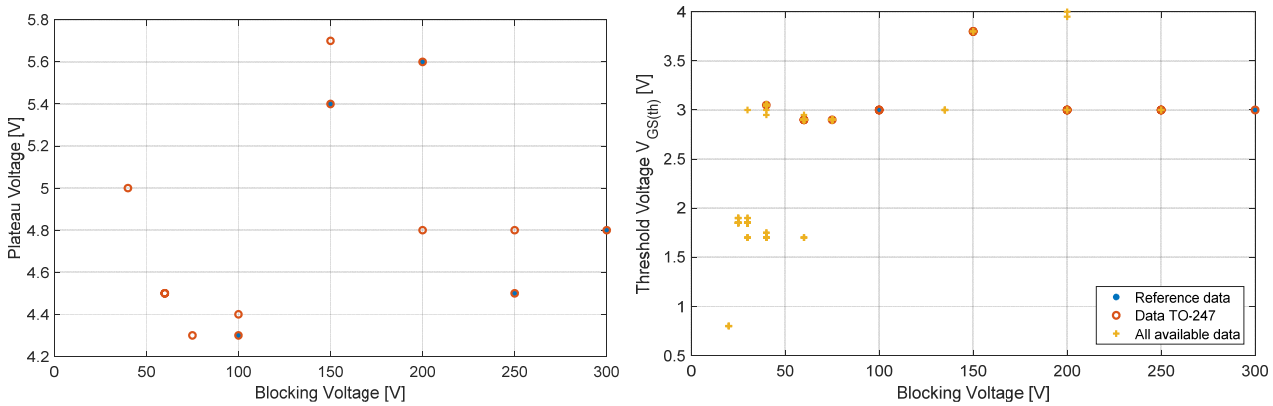

Figure A- 9 Plateau Voltage (left) and Threshold voltage (right) versus blocking voltage for the StrongIRFET Power MOSFET family.

The reference current rise time, reported in the device datasheet, has been scaled to the considered reference conditions for the MOSFET technology, as defined in section A.2.1. Figure A- 10 shows the reference current rise time versus blocking voltage for the StrongIRFET Power MOSFET family. It is proposed to estimate t_{rc0} by the follow meta-model:

$$t_{rc0} = k_{MOS.trc0} \cdot V_{block}^{k_{MOS.trc1}} \cdot A_{chip}^{k_{MOS.trc2}}$$

Where, $k_{MOS.trc0}, k_{MOS.trc1}, k_{MOS.trc2}$ are the meta-parameters for reference current rise time estimation.

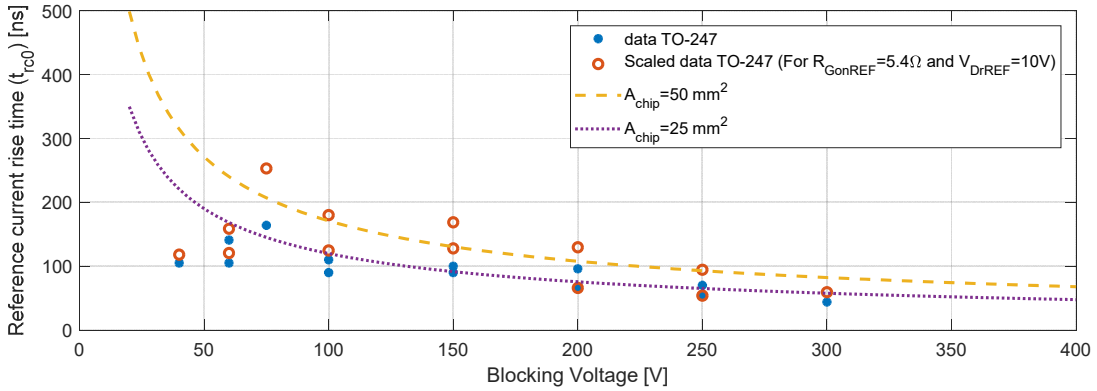

Figure A- 10 Reference current rise time versus blocking voltage for the StrongIRFET Power MOSFET family

The voltage fall time at turn on (t_{fv}) can be approximated by

$$t_{fv} = V_{DD} \cdot R_{Gon} \cdot \frac{C_{rss}^*}{V_{Dr} - V_{pl}}$$

where the average reverse transfer capacitance (C_{rss}^*) can be approximated by:

$$C_{rss}^* = \frac{C_{rss}(V_{DD}) + C_{rss}(R_{DS} \cdot I_{Don})}{2} \approx \frac{C_{rss0}}{2}$$

And the reverse transfer capacitance at zero volts (C_{rss0}) is a MOSFET parameter that can be found in the device datasheet. It is proposed to estimate C_{rss0} by:

$$C_{rss0} = k_{MOS.Crss0} \cdot V_{block}^{k_{MOS.Crss1}} \cdot A_{chip}^{k_{MOS.Crss2}}$$

Where, $k_{MOS.Crss0}, k_{MOS.Crss1}, k_{MOS.Crss2}$ are the meta-parameters for reverse transfer capacitance estimation. Figure A- 11 shows the reverse transfer capacitance versus blocking voltage for the StrongIRFET Power MOSFET family along with the evaluation of the proposed meta-model with fitted meta-parameters reported in Table A- 2.

Finally, t_{fv}, and indirectly R_{Gon}, is limited by the maximum allowed diode voltage rate of change $\left(\frac{dv_{FMAX}}{dt}\right)$, which is a property of the MOSFET device technology:

$$\frac{V_{DD}}{t_{fv}} < \frac{dv_{FMAX}}{dt}$$

Figure A- 12 shows the maximum allowed diode voltage rate of change versus blocking voltage for the StrongIRFET Power MOSFET family along with the evaluation of the proposed meta-model for two equivalent chip area:

$$\frac{dv_{FMAX}}{dt} = k_{MOS.dVF0} \cdot V_{block}^{k_{MOS.dVF1}} \cdot A_{chip}^{k_{MOS.dVF2}}$$

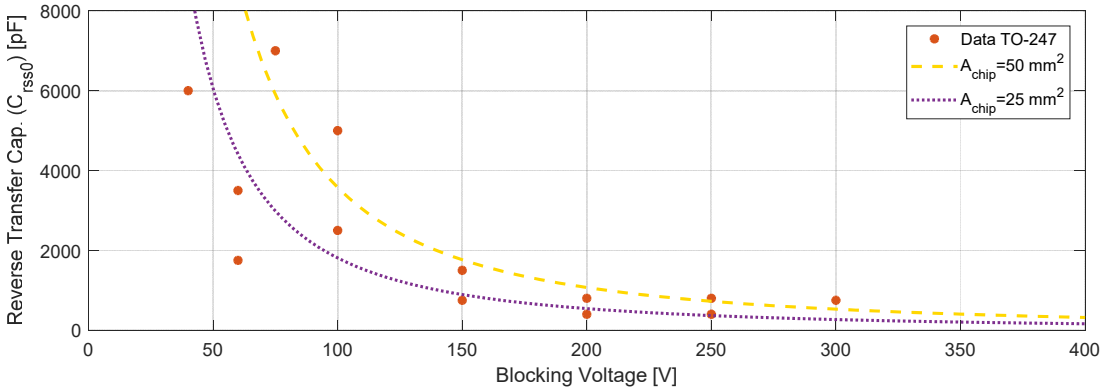

Figure A- 11 Reverse transfer capacitance versus blocking voltage for the StrongIRFET Power MOSFET family

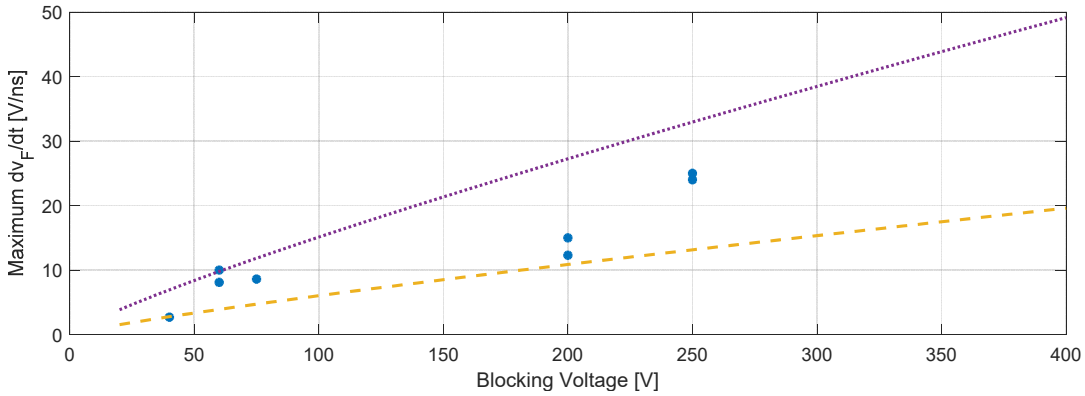

Figure A- 12 Maximum allowed diode voltage rate of change versus blocking voltage for the StrongIRFET Power MOSFET family

A.2.6 Reverse recovery parameters

There are three main parameters related to diode reverse recovery process: the peak reverse recovery current (I_{RR}), the reverse recovery time (t_{rr}) and the reverse recovery charge (Q_{rr}), which are corelated by

$$I_{RR} = k_{MOS.IQt} \cdot \frac{Q_{rr}}{t_{rr}}$$

The parameter $k_{MOS.IQt}$ can be calculated from reference reverse recovery values ($I_{RR0}, t_{rr0}, Q_{rr0}$) found in the device datasheet; in the literature this value is normally approximated to 2, however it has been found that $k_{MOS.IQt}$ varies mainly with device blocking voltage for the considered reference MOSFET technology:

$$k_{MOS.IQt} = k_{MOS.IQt0} \cdot V_{block}^{k_{MOS.IQt1}} \cdot A_{chip}^{k_{MOS.IQt2}}$$

For a given switching conditions, the peak reverse recovery current can be approximated by:

$$I_{RR} = I_{RR0} \cdot \left(\frac{I_F}{I_{FREF}}\right)^{k_{MOS.IRIF}} \cdot \left(\frac{\frac{di_F}{dt}}{\left(\frac{di_F}{dt}\right)_{REF}}\right)^{k_{MOS.IRdiF}}$$

where I_{RR0} is the reference peak reverse-recovery current, which normally can be found in the device datasheet for reference conditions I_{FREF} (reference diode conduction current before turn-off) and $\left(\frac{di_F}{dt}\right)_{REF}$ (reference rate of change of diode current during turn-off process); and $k_{MOS.IRIF}$, $k_{MOS.IRdiF}$ are diode reverse recovery relationship parameters which can be calculated from $I_{RR}\ vs\ I_F\ vs \frac{di_F}{dt}$ relationships normally found in the device datasheet.

It is proposed to estimate $k_{MOS.IRIF}$ and $k_{MOS.IRdiF}$ as following:

$$k_{MOS.IRIF} = k_{MOS.IRIF0} \cdot V_{block}^{k_{MOS.IRIF1}} \cdot A_{chip}^{k_{MOS.IRIF2}}$$

$$k_{MOS.IRdiF} = k_{MOS.IRdiF0} \cdot V_{block}^{k_{MOS.IRdiF1}} \cdot A_{chip}^{k_{MOS.IRdiF2}}$$

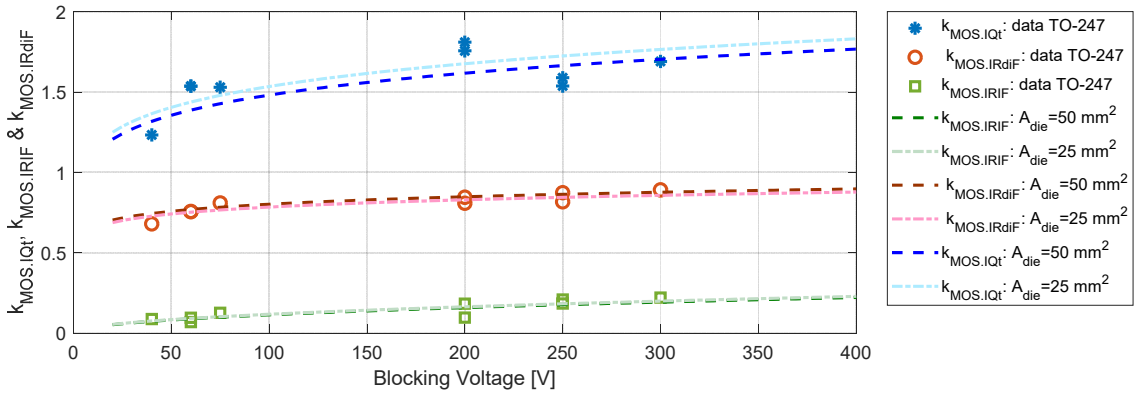

Figure A- 13 Reverse recovery relationship parameters versus blocking voltage for the StrongIRFET Power MOSFET family

Figure A- 13 shows the reverse recovery relationship parameters versus blocking voltage for the StrongIRFET Power MOSFET family along with the proposed meta-models for two different equivalent die areas.

For the estimation of the reference peak reverse-recovery current (I_{RR0}), all data collected from the device datasheets have been scaled to the global reference conditions I_{FREF} and $\left(\frac{di_F}{dt}\right)_{REF}$, as defined in section A.2.1. Then, the following expression has been fitted to estimated I_{RR0}:

$$I_{RR0} = k_{MOS.IRR0} \cdot V_{block}^{k_{MOS.IRR1}} \cdot A_{chip}^{k_{MOS.IRR2}}$$

Figure A- 14 shows the reference peak reverse-recovery current versus the device blocking voltage for the StrongIRFET Power MOSFET family along with the proposed meta-models for two different equivalent die areas.

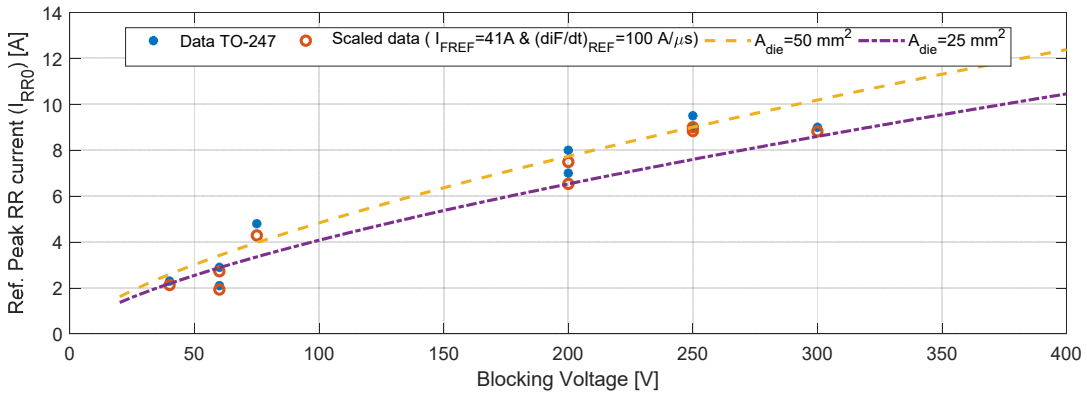

Figure A- 14 Reference peak reverse-recovery current versus blocking voltage for the StrongIRFET Power MOSFET family

Finally, given the switching conditions: the diode conduction current before turn-off (I_F) and the rate of change of diode current during turn-off process ($\frac{di_F}{dt}$), then the peak reverse recovery current can be evaluated, and the remain parameters, t_{rr} and Q_{rr}, can be approximated by

$$t_{rr} \approx 2 \cdot \frac{I_{RR}}{\frac{di_F}{dt}}$$

$$Q_{rr} = I_{RR} \cdot \frac{t_{rr}}{k_{IQt}}$$

A.2.7 Turn-off energy parameters

The turn-off energy loss can be approximated by

$$E_{off} = \frac{1}{2} \cdot V_{DD} \cdot I_{Doff} \cdot \left(t_{fc} + t_{rv}\right)$$

where, V_{DD} is the blocked voltage after turn-off action, I_{Doff} is the conducted current before turn-off action, t_{fc} is the current falling time at turn off, and t_{rv} is the voltage rise time at turn off.

The voltage rise time at turn-off (t_{rv}) can be approximated by

$$t_{rv} = V_{DD} \cdot R_{Goff} \cdot \frac{C^*_{rss}}{V_{pl}}$$

Where R_{Goff} is the total gate circuit resistance for turning off process, and with the average reverse transfer capacitance (C^*_{rss}) evaluated as previously indicated in section A.2.5.

The current falling time (t_{fc}) can be estimated by:

$$t_{fc} = \tau_{Goff} \cdot \log\left(\frac{V_{pl}}{V_{G(th)}}\right)$$

τ_{Goff} time constant for gate turn-off process, assumed proportional to gate resistance and MOSFET input capacitance, and therefore t_{fc} can be approximated by:

$$t_{fc} = t_{fc0} \cdot \frac{R_{Goff}}{R_{GoffREF}}$$

Where, t_{fc0} is the reference current falling time at reference total gate circuit resistance for turning off process ($R_{GoffREF}$), and it can be estimated by:

$$t_{fc0} = k_{MOS.tfc0} \cdot V_{block}^{k_{MOS.tfc1}} \cdot A_{chip}^{k_{MOS.tfc2}}$$

Figure A- 15 shows the reference current falling time versus blocking voltage for the StrongIRFET Power MOSFET family along with the proposed meta-models for two different equivalent die areas.

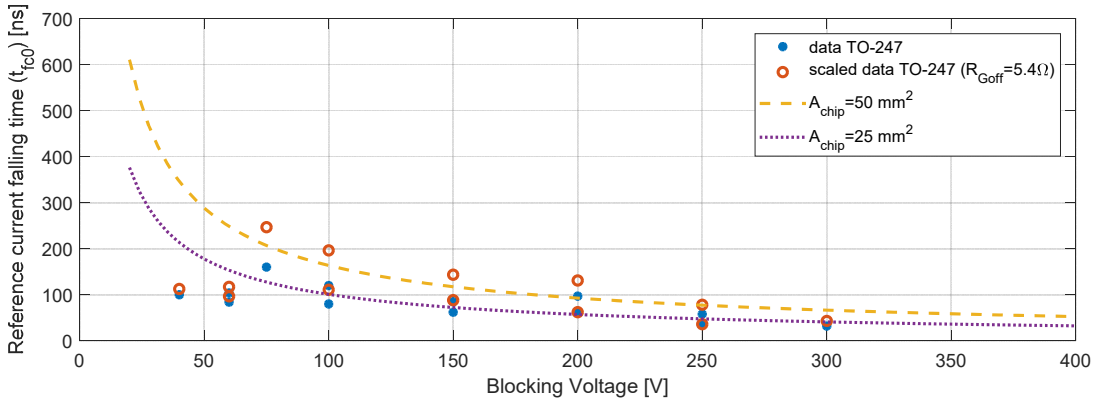

Figure A- 15 Reference current falling time versus blocking voltage for the StrongIRFET Power MOSFET family

A.2.8 Device Cost

The cost of the power MOSFET ($Cost_{MOSFET}$) has been estimated based on budget price reported by the manufacturer. It scales with blocking voltage and die area, and it is proposed to be estimated by:

$$Cost_{MOSFET} = Cost_{MOS0} + k_{MOS.cost0} \cdot V_{block}^{k_{MOS.cost1}} \cdot A_{chip}^{k_{MOS.cost2}}$$

Figure A- 16 shows the Power MOSFET budget price versus blocking voltage (left) and equivalent die area (right) for the StrongIRFET Power MOSFET family along with the evaluation of the fitted proposed meta-model for two different blocking voltage and equivalent chip areas.

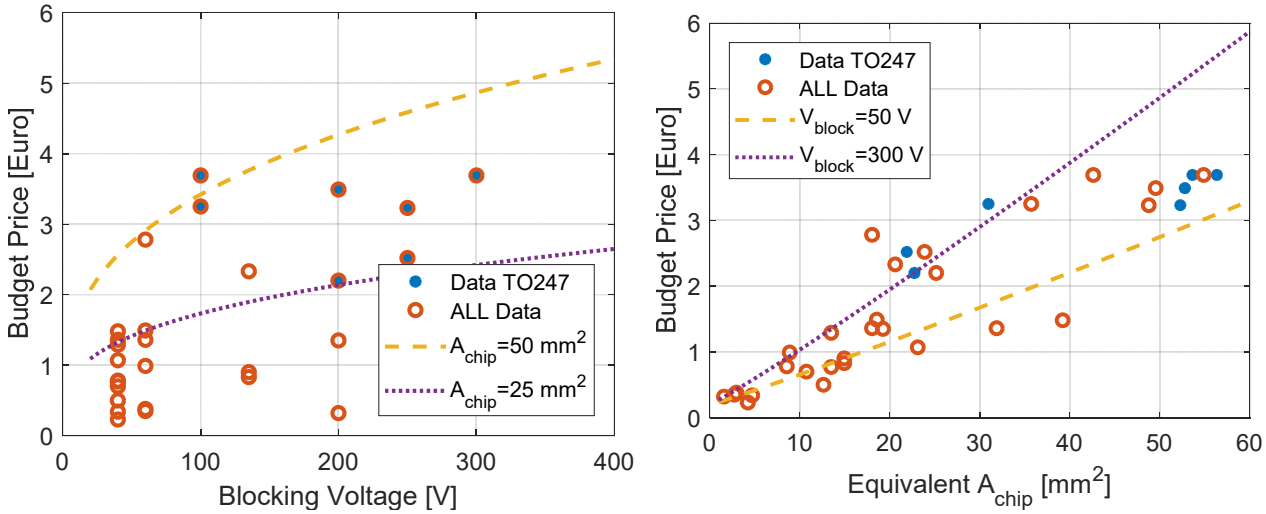

Figure A- 16 Power MOSFET budget price versus blocking voltage (left) and equivalent die area (right) for the StrongIRFET Power MOSFET family

A.2.9 Total gate charge

The total gate charge (Q_{GMOS}) can be estimated by the meta-parameters $k_{MOS.QG0}$, $k_{MOS.QG1}$ and $k_{MOS.QG2}$ for the reference MOSFET technology, as following:

$$Q_{GMOS} = k_{MOS.QG0} \cdot V_{block}^{k_{MOS.QG1}} \cdot A_{chip}^{k_{MOS.QG2}}$$

Figure A- 17 shows the total gate charge versus blocking voltage for all available devices in the StrongIRFET Power MOSFET family along with the evaluated meta-model for three different equivalent chip areas.

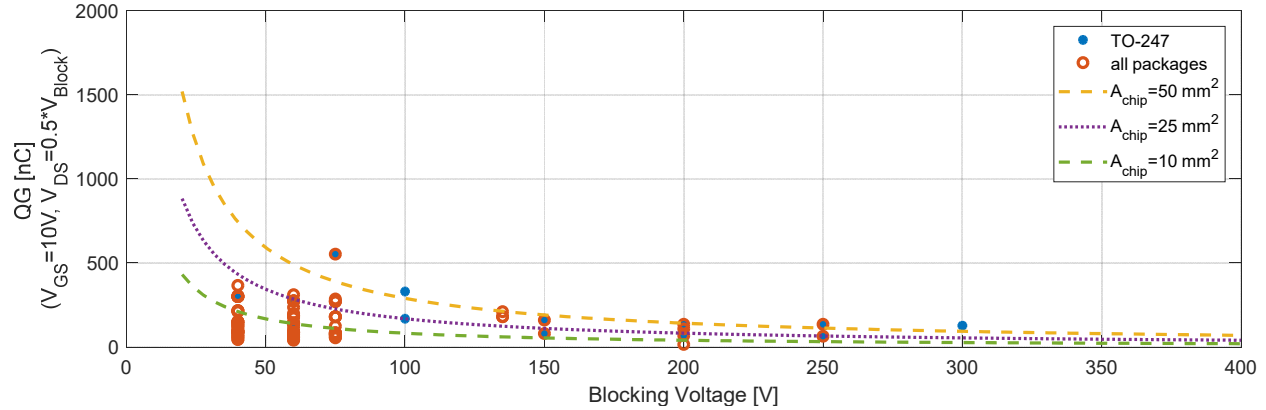

Figure A- 17 total Gate charge versus blocking voltage for the StrongIRFET Power MOSFET family

A.3 DC inductors

If an inductor design technology is kept (core material, conductor type, core geometry…) for different inductance values (L) and nominal current requirements ($I_{L,N}$), the overall inductor volume (Vol_L) and total weight $Weight_L$ are approximated by:

$$Weight_L = k_{LWt0} \cdot I_{L,N}^{k_{LWtI0}} + k_{LWt1} \cdot E_L^{k_{LWtE}} \cdot I_{L.N}^{k_{LWtI1}}$$

$$Vol_L = k_{LVt0} \cdot I_{L.N}^{k_{LVtI0}} + k_{LVt1} \cdot E_L^{k_{LVtE}} \cdot I_{L.N}^{k_{LVtI1}}$$

$$E_L = \frac{1}{2} \cdot L \cdot I_{L.N}^2$$

where, E_L is the inductor nominal energy, $k_{LWt0}, k_{LWtI0}, k_{LWt1}, k_{LWtE}, k_{LWtI1}$ are the inductor meta-parameters for total weight estimation, and $k_{LVt0}, k_{LVtI0}, k_{LVt1}, k_{LVtE}, k_{LVtI1}$ are the inductor meta-parameters for overall volume estimation, which can be obtained against reported data by the inductor manufacturers of a specific inductor technology.

The SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer have been considered as reference inductor technology. Table A- 3 summarizes the parameters and meta-parameters for the considered DC inductor technology.

Table A- 3 Parameters and Meta-parameters for the considered DC inductor reference technology. SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer

Parameter	Meta-parameter	Value	Parameter	Meta-parameter	Value
$\boldsymbol{Weight_L}$ $[\boldsymbol{kg}]$	k_{LWt0}	3.117e-4	$\boldsymbol{Vol_L}$ $[\boldsymbol{m^3}]$	k_{LVt0}	3.4258e-7
	k_{LWtI0}	1.6543		k_{LVtI0}	1.7731
	k_{LWt1}	6.0845		k_{LVt1}	0.0028
	k_{LWtE}	0.8944		k_{LVtE}	1.1615
	k_{LWtI1}	-0.1904		k_{LVtI1}	-0.4999
$\boldsymbol{W_{cL}}$ $[\boldsymbol{kg}]$	k_{LWc0}	0.6576	$\boldsymbol{W_{wdg}}$ $[\boldsymbol{kg}]$	k_{LWw0}	0.1795
	k_{LWcWt}	0.9692		k_{LWwWt}	0.9049
$\boldsymbol{P_{wL0}}$ $[\boldsymbol{W}]$	k_{LPw0}	0.0089	$\boldsymbol{P_{coreL0}}$ $[\boldsymbol{W}]$	$k_{\rho c0}$	0.2654
	k_{LPwI0}	1.6812		$k_{\rho cWc}$	1.0184
	k_{LPw1}	19.8484	$\boldsymbol{f_{Lhref}}$		300 Hz
	k_{LPwE}	0.6256	$\boldsymbol{\Xi_L}$		0.25
	k_{LPwI1}	0.0720	$\boldsymbol{Cost_{mat,L}}$ [EUR]	$\sigma_{core,L}$	8 €/kg
$\boldsymbol{\delta_{iLref}}$		0.30		$\sigma_{wdg,L}$	10 €/kg
$\boldsymbol{F_{rLref}}$		3/2		$Cost_{mat0,L}$	1€/unit
$\boldsymbol{\alpha_L}$		1.439	$\boldsymbol{Cost_{lab,L}}$ [EUR]	$\sigma_{lab,L}$	7€/kg
$\boldsymbol{\beta_L}$		2		$Cost_{lab0,L}$	2€/unit

Figure A- 18 shows the inductor total weight and overall volume versus inductor energy and rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

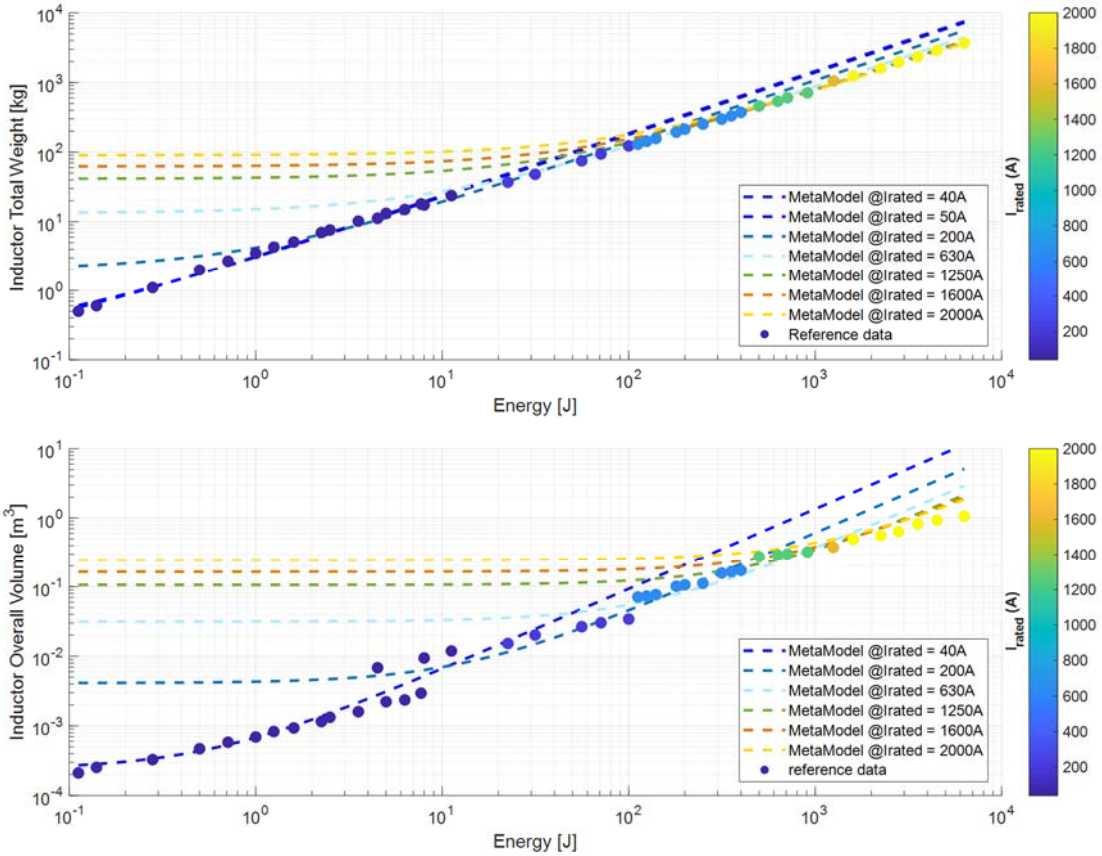

Figure A- 18 Inductor total weight (top) and overall Volume (bottom) versus inductor energy and rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

The inductor core weight (W_{cL}) and inductor winding weight (W_{wdg}) can be estimated as function of the total weight, by:

$$W_{cL} = k_{LWc0} \cdot Weight_L^{k_{LWcWt}}$$

$$W_{wdg} = k_{LWw0} \cdot Weight_L^{k_{LWwWt}}$$

$$W_{cL} + W_{wdg} \leq Weight_L$$

Where, k_{LWc0}, k_{LWcWt} are the inductor meta-parameters for core weight estimation and k_{LWw0} and k_{LWwWt} are the inductor meta-parameters for winding weight estimation, which can be estimated against reported data by the inductor manufacturers of a specific inductor technology.

Figure A- 19 shows the Inductor core weight and winding weight versus inductor total weight and rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer. Reference data and metamodel estimation are plotted in Figure A- 19.

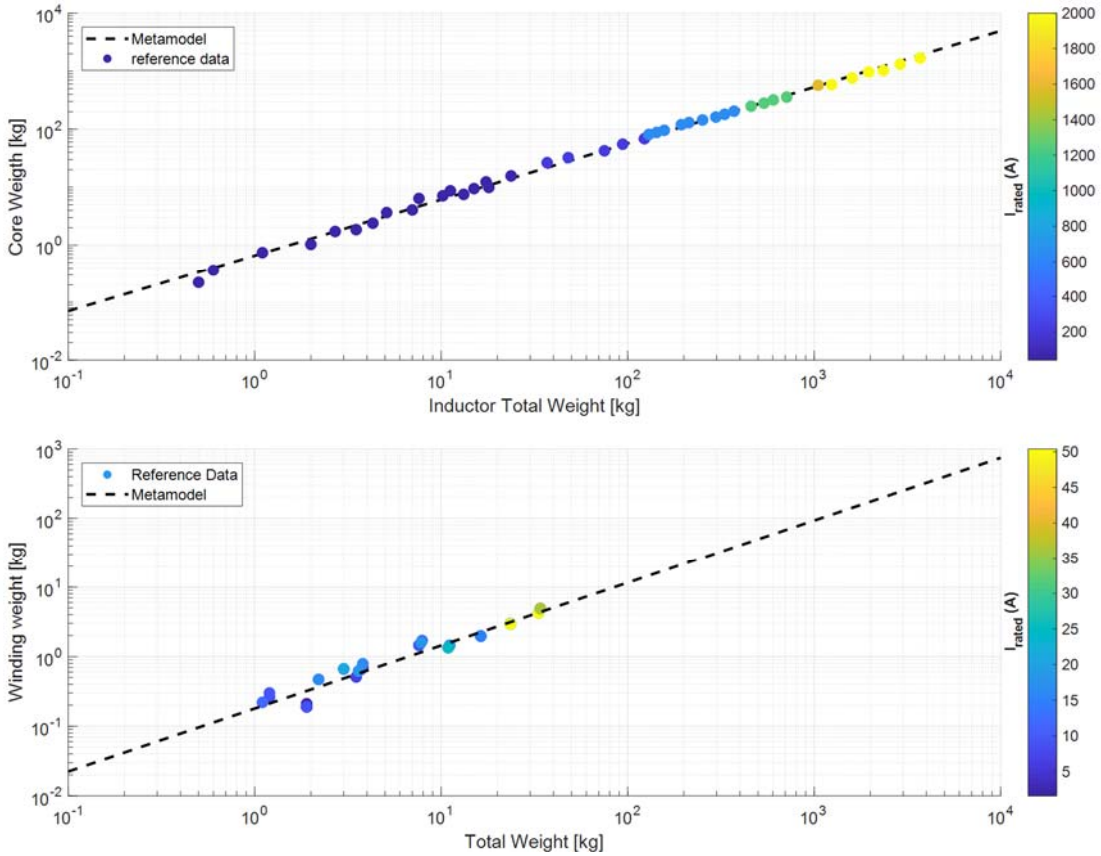

Figure A- 19 Inductor core weight (top) and winding weight (bottom) versus inductor total weight and rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

Winding losses:

The DC inductor winding loss model assumes that the inductor current is composed by mainly two components, the DC component (I_{LDC}), and the ripple current component ((I_{Lh})):

$$I_L^2 = I_{LDC}^2 + I_{Lh}^2$$

Then, the inductor winding losses (P_{wL}) can be estimated by:

$$P_{wL} = ESR_{DC} \cdot I_{LDC}^2 + ESR_{AC} \cdot I_{Lh}^2$$

where, ESR_{DC} is the DC equivalent series resistance of the inductor winding, and ESR_{AC} is the AC equivalent series resistance of the inductor winding, which is frequency dependent. It has been shown in [1] that ESR_{AC} can be approximated by:

$$ESR_{AC} \approx ESR_{DC} \cdot F_{rL}$$
$$F_{rL} \approx (1 + k_{FrL} \cdot f_{Lh}^2)$$

Where, F_{rL} is the eddy current loss factor for inductor winding, and f_{Lh} is the effective frequency of the inductor current ripple component.

Then, the nominal winding losses at a given ripple condition can be expressed by:

$$P_{wL0} \approx ESR_{DC} \cdot \left(1 + \left(1 + k_{FrL} \cdot f_{Lhref}^2\right) \cdot \delta_{iLref}^2\right) \cdot I_{LN}^2$$

Where, P_{wL0} are the reference nominal winding losses of the inductor for the inductor nominal DC current (I_{LN}) with ripple component characterized by its reference effective frequency f_{Lhref} and a relative rms ripple current of $\delta_{iLref} = I_{LhN}/I_{LN}$. Good winding designs normally has a value of F_{rL} between 1.3 and 1.8 for the main/nominal operating frequencies, so it has been assumed that F_{rLref} is a reference parameter for the inductor technology:

$$F_{rLref} \approx \left(1 + k_{FrL} \cdot f_{Lhref}^2\right) \geq \frac{3}{2}$$

On the other hand, similarly to the overall volume and total weight, the nominal winding losses of the inductor can be roughly estimated as function of the inductor rated current and energy by:

$$P_{wL0} = k_{LPw0} \cdot I_{L.N}^{k_{LPwI0}} + k_{LPw1} \cdot E_L^{k_{LPwE}} \cdot I_{L.N}^{k_{LPwI1}}$$

Where, k_{LPw0}, k_{LPwI0}, k_{LPw1} k_{LPwE}, and k_{LPwI1} are the inductor meta-parameters for reference nominal winding loss estimation at reference ripple current conditions δ_{iLref} and f_{Lhref}.

Figure A- 20 shows the inductor reference nominal winding losses and winding losses to winding weight ratio versus inductor energy and inductor rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

With the reference nominal winding losses estimated, then the equivalent resistance can be approximated by:

$$ESR_{DC} \approx \frac{P_{wL0}}{\left(1 + F_{rLref} \cdot \delta_{iLref}^2\right) \cdot I_{LN}^2}$$

$$ESR_{AC} \approx ESR_{DC} \cdot \left(1 + \left(F_{rLref} - 1\right) \cdot \left(\frac{f_{Lh}}{f_{Lhref}}\right)^2\right)$$

For triangular current waveform with frequency f_{sw}, then the effective frequency (f_{Lh}) becomes [1]:

$$f_{Lh} = \frac{2 \cdot \sqrt{3}}{\pi} \cdot f_{sw}$$

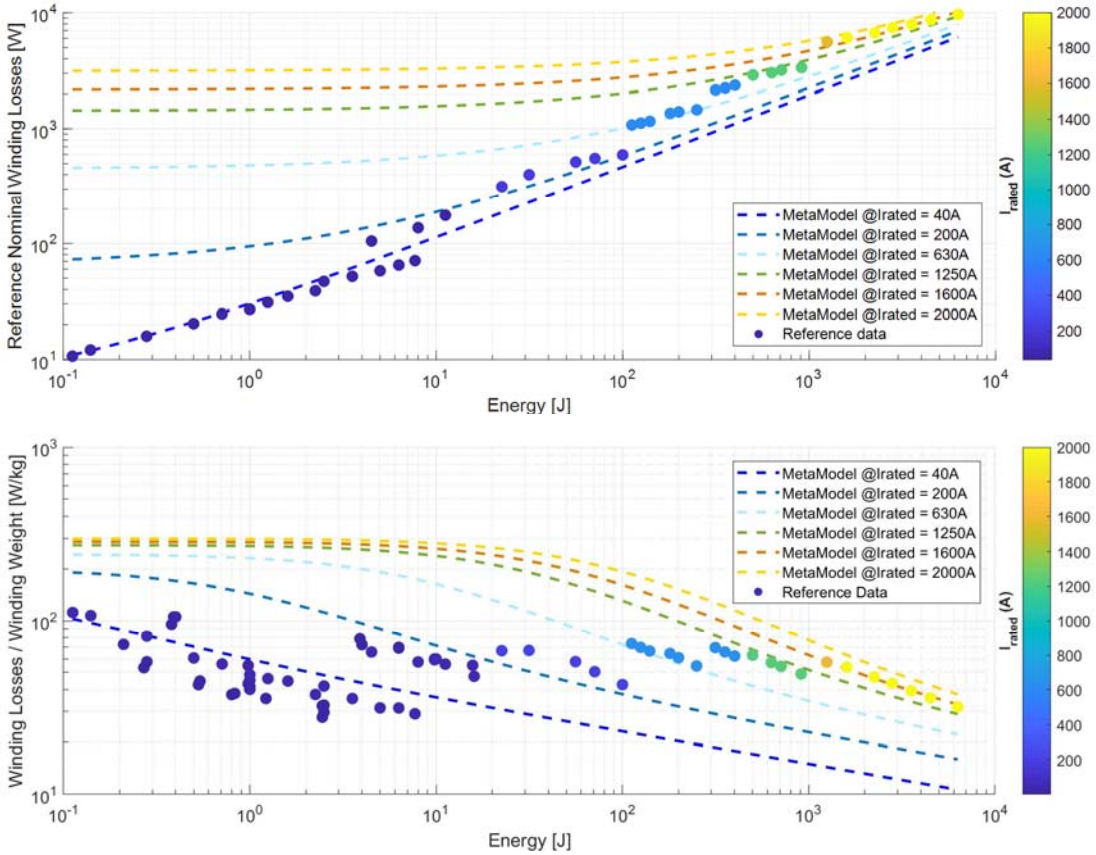

Figure A- 20 Inductor reference nominal winding losses and winding losses to winding weight ratio versus inductor energy and inductor rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer ($\delta_{iLref} = 0.3$ and $f_{Lhref} = 300$).

Core losses

The inductor core losses (P_{coreL}) can be evaluated based on the well-known Steinmetz equation, so for a DC inductor, P_{coreL} scale with the effective frequency (f_{Lh}) and the peak flux density (B_{Lhpeak}) associated to the current ripple:

$$P_{coreL} \propto {f_{Lh}}^{\alpha_L} \cdot B_{Lhpeak}^{\beta_L}$$

Where, α_L and β_L are the Steinmetz core loss parameters for the inductor magnetic core material.

For a given reference core nominal loss data (at given ripple conditions δ_{iLref} and f_{Lhref}), the reference core nominal loss (P_{coreL0}) can be estimated as function of the core weight (W_{cL}) by:

$$P_{coreL0} = k_{\rho c0} \cdot (W_{cL})^{k_{\rho cWc}}$$

Where $k_{\rho c0}$ and $k_{\rho cWc}$ are the inductor meta-parameters for core loss estimation. Figure A- 21 shows the inductor reference nominal core losses versus inductor core weight and rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

Finally, as the flux density is proportional to the ripple current [1], then the inductor core losses (P_{coreL}) can be estimated by:

$$\frac{P_{coreL}}{P_{coreL0}} = \left(\frac{f_{Lh}}{f_{Lhref}}\right)^{\alpha_L} \cdot \left(\frac{I_{LhPeak}}{\sqrt{2} \cdot \delta_{iLref} \cdot I_{L.N}}\right)^{\beta_L}$$

Where, I_{LhPeak} is the peak ripple current with effective frequency f_{Lh}, and P_{coreL0} are the reference core losses for the reference ripple conditions δ_{iLref} and f_{Lhref}.

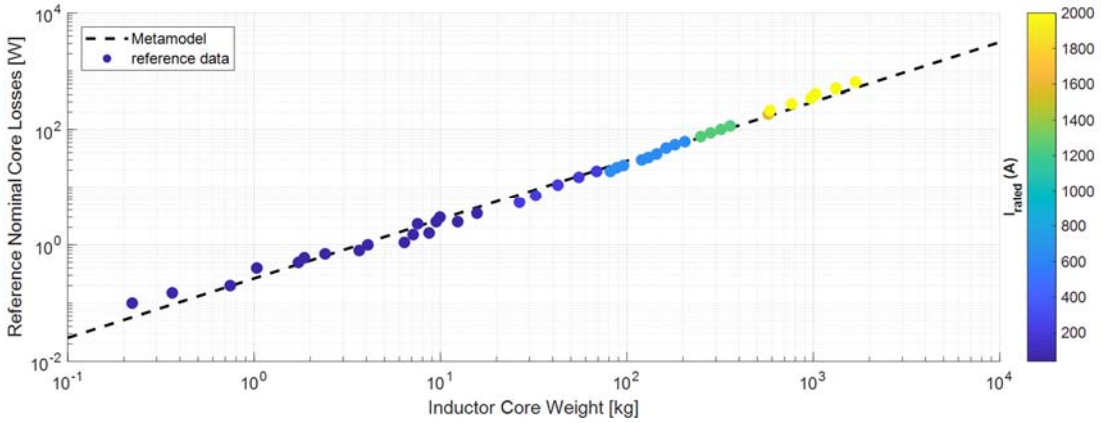

Figure A- 21 Inductor reference nominal core losses versus inductor core weight and rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer ($\delta_{iLref} = 0.3$ and $f_{Lhref} = 300$).

Inductor cost

The DC inductor cost can be estimated based on the model proposed in [19], briefly described here for the sake of completeness:

$$Cost_{Lstr} = \frac{1}{1 - \Xi_L} \cdot \left(\text{Cost}_{mat,L} + \text{Cost}_{lab,L}\right)$$

$$\text{Cost}_{mat,L} = \sigma_{core,L} \cdot W_{cL} + \sigma_{wdg,L} \cdot W_{wdg} + Cost_{mat0,L}$$

$$\text{Cost}_{lab,L} = \sigma_{lab,L} \cdot W_{wdg} + Cost_{lab0,L}$$

Where $\sigma_{core,L}$, $\sigma_{wdg,L}$ and $\sigma_{lab,L}$ are the specific cost per weight of the core and winding, which depends on the employed core and winding type; W_{cL}, W_{wdg} are the core and winding weight, respectively, $Cost_{mat0,L}$ and $Cost_{lab0,L}$ are fixed material and labour cost, and Ξ_L is the supplier gross margin.

For the considered reference inductor technology: $\sigma_{core,L} = 8\ €/kg$, $\sigma_{wdg,L} = 10\ €/kg$, $\sigma_{lab,L} = 7€/kg$, $Cost_{mat0,L} = 1€/unit$ and $Cost_{lab0,L} = 2€/unit$. A supplier gross margin of 25% has been assumed. Figure A- 22 shows the estimated inductor cost versus inductor energy and inductor rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

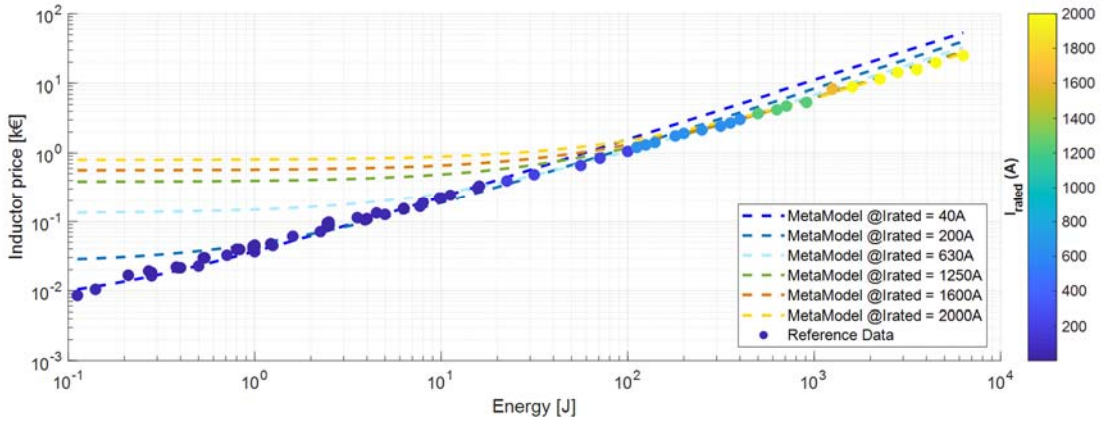

Figure A- 22 Inductor cost versus inductor energy and inductor rated current for the SIDAC iron-core smoothing reactors series 4EM & 4ET from Siemens manufacturer.

A.4 Heatsinks

The developed heatsink models aims to evaluate the performance of a heatsink technology as functions of two main inputs:

- The available device area to be cold down (A_{Base}).
- The required heatsink thermal resistance (R_{thHS})

Three heatsink alternatives has been considered within this work: natural convection heatsinks, air-forced heatsinks and a liquid-cooled cold plates.

A.4.1 Natural convection heatsinks

In this case an aluminium heatsink structure is placed on top of the device to be cold down and only natural convection applies, so the thermal resistance of the aluminium structure (R_{thN}) is the total heatsink thermal resistance ($R_{thHS} = R_{thN}$). Stamping and extrusion heatsink technologies have been considered.

The overall volume of the heatsink (Vol_{HS}) can be approximated to the volume of the aluminium structure (Vol_{HSN}), which can be estimated as function of its base area (A_{Base}) and its thermal resistance (R_{thN}) by:

$$Vol_{HS} = Vol_{HSN} = k_{HSNVol0} \cdot (A_{Base})^{k_{HSNVolA}} \cdot (R_{thN})^{k_{HSNVolR}}$$

Where $k_{HSNVol0}$, $k_{HSNVolA}$ and $k_{HSNVolR}$ are the aluminium structure meta-parameters for volume estimation of the considered aluminium structure technology.

Similarly to the volume, the heatsink cost ($Cost_{HS}$) can be approximated to the cost of the aluminium structure ($Cost_{HSN}$), which can be estimated as function of its base area (A_{Base}) and its thermal resistance (R_{thN}) by:

$$Cost_{HS} = Cost_{HSN} = k_{HSNCost0} \cdot (A_{Base})^{k_{HSNCostA}} \cdot (R_{thN})^{k_{HSNCostR}}$$

Where $k_{HSNCost0}$, $k_{HSNCostA}$ and $k_{HSNCostR}$ are the aluminium structure meta-parameters for cost estimation of the considered aluminium structure technology.

The heatsink weight is the weight of the aluminium structure, which can be estimated based on the average density of the aluminium structure (ρ_{HSN}) by:

$$Weight_{HS} = Weight_{HSN} = \rho_{HSN} \cdot Vol_{HSN}$$

The aluminium structure heatsink technology itself has limitations regarding the thermal resistance versus base area, as very low thermal resistances cannot be obtained for small base areas given physical constraints implicit in the technology. So, a validity range for the base area as function of thermal resistance has been considered, and it is estimated by:

$$A_{BaseMN} = k_{HSNAMN} \cdot (R_{thN})^{k_{HSNAR}}$$
$$A_{BaseMX} = k_{HSNAMX} \cdot (R_{thN})^{k_{HSNAR}}$$

Where k_{HSNAMN}, k_{HSNAMX} and k_{HSNAR} are the meta-parameters for base area and thermal resistance relationship of the considered technology.

A.4.2 Air-Forced Heatsink

In this case an aluminium heatsink structure with fan system is placed on top of the device. Stamping and extrusion heatsink technologies have been considered for the aluminium structures. Square tube axial 12Vdc fans have been considered as reference fan system technology.

The cost, overall volume, and weight of the air-forced heatsink are calculated as summation of the heatsink aluminium structure and fan system components, as follows:

$$Cost_{HS} = Cost_{HSN} + Cost_{HSFan}$$

$$Vol_{HS} = Vol_{HSN} + Vol_{HSFan}$$

$$Weight_{HS} = Weight_{HSN} + Weight_{HSFan}$$

The heatsink structure is modelled as in previous section, and the fan system is evaluated by:

$$Cost_{HSFan} = Cost_{HSFan0} + k_{HSFanCost0} \cdot (A_{Fan})^{k_{HSFanCostA}} \cdot (AFR_{FanMX})^{k_{HSFanCostAFR}}$$

$$Vol_{HSFan} = k_{HSFanVol0} \cdot (A_{Fan})^{k_{HSFanVolA}} \cdot (AFR_{FanMX})^{k_{HSVolAFR}}$$

$$Weight_{HSFan} = \rho_{HSFan} \cdot (Vol_{HSFan})^{k\_HSFanWV}$$

$$A_{Fan} \approx \frac{Vol_{HSN}}{\sqrt{A_{Base}}}$$
$$AFR_{FanMX} = 2 \cdot AFR_{HS}$$

A_{Fan}: Required fan area, which is the area where the air will flow through the heatsink structure. It is approximated considering a square base heatsink area ($A_{Base.HS}$)
AFR_{FanMX}: Maximum fan air flow rate, which is approximated to be twice the nominal air flow rate of the heatsink (AFR_{HS}).

The total heatsink thermal resistance can be evaluated by adding the thermal resistance of the base plate and the thermal resistance of the structure fins, which is a function of AFR_{HS}:

$$R_{thHS} = R_{thB} + \frac{R_{thN} - R_{thB}}{1 + k_{AFR} \cdot AFR_{HS}}$$

$$R_{thB} = \frac{\max\{k_{BFin} \cdot H_{HSFin},\ H_{HSBaseMN}\}}{\kappa_{AL} \cdot A_{Base}}$$

$$H_{HSFin} \approx \frac{Vol_{HSN}}{A_{Base}}$$

A.4.3 Cold Plates

In this case a cold plate is placed on top of the device to be cold down. Different cold plates technologies have been considered.
The cost, overall volume, and weight of the heatsink are calculated as follows:

$$Cost_{HS} = Cost_{CPi} = Cost_{CPC0} + \frac{k_{CPC0} \cdot Vol_{CPi}^{k_{CPCV}} \cdot WFR_{CP}^{k_{CPCFR}}}{R_{thCPi}^{k_{CPCR}}}$$

$$Vol_{HS} = Vol_{CPi} = A_{Base} \cdot t_{CP}$$

$$Weight_{HS} = Weight_{CPi} = k_{CPM0} \cdot Vol_{CPi}^{k_{CPMV}}$$

$$R_{thHS} = R_{thCPi} = \frac{K_{CPR0}}{A_{Base}^{k_{CPRA}} \cdot t_{CP}^{k_{CPRt}} \cdot WFR_{CP}^{k_{CPRFR}}}$$

$$A_{BCPiMN} \leq A_{Base} \leq A_{BCPiMX}$$

Table A- 4 summarizes the cold plate meta-models and found meta-parameters for the considered technologies.

Table A- 4 Cold Plate Meta-model and meta-parameters

Reference Technologies	
Manufacturer	***Series***
Solid State Cooling Systems	LC, LCW, LFLC and HFLC
Wakefield-vette	1204xx, 1209xx, and 180-xx
Aavid, Thermal Division of Boyd Corporation	Hi-Contact
Advanced Thermal Solutions Inc.	ATS-CP and ATS-TCP
Ohmite	CP

Meta-Models			
	Input [units]	***Meta-parameter***	***value***
Thermal Resistance [°C/W]: $R_{thCP} = \frac{K_{CPR0}}{A_{BCP}^{k_{CPRA}} \cdot t_{CP}^{k_{CPRt}} \cdot V_{FR}^{k_{CPRFR}}}$	A_{BCP}: Base Area [m2] t_{CP}:Plate thickness [m] V_{FR}: Flow Rate [dm3/min]	k_{CPR0} k_{CPRA} k_{CPRt} k_{CPRFR}	1.9683e-6 0.5364 1.8718 0.4336
Cold plate Volume [m3] $Vol_{CP} = A_{BCP} \cdot t_{CP}$	A_{BCP}: Base Area [m2] t_{CP}:Plate thickness [m]	--	--
Cold plate Weight [kg] $Mass_{CP} = k_{CPM0} \cdot Vol_{CP}^{k_{CPMV}}$	Vol_{CP}: Volume [m3]	k_{CPM0} k_{CPMV}	15.0475 0.3263
Cold Plate Price [EUR] $Cost_{CP} = Cost_{CPC0} + \frac{k_{CPC0} \cdot Vol_{CP}^{k_{CPCV}} \cdot V_{FR}^{k_{CPCFR}}}{R_{thCP}^{k_{CPCR}}}$	Vol_{CP}: Volume [m3] R_{thCP}[°C/W] V_{FR}: Flow Rate [dm3/min]	$Cost_{CPC0}$ k_{CPC0} k_{CPCV} k_{CPCR} k_{CPCFR}	5 8.0635 0.1766 0.4836 0.4722
Min.-Max. Water Flow Rate $V_{FR.Min} = k_{CPFR0MN} \cdot t_{CP}^{k_{CPFRt}}$ $V_{FR.Max} = k_{CPFR0MX} \cdot t_{CP}^{k_{CPFRt}}$	t_{CP}:Plate thickness [m]	$k_{CPFR0MN}$ $k_{CPFR0MX}$ k_{CPFRt}	3.7208e4 4.4649e5 2.4086

Constraints		
Input variable	***Minimum***	***Maximum***
t_{CP}: Cold plate thickness	10 mm	35 mm
A_{BCP}:Cold plate base area	10 cm2	3000 cm2
V_{FR}: Water flow rate	$V_{FR.Min}$	$V_{FR.Max}$

A.4.4 Heatsink technologies comparison

Figure A- 23 to Figure A- 26 shows the heatsink performance comparison for the considered heatsink technologies within this work. Reference heatsink data along with the evaluated proposed meta-models are plotted.

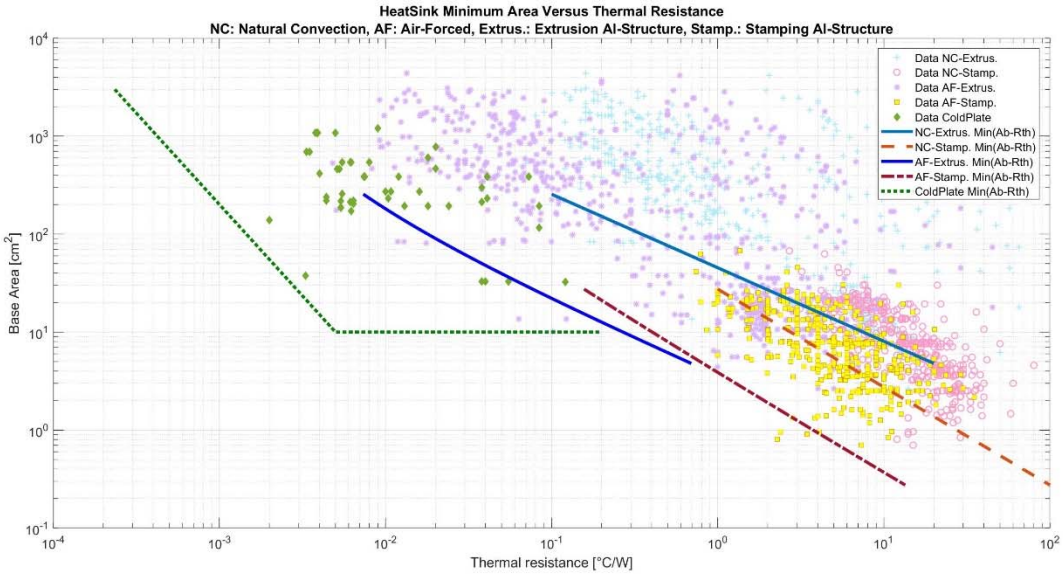

Figure A- 23 Heatsink base area versus thermal resistance for different heatsink technologies. Reference data along with the evaluated meta-models.

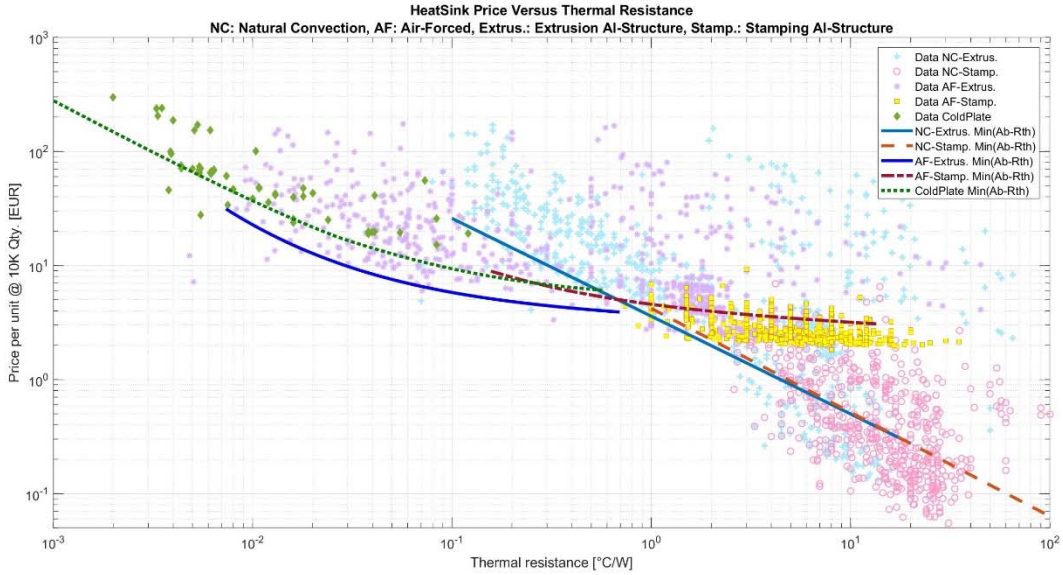

Figure A- 24 Heatsink price versus heatsink thermal resistance for different heatsink technologies. Reference data along with the evaluated meta-models.

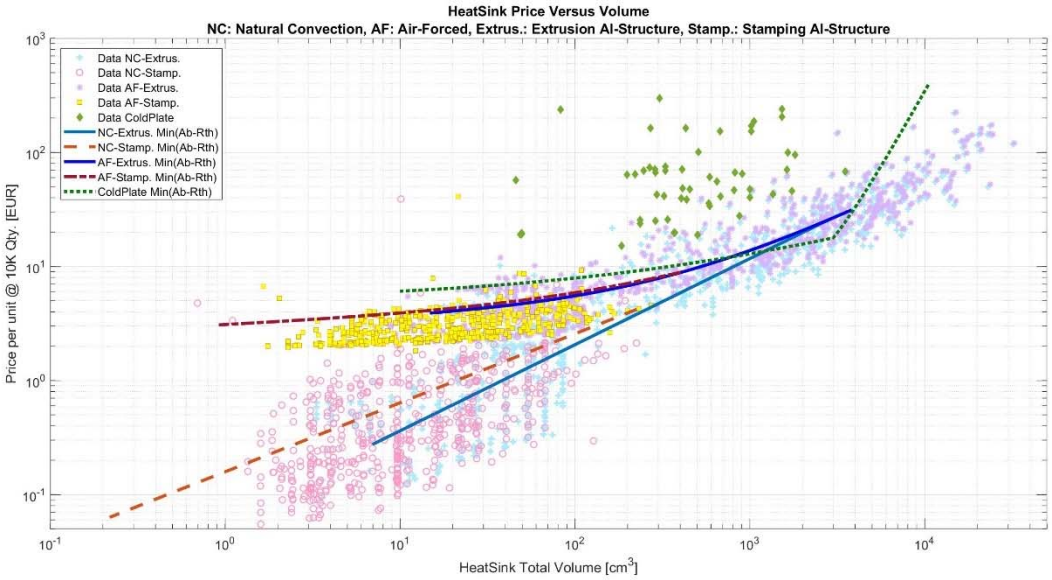

Figure A- 25 Heatsink price versus Heatsink overall volume for different heatsink technologies. Reference data along with the evaluated meta-models.

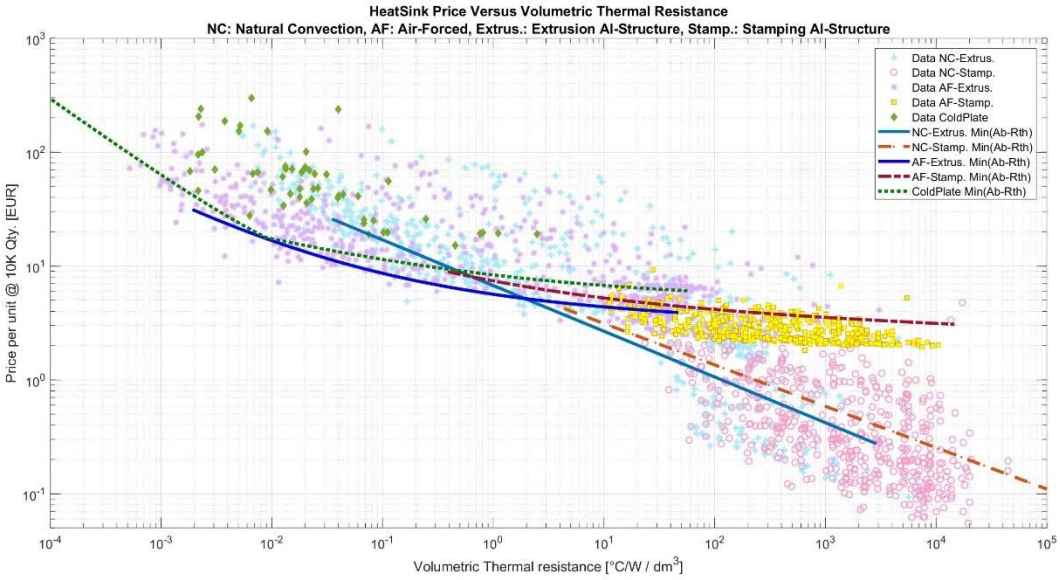

Figure A- 26 Heatsink price versus volumetric thermal resistance for different heatsink technologies. Reference data along with the evaluated meta-models

B Water cooling system based on microchannel cold plates.

This cooling system, also commonly name as "jacket cooling", is composed by two main components: the microchannel cold plates and the thermal pads (interfacing the battery cells and microchannel cold plates). The core element of this cooling system is the microchannel cold plate. An illustrative example of a pouch cell with microchannel cold plate is shown in Figure B-1 as reported in [12, 13]. Figure B-2 shows a simplified thermal model for the water-cooling system based on microchannel cold plates. The average thermal resistance of the microchannel cold plate cooling system ($R_{thHS.\mu CP}$) can be estimated as follows:

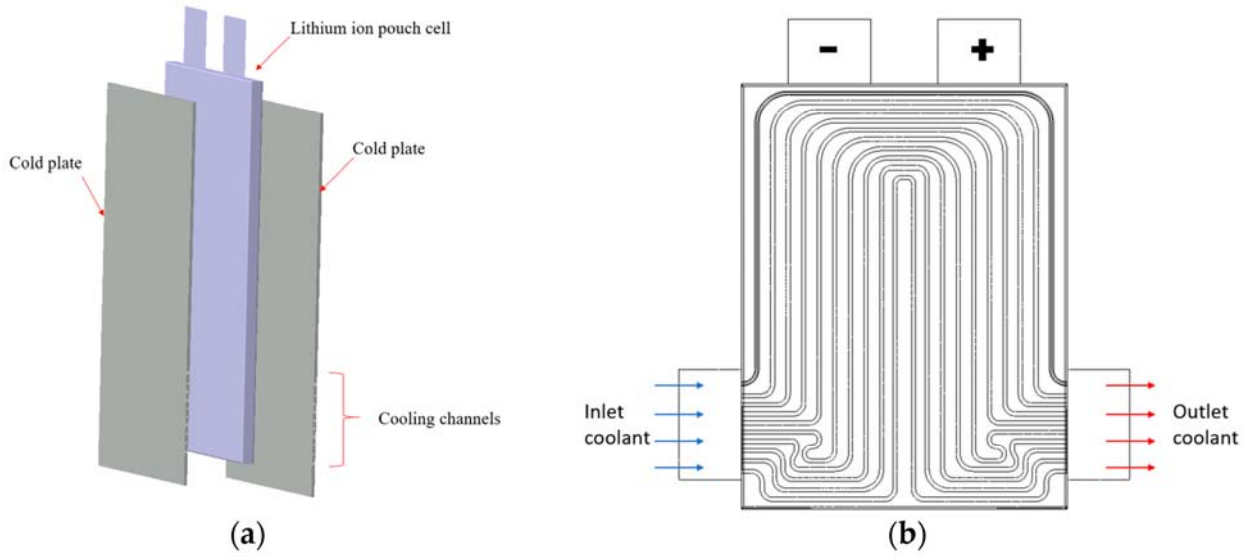

Figure B-1 Exemplary geometry of pouch cell with microchannel cold plate. Figure taken from [12]

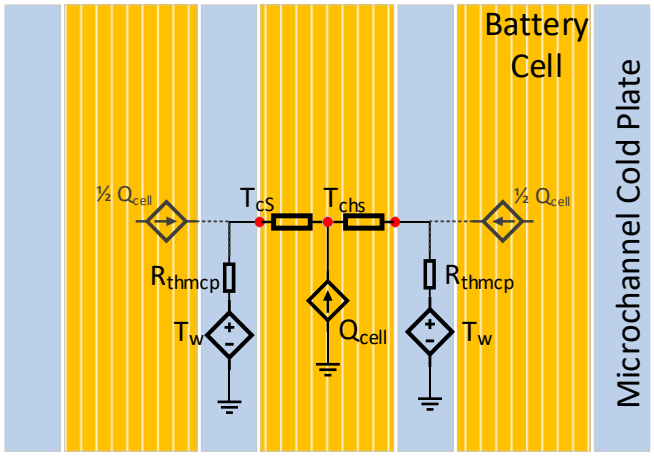

Figure B-2 Simplified thermal model for battery module with microchannel cold plates.

$$R_{thHS.\mu CP} = R_{thCellx} + R_{thTP} + R_{th\mu CP}$$

where $R_{thCellx}$is the in-plane cell thermal resistance (from centre of the cell to the cell surface), R_{thTP} is the thermal pad thermal resistance and $R_{th\mu CP}$ is the microchannel cold plate thermal resistance (double side cooling). $R_{thCellx}$ and R_{thTP} are defined as in section 3.4.
The microchannel cold plate thermal resistance can be estimated based on the effective head transfer coefficient (h_{eff}) of the microchannel cold plate base surface ($A_{B\mu CP}$):

$$R_{th\mu CP} = \frac{1}{L_{cell} \cdot W_{Cell} \cdot k_{he\mu 0} \cdot V_w^{k_{he\mu 1}}}$$

where $k_{he\mu 0}$ and $k_{he\mu 1}$are proportionality regression coefficients found by taking data from the reference microchannel cold plate technology and V_w is the inlet water flow speed (m/s). Table B- 1 presents the considered microchannel cold plate parameters.

Table B- 1 Microchannel cold plate parameters

	Parameter	Value
Thermal Pad Reference material: H48-6 / TG-AH486 @ T-Global Technology	Thermal Conductivity [W/mK]	3.4
	Thickness [mm]	0.3
	Density [kg/m3]	2420
	Cost density ($Cost_{TP1}$) [EUR/kg]	30
Microchannel Cold Plate Reference Technology: • Low flow LC @ Solid State Cooling Systems • Geometry and performance as in [13] [12].	Effective head transfer coefficients	$k_{he\mu 0} = 347.72$ $k_{he\mu 1} = 0.2136$
	Thickness [mm]	1.7
	Water Flow speed [mm/s]	4.5 Range {1, 7.5}
	Density [kg/m3]	2011.7
	Inlet/outlet duct cross-sectional area [cm2] (10*1.3mmx3mm)	0.39
	Cost density ($Cost_{CP1}$) [EUR/kg]	61
	Cost per unit ($Cost_{CP0}$) [EUR]	57

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