A Novel Scalable Decision Tree Implementation on SoC Based FPGAs

MOSTAFA KORAEI, SINTEF AS, Norway

PETTER LEFOKA, Mantena AS, Norway

Machine learning algorithms are rapidly growing in predictive maintenance and condition monitoring systems for valuable assets. Decision tree classification (DTC) is one of popular methods in condition monitoring systems based on vibration analysis. Due to big amount of data coming out from vibration sensors, the processing should be done on edge close to the sensors. DTC can reach high accuracy but at the same time it is computationally intensive and edge processors are not able to run it so fast. There are some FPGA implementation that work fine for small datasets but have issues when there is a real big dataset that needs deep trees. In this paper we introduce our new method of Decision Tree (DT) implementation on SoC based FPGAs. We have shown that using a combination of FPGA and processor, the DT can be implemented much faster and more scalable for trees with depth up to 50. We have used Vivado HLS to implement our DTs and connected them to the processor of SoC via AXI interfaces. We have shown that our implementation gains up to 2.27x speed up comparing with only software implementation.

CCS Concepts: • **Computer systems organization** → **Embedded systems**; *Redundancy*; Robotics; • **Networks** → Network reliability.

Additional Key Words and Phrases: Decision trees, FPGA, Predictive maintenance, HLS

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1 INTRODUCTION

The rising cost of maintaining expensive assets and increasing demand for more running time and lower unexpected failure in different industries, implies request for more robust and reliable maintenance approaches [1, 2, 16]. Recent years witness the rapid development in using Machine Learning methods for predictive and condition based maintenance [2, 5, 8, 10]. Vibration analysis has become a reliable and important method for monitoring rotating machines because the vibration signal is a fundamental parameter and is varying based on structure of the machine, its working conditions and potential damages [5, 8]. Run time vibration spectrum of a big machine contains lots of information about the health condition of the machine in general and specifically about the components that are located close to the sensor [5, 11].

Different faults in a rotating machinery are induced due to the multiple parameters involved that may be related to load condition of the machine, undeniable tolerance limits provide while fitting the rolling bearing elements in the rotating machinery, age of the machine, inadequate lubrication and even environmental conditions.

Many of mechanical defects can be found before result in a major failure by interpreting the spectrum of the vibration sensors. There are some analytical method for calculating the frequency characteristics of a healthy machine and

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for different potential failures of a specific machine[11] [12] and [6]. The frequency characteristics obtained by the analytical method represent the fundamental frequencies for the different moving parts in a machine. In addition of the main fundamental frequencies, we should consider various harmonics range of the frequencies at different speed and also for the different conditions[3, 6]. While this amount of information needs expert engineers for analysing and diagnosing the machine condition, some industries have tens and hundreds instances of one asset that need need to be maintained. For many industries with expensive assets like wind turbines, gas turbines and train bogies, it is almost not feasible to interpret data that comes from different instances by human experts continuously.

Decision tree classifiers (DTC) are one of popular machine learning techniques in vibration analysis for predictive maintenance systems[15] and [4]. Different studies has shown that decision trees perform well in condition classification of machines based on vibration analysis[1] , [7] and [9]. Some studies like [13] show that decision tree algorithm is able to classify planetary gearboxes vibration data, resulting in 99,74% accuracy on the test dataset. This technique aims to extract knowledge from real time with combination of historical data of the machine. Decision trees are computing intensive algorithms[17] and [14] and when it comes to predictive maintenance and vibration analysis with tens of parameters and deep trees they even need more computing resources. Decision trees have been attractive for many researchers with software and hardware field of interest [2] and [9] and [10].

For some applications it is possible to transfer data to a modern PC and run the model there, then this computing intensive is not a critical bottleneck for using decision tree classifiers in practice. However, vibration sensors have one of widest band width in industrial sensors from few KHz to tens of KHz in most of applications, it is very important to process the data on edge rather than sending it to cloud or on premise infrastructures in a central office. The reason is not only reducing the communication band width but in some applications like on train bogies, energy consumption is also important and the device is supposed to work on batteries for years. Many works have been done on accelerating decision trees on FPGA to reduce the power consumption and CPU frequency but the problem is with direct implementation a practical tree with depth of 30 to 100 needs a big amount of FPGA resources. More resource requirement results in bigger and more expensive FPGA.

In this work, we study the use of SoC based FPGA (Zynq7015) modules from Trenz Electronics to accelerate a decision tree classifiers for edge computing applications. Deep trees are usually computing-bound and increasing the number of features and data dimension makes them memory-bound as well. In this paper we propose a novel flexible implementation of decision trees in SoC that uses FPGA resources for the partial tree implementation and a state machine in the processor of the SoC for controlling the dataflow and configuration of each partition of the tree. While our contribution is introducing a novel hardware architecture for acceleration of decision trees on FPGA we have shown that performance is 2.27x higher than CPU implementation.

2 RESULTS

In Table 1 we see the resource utilization for different partial trees. We have assigned 9 percent of DSP blocks for FFT core and because of that cannot use more than 90 percent of available DSP slices on the FPGA. Due to this lack of resources we limited the depth of our partial decision trees to 9. Table 1 shows the resource utilization for different partial decision trees with depth of 4 to 9.

We have also implemented each main decision tree model in software and used the execution time of the software as the base line to compare our new FPGA implementation with it. As this figure shows, we gain better speedup until we have partial decision tree with depth of 7 then the speed up saturates or even being decreased. The main reason for this

Table 1. Resource utilization of different partial decision trees in percentage of available resources on the FPGA

Partial Tree Depth	Logic Cells %	Block RAMs %	DSP Slices %
4	11	0	6
5	13	1	10
6	16	4	18
7	24	9	29
8	42	20	51
9	78	34	86

issue is the saturating in the FPGA resources. According to Table 1 the DSP slices and logic cells utilization is more than 70 percent when we have a partial tree with depth of 9. This numbers would even make more sense when we know that we need 9 percent of DSP slices and 18 percent of logic cells for FFT core and peripheral interfaces like ADC drivers. Because of this the maximum frequency that the logic can work drops and instead of having more efficient hardware implementation but because of lower frequency that the whole hardware can work on it, we have a reduction in speed up.

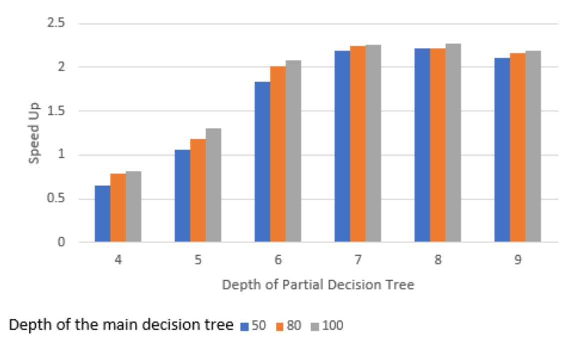

Fig. 1. The speed up comparison between different partial decision tree depth for different decision tree models.

Another interesting point in the Figure 1 is that the speed up is increased by using deeper decision tree. It makes sense because with bigger trees need more partial trees to cover and it results in lower percentage of software overhead on the performance.

3 CONCLUSION

In this paper we have introduced a new method for implementing deep decision trees on SoC based FPGAs by using partial decision trees on hardware and controlling it by software that is implemented in the processor side of the SoC. We have used our method for a predictive maintenance system that is designed to determine health condition of train bogies and tested the system with real accelerometer data and collected data by an industrial test bench. The results show that we have managed to gain 2.11x to 2.27x speed up for trees with depth of 50, 80 and 100 comparing to software implementation. We have used a small SoC for this project and the results show that the system is computing bond now and can gain even more speed up if we use bigger SoC.

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