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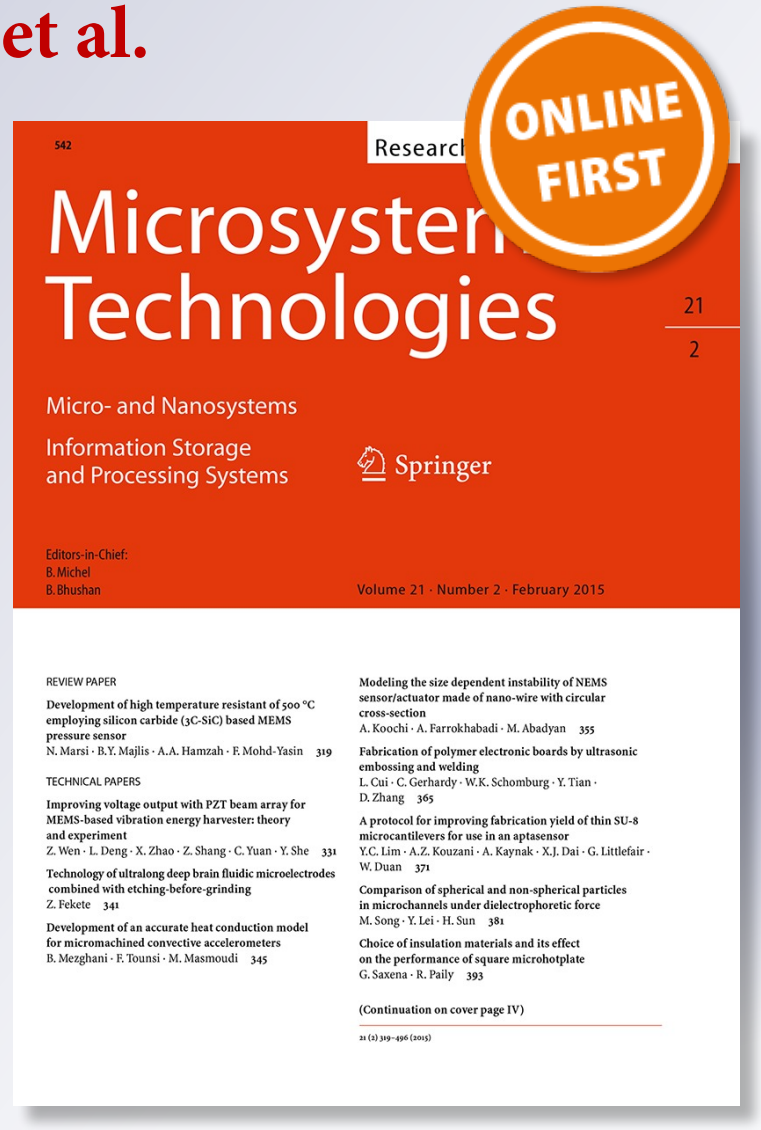

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TECHNICAL PAPER

Conductivity of high-temperature annealed silicon direct wafer bonds

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Abstract Silicon direct wafer bonding is a process with many application areas. Depending on the application, perfect insulation or negligible resistance is desired across the bonded interface. We have investigated the resistivity of hydrophilic high-temperature silicon direct wafer bonds by measuring the resistance across bonded frames suitable for device encapsulation. Frame widths of 100, 200, and 400 μm were fabricated. Hydrophilic pre-bonded laminates resulted in strong bonds and a dicing yield above 89 % for frame widths of 200 μm or wider. The average resistance of dies from boron implanted laminates was 0.35–0.44 Ω, and the average resistance of dies from un-implanted laminates was 0.51–0.68 Ω. All resistances were independent of the bonding area, showing that the resistance of the bonded interface was negligible. Dies from boron implanted wafers had good Al–Si contacts and lower standard deviation of the resistance, indicating that the implantation improved the reliability of the electrical contacts. In the case of boron implanted laminates, the low resistance is explained by a discontinuous SiO_2 and areas with continuous silicon lattice at the bonded interface. The results show that the oxide formed during silicon–silicon direct wafer bonding is broken up during bond annealing for 2 h at 1,050 °C, forming electrical connections of high quality between the two bonded wafers.

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1 Introduction

Silicon direct wafer bonding (SDWB) is a process with many application areas. According to Plössl and Krauter (1999), the four most commercially important are the fabrication of silicon on insulator (SOI) wafer material, power electronics, high-brightness light emitting diodes, and micromechanical devices. There are high-temperature and low-temperature, hydrophilic and hydrophobic SDWB processes. All four process types have been extensively studied (Ljungberg et al. 1994; Plössl and Kräuter 1999; Reiche and Gösele 2012; Wiemer et al. 2012). In hydrophobic bonds, the two silicon lattices are in contact (Reiche 2006). Wafer bonding of hydrophilic surfaces result in the presence of an oxide interfacial layer (Reiche 2006). Usually the oxide layer is 3–4 nm thick at room temperature or moderate temperature (Plössl and Kräuter 1999). After annealing the sample at temperatures above 1,000 °C, the layer thickness decreases to 2–2.5 nm (Plössl and Kräuter 1999; Reiche 2006).

Depending on the application, the electrical conductivity across the bonded interface may be of high importance. Some applications require negligible resistance and ohmic behavior of the bonded interface. Other applications need the bonded interface to be electrically isolating. Therefore, a number of studies address the question of the silicon oxide interphase stability (Wolstenholme et al. 1987; Ahn et al. 1990). These studies indicate that oxide layers of 1.5–2 nm were broken up during thermal annealing for 10 min at temperatures above 950 °C. By longer annealing times and higher annealing temperatures, oxide spheroidization occurred, creating islands or spheres with dimensions around 4–5 nm. The oxide break-up resulted in areas where the silicon lattices were in direct contact.

Charge transport across the bonded interface has been investigated for hydrophilic and hydrophobic SDWB. It has

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been hypothesized that charged electronics levels at or in the interface cause potential barriers that restrict the charge transport across the bonded interface (Plössl and Kräuter 1999; Bengtsson 1992). Bengtsson and Engström (1989) observed hydrophobic bonded interfaces to have ohmic behavior and low resistance, while hydrophilic bonded interfaces had nonlinear I–V curves and higher resistance. Kub et al. (1998) confirmed ohmic behavior and no potential barrier of hydrophobic bonded wafer interfaces. Contrasting the results of Bengtsson and Engström (1989), Shimbo et al. (1986) observed ohmic behavior and an interface resistivity below 10^{-6} Ω/cm^2 of hydrophilic bonded p-type wafers. Transmission electron microscopy showed lattice continuity across the interface similar to that obtained by epitaxial growth (Shimbo et al. 1986).

We have explored hydrophilic high-temperature SDWB devices with respect to electrical conductivity across the bonded interface on a sample set consisting of more than 150 individual samples. The electrical properties of wafer laminates with and without an original oxide interfacial layer are investigated and the effect of p-type implantation on the resistance is reported. Processes with high yield, giving strong bonds with low electrical resistance and ohmic behavior are identified.

2 Design

A test design with four different frame structures was made. The frames were suitable for enclosing a generic MEMS device, with an outer dimension of 3 × 3 mm^2 and frame widths of 100, 200, and 400 µm. Frames of all three widths had straight corners. One frame structure of width 200 µm with rounded corners was also designed. In addition to the frames, other structures were included to increase the total bond area of the wafer to 38 % of the wafer area. The design of the four frame structures and the test wafer is illustrated in Fig. 1, while the design dimensions and number of chips per wafer are listed in Table 1.

3 Experimental

We used 14 wafers of diameter 150 mm, thickness 300 µm, p-type, and with resistivity 0.01–0.02 Ωcm. Seven wafers were used as bottom wafers, and 7 wafers were prepared as top wafers. The top wafers were oxidized to a nominal thickness of 750 nm. The bonding pattern was defined by deep reactive ion etching, using the SiO_2 as masking material. After etching, the bonding structures protruded 6 µm above the remaining Si surface. Die identifying marks and dicing marks were made on the other side of the wafers.

Two top wafers and two bottom wafers were boron implanted on both sides applying a dose of 2 × 10^{15} cm^{-2}. The implants were activated by a furnace process at 900 °C for 60 min in N_2 ambient. One of the bottom wafers was thermally oxidized to a nominal thickness of 60 nm. The wafer pairs were prepared for hydrophilic bonding. The wafers were cleaned in piranha for 15 min, rinsed in

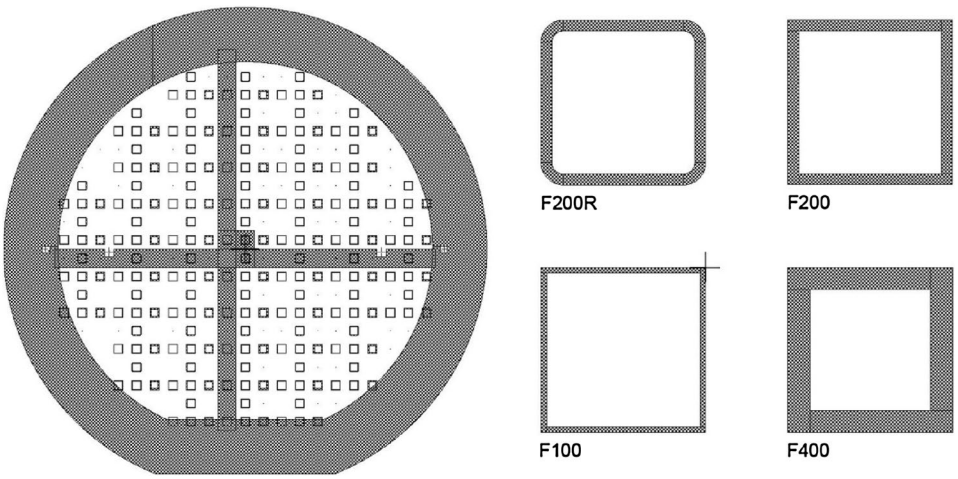

Fig. 1 *Left* layout of the test wafer. *Right* design of the four test frames. *Grey area* is the protruding bond area

Table 1 Overview of frame dimensions and number of dies on wafer

Die name	Description	No. of dies on wafer	Area [mm^2]
F100	Square frame, straight corners, width 100 µm	37	1.16
F200	Square frame, straight corners, width 200 µm	50	2.24
F200R	Square frame, rounded corners, width 200 µm	47	2.14
F400	Square frame, straight corners, width 400 µm	46	4.16

Table 2 Overview of bonded laminates

Wafer ID	Implanted (cm^{-2})	Bond SiO_2 (nm)	Pre-bonding treatment
I-1	No	No	Hydrophilic
I-2	No	No	Hydrophilic
I-3	No	No	Hydrophilic
I-4	No	No	Hydrophilic
I_Oxide-1	No	60	Hydrophilic
I_Boron-1	2×10^{15}	No	Hydrophilic
I_Boron-2	2×10^{15}	No	Hydrophilic

de-ionized water (DIW) for 15 min, rendered hydrophilic in RCA-1 for 10 min, rinsed in DIW, and spin-dried.

Stacks of one top wafer and one bottom wafer were bonded together in an SB6e wafer bonder (Suss) applying a tool pressure of 350 mbar for 2 min at an ambient temperature of 50 °C and a bond chamber pressure below 5×10^{-3} mbar. The bonding was performed less than 2 h after the hydrophilization. The bonded laminates were left overnight before cleaning in RCA-1 and RCA-2 and bond annealing for 2 h at 1,050 °C in N_2 ambient. A 0.8 µm thick Aluminum layer was sputter deposited on both sides of the laminates and patterned on one side to realize electrical contacts. The contacts were sintered for 30 min at 350 °C in forming gas. Finally, the laminates were diced into individual dies of 6×6 mm^2, each containing one frame structure. Table 2 shows an overview of the bonded laminates, and Fig. 2 shows the cross-section of the three types of bonded dies.

The quality of the bond was monitored by infrared photography before and after bond annealing. Electrical measurements were done before dicing and on a minimum of ten individual dice after dicing. After dicing, the dicing yield was noted, defined as the percentage of dies that did not delaminate during dicing. The electrical measurement on individual dies was done by the four-point probe method. A specified current was applied across the die by two probes connected to a 2,635 System Sourcemeter (Keithley). The resulting voltage was recorded by two different probes, connected to a 2,120 Digit Sourcemeter (Keithley). On the dies from laminates I-1, I-2, I-3, I_Boron-1, and I_Boron-2, the current range was from minus 100 mA to 100 mA. For these dies, the resistance through the bonds was calculated as $\partial V/\partial I$ at the value $I = 50$ mA. For dies with no measurable conductivity, the capacitance between the two metal contacts was measured, using a measurement frequency of 1 kHz. The breakdown voltage was measured on selected dies. The cross-sections of three different dies were investigated by transmission electron microscopy (TEM) to identify the presence and thickness of SiO_2 at the bonded interface. The bond strength was measured by pull testing of bonded dies. The bond strength results have been presented by Schjølberg-Henriksen et al. (2014).

4 Results

An infrared photograph of bonded implanted laminate I_Boron-1 directly after bonding is shown in Fig. 3. The bond quality appeared to be good.

The dicing yield is plotted in Fig. 4 and shows that frames of design F100 had significantly lower yield than frames of width 200 and 400 µm. The dicing yield of laminate I-4 was significantly lower than the yield of the other six laminates. The infrared photograph of laminate I-4 revealed an un-bonded quarter wafer. The yield of dies with frame width of 200 and 400 µm, excluding laminate I-4, was between 89.1 % and 100 %.

The electrical measurements before dicing revealed that laminate I-4 had poor electrical contact between the Silicon and the Al metal. A typical I–V curve from laminate I-4 is shown in Fig. 5. Measurements from this laminate were therefore excluded from our sample set. Figure 6 shows typical I–V curves from dies of design F200 from the laminates I-1, I-2, I-3, I_Boron-1, and I_Boron-2. All dies had linear I–V curves, showing ohmic behavior. The average resistances, calculated from ten dice of each design, are plotted in

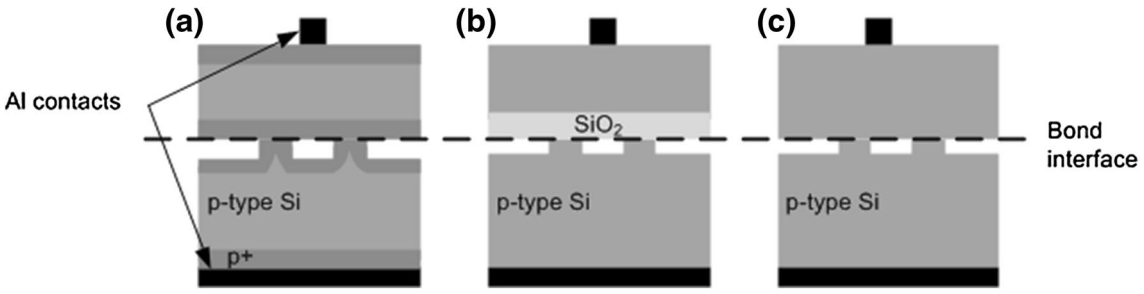

Fig. 2 Cross-sectional sketches of dies. **a** Die with boron implantation (e.g. wafer I_Boron-1). **b** Die with bonding oxide (e.g. wafer I_Oxide-1). **c** Die without implantation and bonding oxide (e.g. wafer I-1)

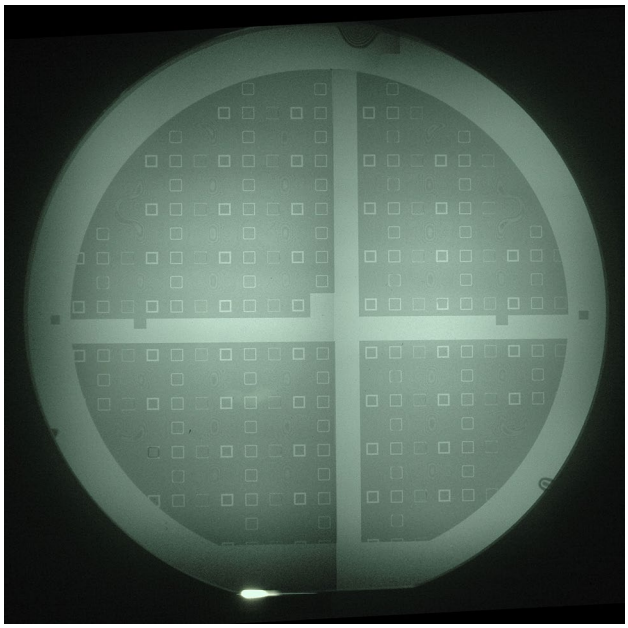

Fig. 3 Infrared photograph of laminate I_Boron-1, which appears to be of good bond quality

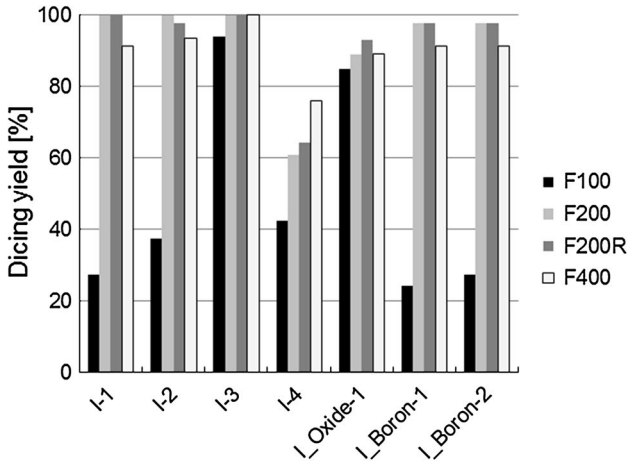

Fig. 4 Dicing yield of the four different frame designs of the seven laminates

Fig. 7 and the values are listed in Table 3. Dies from laminates I_Boron-1 and I_Boron-2 had slightly lower resistance than the ones from the non-implanted laminates I-1, I-2, and I-3. The standard deviation was also lower in the sample sets from implanted laminates. The theoretical resistance was calculated from the wafer resistivity and the average contact area as resistor cross-section. The average contact area of the top wafer is (0.13 mm^2 + bond area)/2 and the average contact area of the bottom wafer is (36 mm^2 + bond area)/2. Using the bond areas of frames F100 and F400 and the two extreme values of material resistivity results in a theoretical

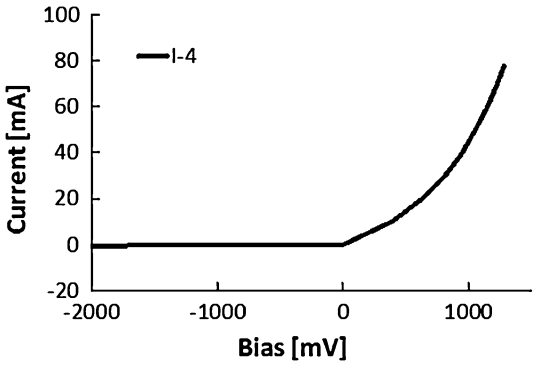

Fig. 5 Typical I–V curve recorded from laminate I-4

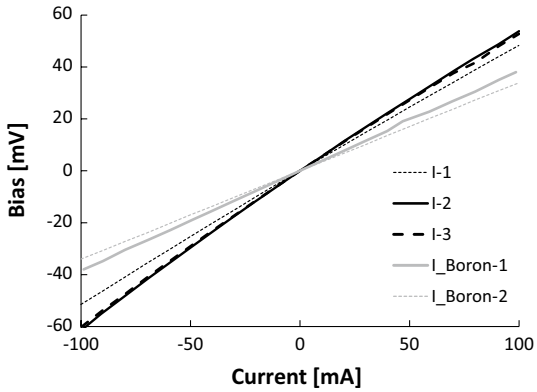

Fig. 6 Typical current–voltage plots for frames of design F200 from each of the five laminates I-1, I-2, I-3, I_Boron-1 and I_Boron-2. *Black lines* are un-implanted laminates and *grey lines* are boron implanted laminates. All dies had linear, ohmic behaviour

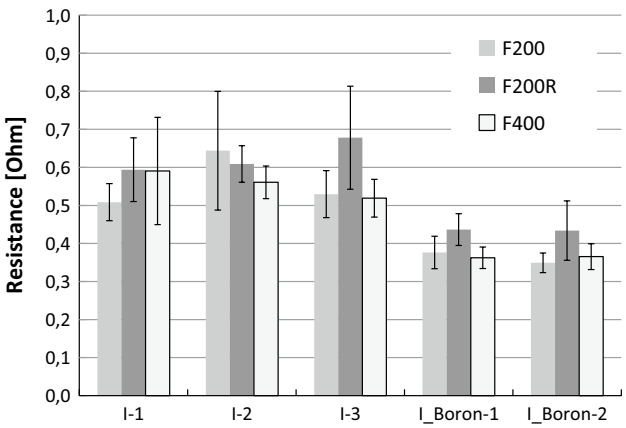

Fig. 7 The average and standard deviation of the measured resistance between the two metal contacts on the dies. Ten dice from each laminate and design were measured

resistance between 0.02 and 0.1 Ω. For the five laminates I-1, I-2, I-3, I_Boron-1, and I_Boron-2, there was no significant difference between I–V curves with respect to frame

Table 3 Average values and standard deviation of the resistance as plotted in Fig. 7

Wafer	Resistance (Ohm) F200	Resistance (Ohm) F200R	Resistance (Ohm) F400
I-1	0.51 ± 0.05	0.59 ± 0.08	0.59 ± 0.14
I-2	0.64 ± 0.16	0.61 ± 0.05	0.56 ± 0.04
I-3	0.53 ± 0.06	0.68 ± 0.14	0.52 ± 0.05
I_Boron-1	0.38 ± 0.04	0.44 ± 0.04	0.36 ± 0.03
I_Boron-2	0.35 ± 0.03	0.43 ± 0.08	0.37 ± 0.03

Ten dice of each design were measured on each wafer

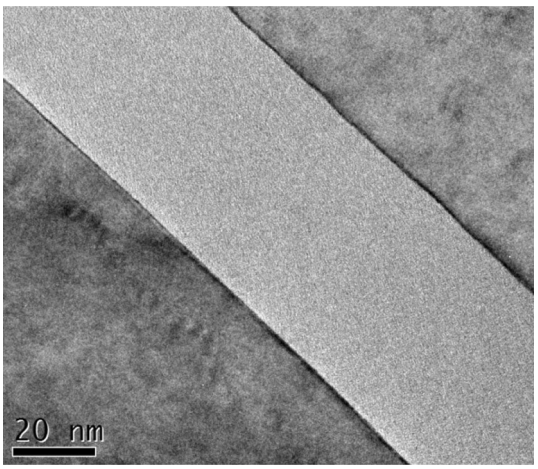

Fig. 8 TEM cross-section of the bond interface of a die from laminate I_Oxide-1. A continuous SiO_2 layer of thickness around 53 nm is seen between the two silicon wafers

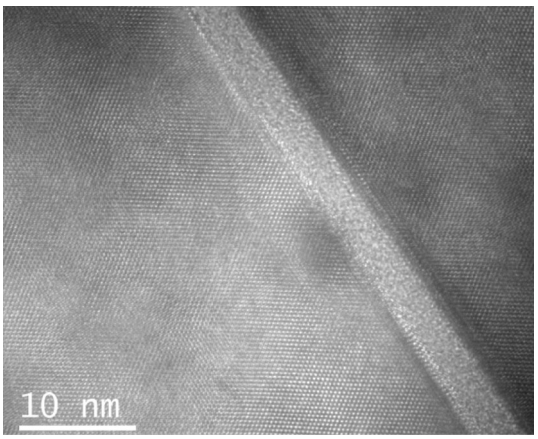

Fig. 9 TEM cross-section of the bond interface of a die from laminate I-3. A continuous SiO_2 layer of thickness around 4 nm is seen between the two silicon wafers

design. The maximum current density occurred on the F200 dies, and was 4.0×10^4 A/m^2 for the un-implanted dies and 6.2×10^4 A/m^2 for the implanted dies at 50 mV bias.

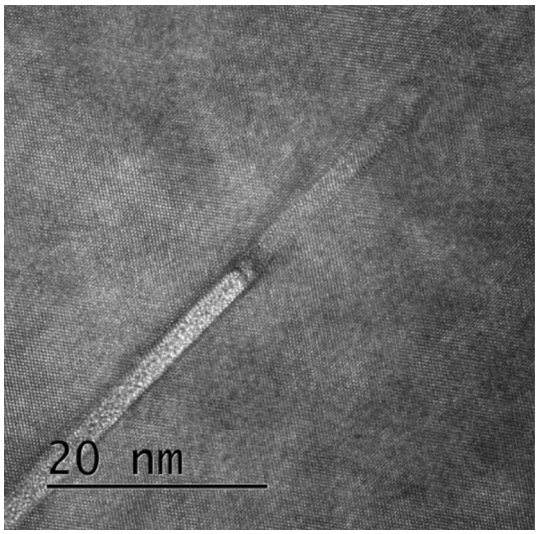

Fig. 10 TEM cross-section of the bond interface of a die from laminate I_Boron-1. A discontinuous SiO_2 layer of thickness around 2 nm is seen between the two silicon wafers. There are areas with continuous silicon material

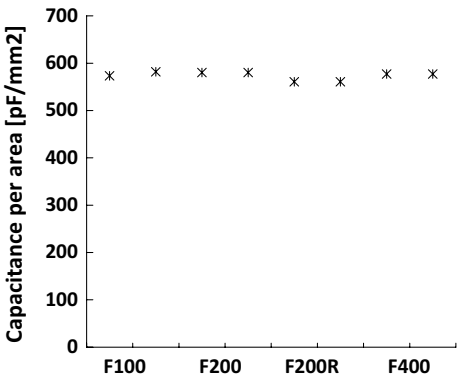

Fig. 11 Capacitance per bond area for two dies of each of the four designs from laminate I_Oxide-1

Figures 8, 9, 10 show TEM cross-sections of the bonded interface of laminates I_Oxide-1, I-3, and I_Boron-1. Laminate I_Oxide-1 appears to have a continuous layer of SiO_2 of thickness around 53 nm at the bond interface. Laminate I-3 appeared to have a continuous layer of SiO_2 with thickness 4 nm at the bonding interface. Laminate I_Boron-1 appeared to have a discontinuous SiO_2 layer at the bonding interface. Areas with an SiO_2 layer of thickness 2 nm and areas with continuous silicon material are visible in Fig. 10.

Figure 11 shows the capacitance per bond area for two dies for each of the four three frame designs of laminate I_Oxide-1. The average capacitance was 574 pF/mm^2, corresponding to an SiO_2 layer of thickness 60.2 nm. A typical I–V curve showing oxide breakdown on a die from laminate I_Oxide-1 is shown in Fig. 12. The oxide breakdown

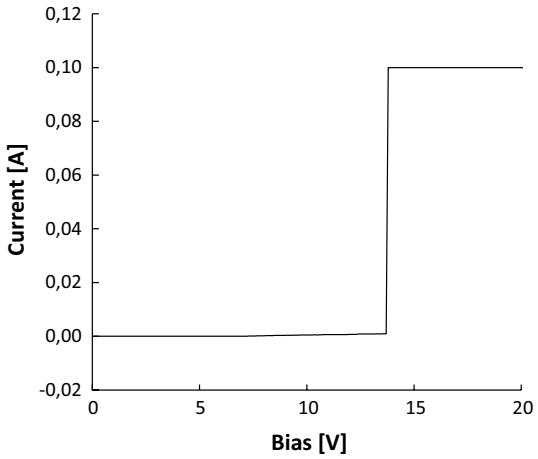

Fig. 12 Typical breakdown curve

voltages ranged from 13 to 42 V, indicating a dielectric strength of the oxide of 2.2–7.0 × 10^6 V/cm, assuming an oxide thickness of 60 nm.

5 Discussion

The hydrophilic pre-bonded laminates, kept together by hydrogen bonds, did withstand the wet RCA cleaning prior to bond annealing. This fact indicates that the investigated hydrophilic bond procedure resulted in relatively strong pre-bonds. Implanted wafers bonded equally well as non-implanted wafers, indicating that boron implantation did not significantly impede SDWB. This indication is further supported by the fact that bond strength measurements did not show any significant difference between implanted wafers, non-implanted wafers, and wafers with an intentional 60 nm thick SiO_2 at the bond interface (Schjølberg-Henriksen et al. 2014).

The low dicing yield of the F100 dies in Fig. 4 suggests that 100 µm is too narrow for obtaining a mechanically robust bonded frame. Frame widths of 200 and 400 µm had dicing yields of 89.1 % or higher. This high yield obtained on discontinuous frame structures supports the hypothesis of strong bonds, since the applied design does not allow for the propagation of a continuous bonding wavefront (Tong and Gösele 1998). The infrared pictures showed that the bonded area of 38 % of the wafer surface was enough to achieve bonds of high quality in all the intended bond area of all the seven bonded laminates, except one un-bonded quarter on laminate I-4. To avoid un-bonded quarters, a higher percentage of bond area of the wafer surface would probably have been beneficial (Taklo 2012).

The I–V measurements on wafer level showed that laminate I-4 had poor electrical contact between the aluminum and the un-implanted silicon. We think that a barrier was introduced between the Al and Si on one side of laminate I-4, but not on laminates I-1–I-3. The barrier could for instance be due to missing back-sputtering on one of the sides of laminate I-4 prior to the deposition of the Al contacts.

The results in Figs. 6, 7, and Table 3 demonstrate that hydrophilic pre-treated SDWB laminates annealed at 1,050 °C for 2 h result in electrically conductive bond interfaces with ohmic behavior. There was no correlation between the bonded area and the resistance, indicating that the resistance in the actual bond interface was negligible compared to the total resistance of the test structure. The average resistance across the dies was between 0.35 and 0.68 Ω. This value is 3–10 times higher than the calculated resistance in the bulk silicon of 0.02–0.1 Ω, and is probably due to contact resistance in the investigated system. The two implanted laminates had lower average resistance and lower standard deviation than the four un-implanted laminates (see Table 3). This result could indicate that the boron implantation improved the reliability of the electrical contacts across the bonded interface or at the aluminum contacts.

To our knowledge, the current study is the first report showing high conductivity and ohmic behavior of direct silicon bonds, investigating a set of more than 150 samples. The results obtained in the present study differ somewhat from the results of Bengtsson and Engström (1989), who reported non-linear I–V curves and resistances around 60 Ω for hydrophilic bonded laminates. However, the current results are in agreement with the electrical results obtained by Shimbo et al. (1986).

The TEM cross-section in Fig. 10 shows areas of continuous silicon lattice at the bonded interface of laminate I_Boron-1. This result is in agreement with the results that SiO_2 layers of thickness 15–20 Å break up during annealing above 950 °C (Wolstenholme et al. 1987) and 1,100 °C (Ahn et al. 1990) and that oxide "balls" or spheroids are formed during annealing above 1,100 °C (Wolstenholme et al. 1987; Ahn et al. 1990). This effect causes defined areas of continuous silicon lattice across the bonded interface, and is a likely explanation why the measured resistance was low and independent on the bonding area on laminates I_Boron-1 and I_Boron-2.

Figure 9 shows no discontinuity in the 4 nm thick SiO_2 at the bonded interface of laminate I-3. However, Fig. 7 and Table 3 show that the resistances of dies from laminate I-3 were similar to those from laminate I_Boron-1. The more likely explanation is that areas with continuous silicon lattice were indeed present on laminate I-3, but that none were visible in the relatively small sample area investigated by TEM. Another possibility is that the laminate I-3 did indeed have a continuous SiO_2 layer of thickness 4 nm at

the bonded interface which provided negligible electrical isolation. Bengtsson (1992) found that the bonded interface is a defect-rich region gettering metallic impurities, that commonly used dopants segregate at the interface, and that the bonding process may affect charges and electrically active interface states at the bonded interface. These three effects could result in an SiO_2 layer giving negligible electrical insulation at a thickness of 4 nm.

The nominal thickness of the SiO_2 layer of laminate I_Oxide-1 was 60 nm. The cross-sectional TEM image in Fig. 8 and the capacitance measurements in Fig. 11 suggest that the actual SiO_2 thickness was equal to the nominal thickness. This 60 nm thickness was sufficient to provide electrical isolation between the two bonded wafers. The dielectric strength of the bonded oxide of 2.2–7.0 $\times$ 10^6 V/cm is slightly lower than the tabulated value of 6.8–9.9 $\times$ 10^6 V/cm (Nicollian and Brews 1982). This could be an indication of imperfections in the oxide that is present at the bonded interface.

6 Conclusion

We have investigated the resistivity of hydrophilic high-temperature silicon direct wafer bonds. Hydrophilic pre-bonded laminates resulted in strong bonds and a dicing yield above 89 % for bond widths of 200 µm or wider. The average resistance of dies from boron implanted laminates was 0.35–0.44 Ω, and the average resistance of dies from un-implanted laminates was 0.51–0.68 Ω. All resistances were independent on bonding area, showing that the resistance of the bonded interface was negligible. Dies from hydrophilic bonded, boron implanted wafers had no Shottky diode formation, slightly lower resistance values and lower standard deviation, indicating that the implantation improved the reliability of the electrical contacts. In the case of boron implanted laminates, the low resistance is explained by a discontinuous SiO_2 and areas with continuous silicon lattice at the bonded interface. The results show that the oxide formed during silicon–silicon direct wafer bonding is broken up during bond annealing for 2 h at 1,050 °C, forming electrical connections of high quality between the two bonded wafers.

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Conflict of interest The authors declare that they have no conflict of interest.

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