3D Integration Technologies for Wireless Sensor Systems (e-CUBES)

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INTRODUCTION

The innovative approach presented here will realize so-called e-CUBES® (electronic cubes) [1], i.e. investigate and develop ultra small sensor cubes with dimensions of a few mm^3 which are wirelessly communicating among each other. The fabrication of e-CUBES with their need for high-level miniaturization (see Fig. 1) can only be realized by system integration technologies, which use the third dimension: 3D System Integration. In general not only one 3D integration technology is suitable for the fabrication of the large variety of 3D integrated systems. Moreover, a single product may need several different technologies for a cost-effective fabrication. Wireless sensor systems represent an excellent example for the need of a suitable mixture. Consisting of MEMS, ASICs, memories, antennas, and power supply modules they can only be fabricated in a cost-effective way by application of 3D technologies, which are particularly optimized for the integration of the different sub-modules. The main objective is to achieve extreme miniaturization of wireless sensor nodes. In consequence, all wiring should be realized through the stacked devices. Wire bonds are replaced by through-Si vias combined with electrical and mechanical interconnections between the devices. The removal of long wire bonds is especially beneficial for sensors based on a capacitive sensing principle (rather than i.e. a piezo-resistive sensing principle), since parasitic effects will be reduced.

BASIC e-CUBES CONSTRUCTION

The basic concept of an e-CUBES system is shown in Fig. 1. The enabling technologies described below are optimized for the 3D integration of the application layer, consisting of a processing unit and a sensor function.

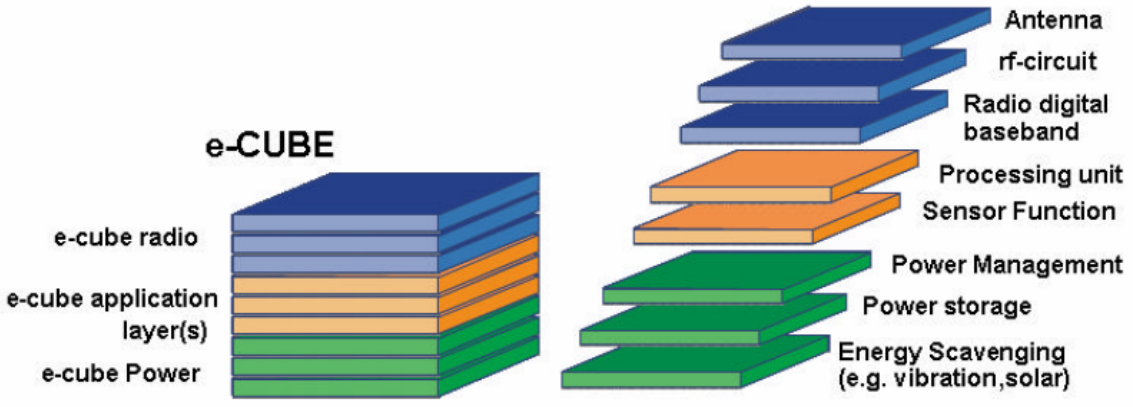

Figure 1: Basic structure of an e-CUBES system: 3D stacking of functional sub-systems.

Sensor Node Architecture

The sensor node which has been selected for the demonstration of a 3D integration concept represents a tire pressure monitoring system (TPMS). The key element of the complete system is a die-stack of a microcontroller, an RF transceiver and a pressure sensor as shown in Fig. 2. Additional components e.g. a bulk acoustic resonator (BAR) is flip chip (FC) assembled on top of the transceiver die. The cap of the sensor die and the transceiver die are processed with trough silicon vias (TSV´s) and matching routing and interconnection layers on relevant sides.

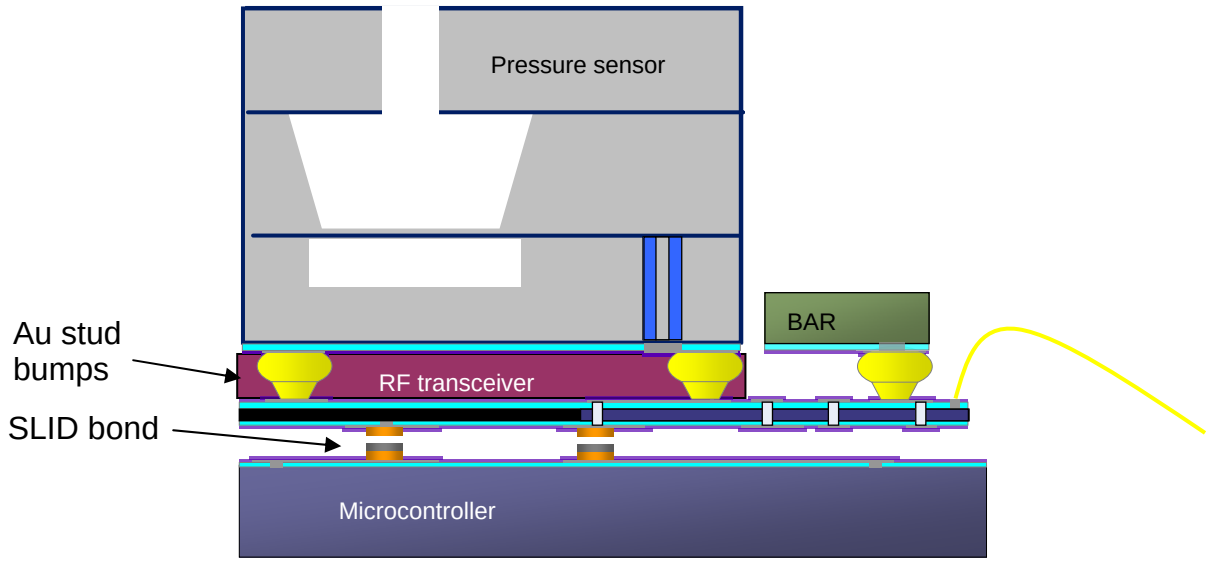

Figure 2: Schematic of a 3D integrated sensor/ASIC stack.

Each of the devices is a fully tested electronic device before stacking, which is possible because only chip-to-wafer bonding technologies are applied. Wafer-to-wafer bonding technologies are ruled out for this sensor node due to the different wafer and step sizes on which the involved dies are manufactured. The microcontroller wafer will be kept as a wafer during stacking whereas the RF transceiver, the pressure sensor and the BAR will be mounted as single chips.
There are a number of issues which influence the selection of interconnection and chip-to-wafer bonding method.

- Availability of the electronic component as e.g. wafer or single device (KGD)
- Device properties (e.g. fragile MEMSs or sensitive surfaces)
- Warp and co-planarity of the devices
- Temperature regime for 3D assembling of the components
- 3D stacking process sequence
- IO Interconnection density
- Pad metallization of devices (e.g. Al, Au)
- Required strength and hermeticity of final bonded system
- Required reliability of assembled stack
- Material limitations due to directives (e.g. lead free)

The final choice of interconnection technology must be based on the requirements of the specific application.

ICV-SLID technology for 3D IC integration

The RF transceiver and the microcontroller will be stacked first using an advanced interconnection technology e.g. back to face SLID interconnection with a thin CuSn metal layer. The formation and filling of the TSV as well the preparation of the IO pad metallization will be done on wafer level for the RF transceiver and the microcontroller respectively.
Fraunhofer IZM developed a pure "via first" 3-D integration process, the so-called ICV-SLID technology based on inter-chip vias (ICV) through the device substrates (through silicon vias) and metal bonding using solid-liquid-interdiffusion (SLID) soldering [2]. The SLID metal system provides the mechanical and the electrical connection, both in one single step. The ICV-SLID fabrication process is optimized for chip-to-wafer stacking with very high interconnect densities and therefore well suited for the cost-effective production of both high-performance applications and highly miniaturized multi-functional systems.
The through silicon vias are fully processed (etched, isolated and metallized) prior to a thinning sequence, with the advantage that the later stacking of the separated known good dice to the bottom device wafer is the final step of the 3D integration process flow. As a fully modular concept, it allows the formation of multiple device stacks. The corresponding schematic of the die-to-wafer stacking process is shown in Fig. 3. Thinned and stabilized devices (by use of handling substrates) with pre-processed through silicon vias are aligned, stacked and electrically and mechanically interconnected by intermetallic bonding.

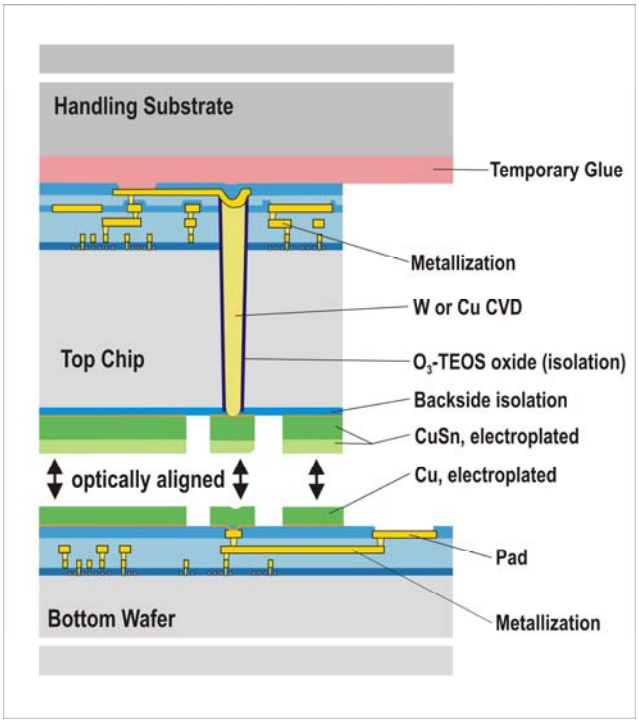

Figure 3: ICV-SLID technology – Stacking of the thinned and stabilized top chip (with pre-processed TSVs) to the bottom device wafer.

Both techniques, tungsten CVD and copper CVD, are well-suited for the metallization of high aspect ratio TSVs [3]. Depending on the lateral TSV size, it should be differentiated between a complete CVD-based TSV fill or the use of CVD as a seed layer with a subsequent electroplating process to complete the fill. A complete fill by CVD is generally applicable for small TSV diameters in the range of up to approximately 3 µm, especially at high aspect ratios. This limitation to comparably small TSV sizes is due to the metal properties and also due to the deposition process itself. The tungsten fill process is stress limited. The copper fill process is determined by the efficiency as precursor costs and relatively long processing times. In case of the Cu-CVD, new precursor developments could make the current Cu-CVD

process more efficient. Both processes are highly qualified for making seed layers. The high conformality of CVD allows for a film deposition with homogenous thickness on top and inside the TSV structures. Homogenous film thickness is a major condition for equal current density distribution in electroplating processes thus enabling void free filling results. For the application of 3D IC integration for e-CUBES, W-CVD was chosen because of its potential for cost-effective fabrication. The corresponding process sequence is described briefly: After completion of the TSV insulation, a full in situ process sequence under vacuum is performed, consisting of an Ar pre-sputtering step in the W etch back chamber (RIE), multiple deposition/etch steps to achieve a 20 to 30 nm thick, plasma-densified titanium nitride seed layer in the TiN-MOCVD chamber, followed by approximately 1100 nm W-CVD, cool down under vacuum and partial etching of tungsten in the W etch back chamber.

Au stud bumps and vias for 3D MEMS integration

The pressure sensor and the BAR will be stacked onto the RF transceiver die using FC with Au stud bumps. SINTEF tested the use of FC with Au stud bumps for dummy sensor dies and dummy ASIC wafers as shown in Fig. 4 [5]. FC interconnection with Au stud bumps is advantageous when there is a low number of interconnects between devices or when any of the devices can not see any further wet processing due to i.e. inlets. Both boundary conditions are given for the pressure sensor wafer stack in the TPMS demonstrator. FC assembly of the BAR and the sensor device onto the RF transceiver is compatible to the stacked arrangement of the RF transceiver with TSV and the microcontroller wafer underneath both with regard to mechanical integrity (can one say that?) and temperature budget.
Au stud bump bonding using an underfiller to ensure mechanical strength has been selected for the pressure sensor die which is rather thick compared to its lateral dimensions (1:2). The thinner and smaller BAR device which is less bulky (1:6) is only available as single devices. Parts of its surface can not be covered with any material as that will hinder proper functionality. Au stud bump bonding has been considered a viable solution also for this device, but no underfilling is allowed.

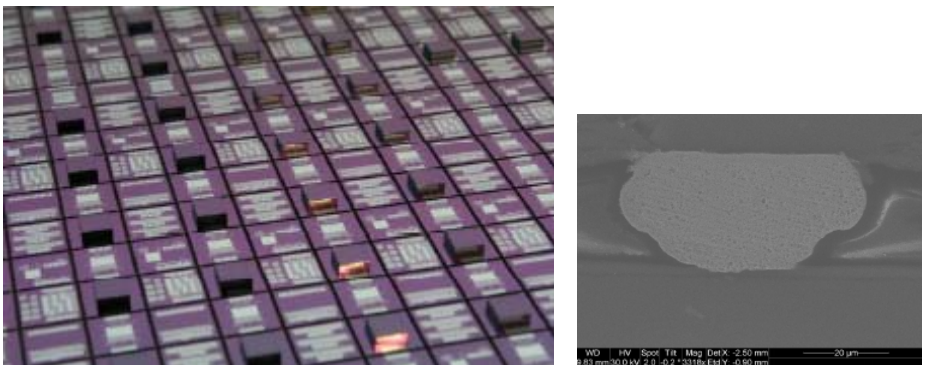

Figure 4: Dummy sensor devices bonded to a dummy ASIC wafer with Au stud bumps shown to the left. Cross section of a single bump inside an underfiller shown in the SEM image to the right.

Silicon vias with glass insulation ensure that electrical signals to and from the active elements of the pressure sensor in the TPMS demonstrator are transferred through the cap of the die. An aluminium routing layer on top of the cap is the only required metallization needed for Au stud bumping. The routing of the BAR device is gold based (I will not say only gold since Infineon may not like that) which is ideal for Au stud bump bonding. An alternative solution for vias through thick MEMS wafers is use of hollow vias with thermal oxide as insulation and highly doped poly silicon as a conductive layer [4]. Routing to such vias can be realized in aluminum and be prepared for Au stud bumping by combining dry film resist and dry etch of conductive layers [5].

EXPERIM ENTAL RESULTS

Initial tests of Au stud bump bonding and vias for MEMS

Only few vias and interconnecting Au bumps are required for the pressure sensor, but additional dummy bumps are included to achieve a homogenous pressure distribution during stud bump bonding (SBB). A large amount of bumps (>50) is not recommended because the total tool pressure available during SBB is limited. The strength of the bond for bulky devices will be assured by using the underfill Epotek 353 ND which can withstand post processing temperatures in the range of ~260^{o}C.

Initial tests for Au SBB of the pressure sensor in the TPMS demonstrator are performed by SINTEF and Fraunhofer IZM using dummy sensor wafers and dummy substrates. The Au stud bumping is performed by Kulicka and Soffa [6]. The dummy sensor wafer is either an anodically bonded glass-silicon-glass stack without any vias or a single wafer with hollow vias. An SEM image of hollow vias with sputtered aluminum is shown in Fig. 5.

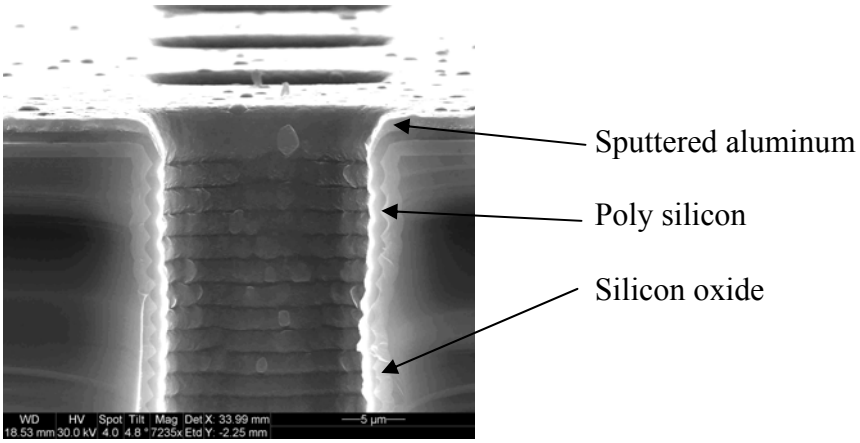

Figure 5: SEM image of the top of hollow vias that can be used as vias through thick MEMS wafers. The insulating oxide layer, the conductive poly silicon and the sputtered aluminum are indicated.

For both kinds of dummy sensor wafers there is aluminum routing prepared for Au stud bumping and various electrical test measurements (Kelvin structures and Daisy chains). The design of the routing is shown in Fig. 6 for the two types of dummy sensors. There are 32 pads for Au stud bumps in each design. For the wafer with hollow vias an aluminum routing layer is designed for the back side of the wafer as well, but the layer has been omitted in the figure for simplicity.

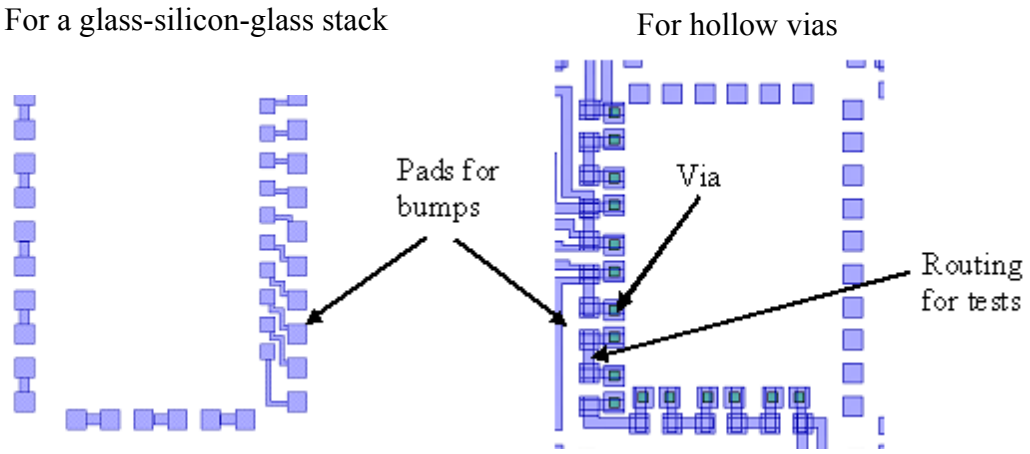

Figure 6: Design of aluminium routing for a glass-silicon-glass stack without vias (left) and for a single wafer with hollow vias (right). A number of 32 pads are present in both designs for Au stud bumping.

Bumped dummy sensor wafers are diced and will be assembled by Datacon [7]. A bumped glass-silicon-glass stack is shown in Fig. 7. The quality of the Au stud bumps is inspected before bonding. The average (± standard deviation) lateral dimension of the bumps was 51.60 ± 0.86 µm for 30 measured bumps on a glass-silicon-glass stack. Their average height was 30.20 ± 1.00 µm and their average shear strength was 23.32 ± 1.71 gf.

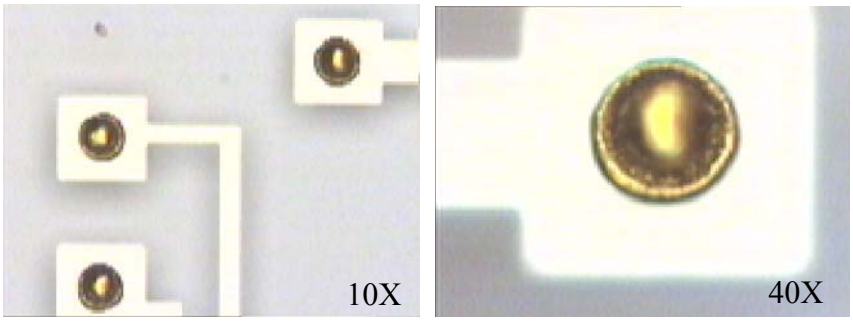

Figure 7: Au stud bumps on aluminum routing for a dummy sensor glass-silicon-glass stack.

Bumped dummy sensor dies will be bonded to special test substrate wafers imitating the RF transceiver die. The substrate wafers will have a thermal oxide layer for insulation and a metal layer for routing. Test substrates have been manufactured by SINTEF having pure Al and by Fraunhofer IZM having AlSi. The purpose of the design for the test substrates is testing of electrical resistance of the Au bump interconnections, the hollow vias, and the combination of the two. Additionally, test chips will be used for mechanical testing of bond strength. An overlay of the design for the routing on the test substrate and a glass-silicon-glass dummy sensor chip is shown as an example in Fig. 8

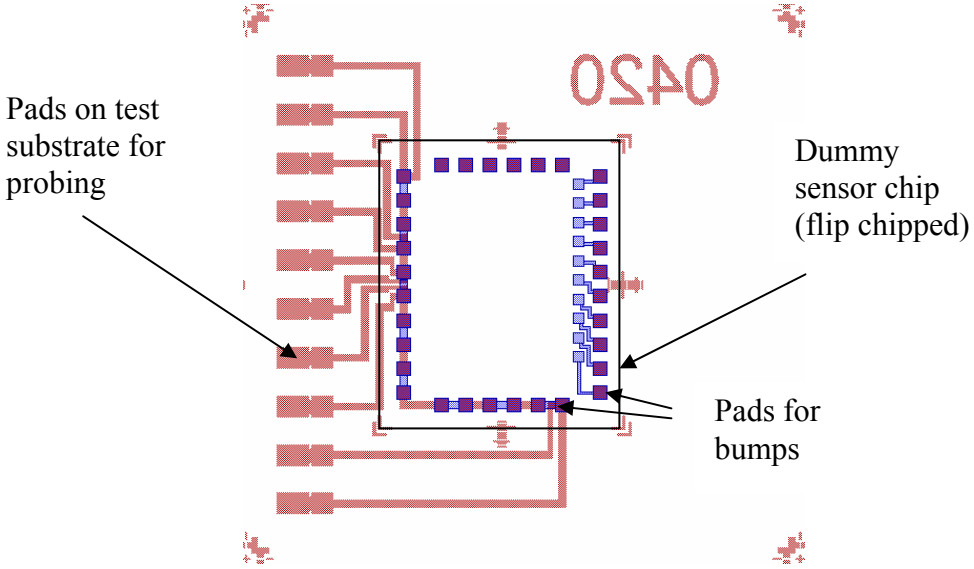

Figure 8: Design of routing on the test substrate and on the dummy glass-silicon-glass sensor chip.

Real pressure sensors with silicon vias in a glass matrix are being manufactured by Infineon Technologies SensoNor for the TPMS demonstrator [8]. SINTEF will pattern the aluminum routing on those wafer stacks with the same mask as the one presented for the glass-silicon-glass stacks.

IC device-stack formation by ICV-SLID technology

The IC device-stack was fabricated by bonding of top device chips to a bottom device wafer by approx. 10 µm thin soldering pads which provide both electrical and mechanical interconnection by a Cu/Sn SLID metal system [9]. The through-Si vias were fully processed - etched and metallized as well - prior to the thinning sequence, with the advantage that the later stacking of the separated known good dice to the bottom device wafer was the final step of the 3D integration process flow. The corresponding fully processed 3D integrated test structure fabricated with ICV-SLID technology is shown in Fig. 9. The 2 x 10 µm^2 and > 20 µm deep through silicon vias were isolated with a highly conformal O_3/TEOS oxide and void-less filled with tungsten CVD. The thinned top chips were connected to the bottom device wafer by the SLID metal system (Cu, Cu_3Sn, Cu). The Cu/Sn metallization for the SLID interconnect was realized using through-mask electroplating. The copper and tin thicknesses were selected according to the temperature profile during bonding in with respect to the topography of the devices. During bonding at approx. 300°C the deposited Sn was completely transferred into Cu_3Sn intermetallic alloy. This so-called ε-phase is thermodynamically stable with a melting point above 600 °C. Using appropriate film thicknesses, tin was consumed and the solidification was completed within a few minutes, leaving unconsumed copper on both sides (see Fig. 9). The W-filled TSVs are interconnected by Al wiring to the metallization of the top device and by the above described soldering metal system to the metallization of the bottom device. Vertical interconnect resistances of approx. 0.3 Ohm were measured with TSV test structures. The optimized chip-to-wafer 3D-IC stacking technology is well suited for cost-effective fabrication of the processing unit of e-CUBES.

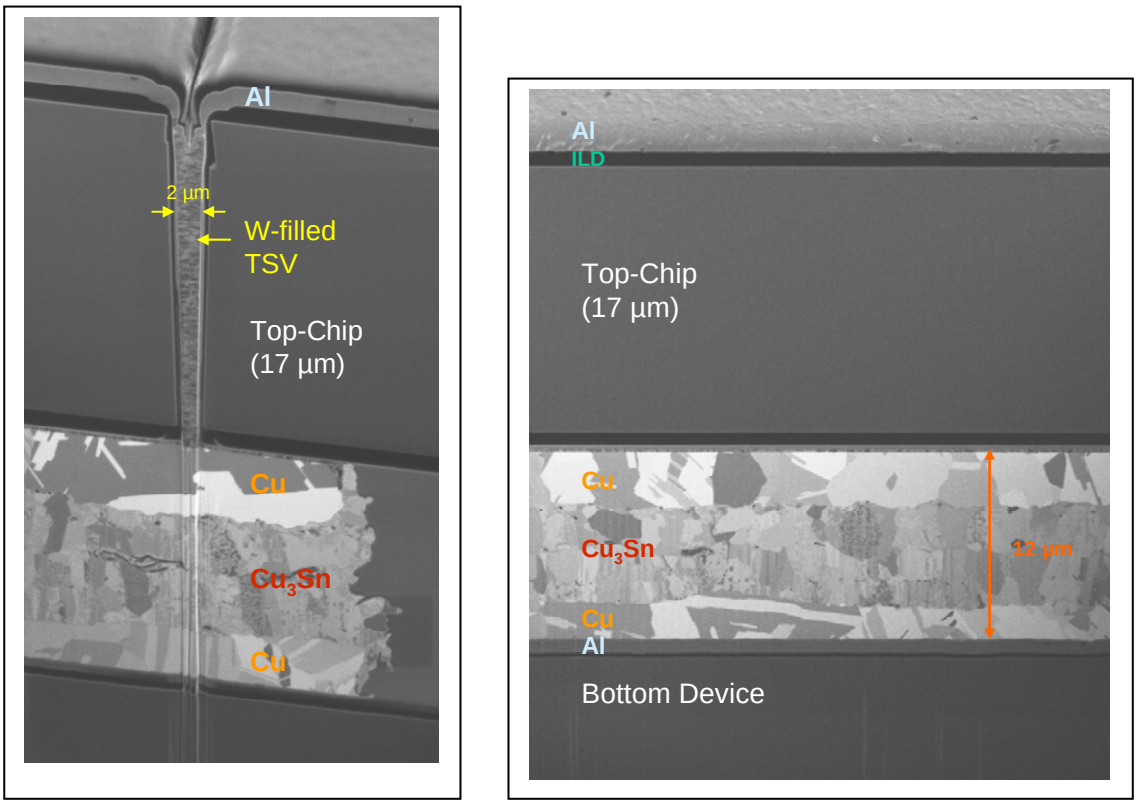

Fig. 9: FIB of a device-stack, 3D-integrated by ICV-SLID technology
Left: region with CVD-tungsten filled TSV; Right: Cu/Sn SLID bond in detail

CONCLUSION

The realization of ultra-minaturized wireless sensor nodes like “e-CUBES” represents an entirely new challenge and requires a synergy of individual technologies at an exceptionally early stage. In order to realize future small sized wireless autonomous sensors, new integration technologies are required that also use the third dimension for system integration. 3D integration technologies based on wafer level approaches have the potential to meet the requirements of extreme miniaturization. The stacking concept allows combination of different devices (e.g. MEMS-sensor, DSP, RF transceiver, power supply).
ICV-SLID technology and other interconnection and via techniques (e.g. Au stud bumps and solder microbumps, silicon vias and hollow vias) are well suited for device stacking. Selection of interconnection technology depends on the availability of electronic devices (e.g. wafer or single die) and several other application specific requirements, as e.g. vertical interconnect densities. The ICV-SLID technology is optimized for the fabrication of 3D ICs (i.e. processing unit of e-CUBES). Fabrication of wireless sensor nodes needs as well technologies optimized for 3D integration of subsystems of sensors, radios and energy supply devices. The fabrication of distributed wireless sensor systems is a typical example for the need of mixed approaches, taking advantage of a combination of different specific 3D integration technologies.
The newly generated system solutions will be innovation drivers and provide special attraction for new applications such as ambient intelligence and environment sensing.

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