ETCHING BURIED OXIDE AT THE BOTTOM OF HIGH ASPECT RATIO STRUCTURES

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INTRODUCTION

Dry anisotropic etching using high density plasmas is a key technology that is widely used in micro-fabrication and high aspect ratio structures in silicon play an important role in many MEMS and semiconductor applications. SOI substrates are often employed in order to ensure a uniform etch depth for all structures, by using the buried oxide (BOX) as an etch stop layer. In this present work, we look at the challenges involved in anisotropic etching of the BOX layer at the bottom of high aspect ratio structures and we report on a newly developed etch process for this purpose.

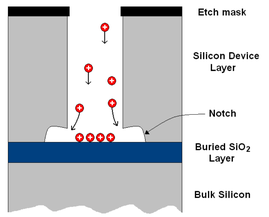

Figure 1: Notching resulting from the charge buildup on the BOX layer.

Charge accumulation on the exposed BOX layer inside high aspect ratio structures distorts ion trajectories and causes deflection of ions towards the sidewalls of the etched structures. This leads to undesirable lateral etching of structures in the silicon device layer which is known as notching (figure 1). This could cause problems in the subsequent fabrication steps or hamper the performance of the devices. An additional challenge when etching the BOX layer is the fact that the etching of SiO_2 layers in general requires a relatively high amount of energetic ion bombardment. As the amount of energetic ion bombardment at the bottom of high aspect ratio structures is considerably reduced, it results in a very low etch rate for the BOX layer.

EXPERIMENTAL SETUP

All experiments were performed on an Alcatel AMS200 SE I-Productivity etch tool. It is a down-stream etch tool equipped with a high density ICP source. Electrostatic substrate clamping is used and the substrate can be biased either by applying RF power (13.56 MHz) or pulsed/non-pulsed LF power (100 KHz to 460 KHz). The typical process gases used are SF_6, C_4F_8 and O_2. On this tool it is possible to run a switched etch process such as the BOSCH DRIE process as well as continuous etch processes such as dielectric etch or isotropic silicon etch, making it a very versatile tool for micro-fabrication.

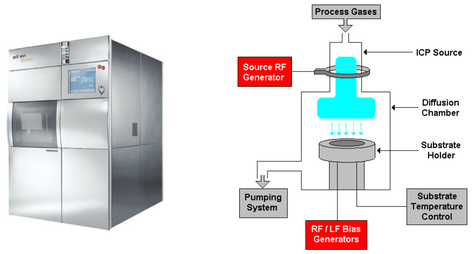

Figure 2: Alcatel AMS200 SE I-Productivity etch tool and a functional illustration of the same.

The substrates used in these experiments were all 100 mm diameter SOI wafers with a nominal thickness of 340 µm. Two types of wafers were used with different silicon device layer and BOX layer thicknesses. On all the wafers test structures in the form of trenches with a width of approximately 7 µm and a length of 70 µm were etched down to the BOX layer using the BOSCH process. The trenches had an aspect ratio of approximately 5:1. The goal of the experiments was to develop an etch process to anisotropically etch through the BOX layer at the bottom of the trenches with as little notching as possible.

RESULTS

Etch Results I

The SOI wafers had a 0.5 µm thick BOX layer and a 43 µm thick device layer. Figure 3a shows the results obtained with a standard dielectric etch process (Recipe RF1) which uses RF bias. Figure 3b shows the results obtained with a new process (Recipe RF2) which uses double the RF bias power, half the pressure and half the C_4F_8 gas flow compared to recipe RF1.

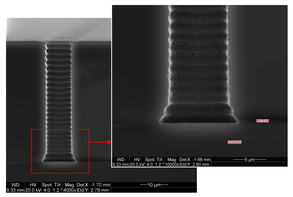

Figure 3a: Etch results obtained using recipe RF1 on SOI wafers with a 0.5 µm thick BOX layer.

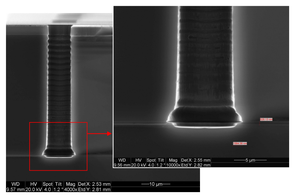

Figure 3b: Etch results obtained using recipe RF2 on SOI wafers with a 0.5 µm thick BOX layer.

With recipe RF1, no buried oxide was etched at all whereas with recipe RF2, the significantly higher ion energy made it possible to etch through the 0.5 µm thick BOX layer. However in both cases there was a considerable amount of notching that resulted from the BOX layer etch..

Etch Results II

The SOI wafers had a 2 µm thick BOX layer and a 40 µm thick device layer. Figure 4a shows the results obtained with a recipe RF2 that was successfully used to etch through a 0.5 µm thick BOX layer. Figure 4b shows the results obtained with a newly developed process (Recipe LF1) which uses pulsed LF bias.

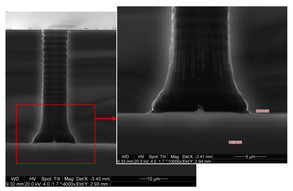

Figure 4a: Etch results obtained using recipe RF2 on SOI wafers with a 2 µm thick BOX layer.

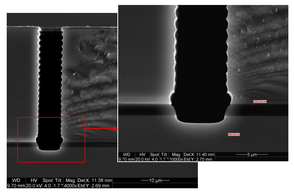

Figure 4b: Etch results obtained using recipe LF1 on SOI wafers with a 2 µm thick BOX layer.

In spite of the high ion energy, with recipe RF2 almost no buried oxide was etched and there was a very large amount of notching. However recipe LF1 which uses pulsed LF bias made it possible to etch through even the 2 µm thick BOX layer with very minimal notching resulting from the BOX layer etch.

Parameter	Recipe RF1	Recipe RF2	Recipe LF1
Avg. etch rate of top surface SiO_2 (nm/min)	456	609	202
Avg. etch rate of 0.5 µm BOX layer (nm/min)	~0	~167	~120
Avg. etch rate of 2.0 µm BOX layer (nm/min)	~0	~0	~105
Avg. photoresist etch rate (nm/min)	310	526	115
Avg. aluminium etch rate (nm/min)	12.3	38.9	7.8

Table 1: Summary of etch-rates for all the etch processes

APPLICATION

MEMS accelerometers were fabricated along with through-silicon vias (TSVs) on SOI substrates. The use of TSVs significantly simplifies the mounting of the components and it also results in the smallest geometry. Using a via-first approach, TSVs were first created on the SOI wafers followed by fabrication of the MEMS devices.

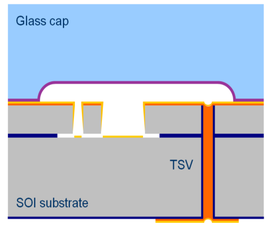

Figure 5: A schematic cross-section of a MEMS accelerometer with TSVs through the SOI wafer.

Plasma etching was extensively used in the fabrication process. For creating the TSVs, the BOSCH process was used to etch through the silicon device layer and the bulk silicon. The 2 µm BOX layer was etched using the newly developed 'pulsed LF bias' etch process. This enabled us to minimize the notching at the bottom of the device layer which would have led to void formation in the TSVs.

CONCLUSION

Anisotropic etching of buried SiO_2 layers at the bottom of high aspect ratio structures is challenging. We have shown that for this purpose a dielectric etch process using RF bias has significant limitations: very low etch rate, notching issue, and low selectivity to the etch mask. The root cause of the problem is the charging of the BOX layer which causes ion trajectories to diverge towards the sidewalls of the high aspect ratio structures.

Although pulsed LF biasing has been used to limit notching in deep silicon etching, to our knowledge its use in etching of the BOX layer has not been reported in literature until now. We have successfully developed a new dielectric etch process using pulsed LF bias. The 'ON' time of the pulses provide enough ion energy to etch the BOX layer while the built-up charge gets enough time to discharge during the 'OFF' time of the pulses. Using this new process it is possible to etch through even relatively thick buried oxide layers with very little notching.

ACKNOWLEDEGMENT

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FOR FURTHER INFORMATION

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