High aspect ratio deep RIE for novel 3D radiation sensors in high energy physics applications

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***Abstract*–3D detectors with electrodes penetrating through the entire silicon substrate have many advantages over conventional planar silicon technology, for example, high radiation tolerance. High aspect ratio through-wafer holes are essential in such fabrication, and deep reactive ion etching (DRIE) is used. A series of DRIE processes were tested and optimised to achieve the required aspect ratio, and in 5-µm wide trenches, aspect ratios of 58:1 were achieved.**

I. Introduction

FUTURE high energy physics experiments requires radiation hard detectors with fast time response and sensitive borders to cope with the increasingly stringent research requirements. 3D detectors, as shown in Fig.1 have electrodes penetrating through the entire silicon substrate have drawn high interests amongst the high energy physics community in recent years, due to their unique advantages such as fast time response, edgeless capability and radiation hardness as described in previous literatures [1-13]. In addition, the through-wafer electrode technology can provide the possibility to connect 3D detectors on a wafer level via 3D interconnects. The two different electrode types, n and p are also accessible from the front and the backside of wafer in 3D detectors, allowing easy processing for double-sided readout if desired. Together with the short electrode spacing, double-sided read-out can tremendously improve the spatial resolution in pixel detector systems [14, 15].

These advantages are strongly dependent on a successful deep reactive ion etching (DRIE) process. In the final 3D sensors, the through-wafer electrodes are filled with highly doped polysilicon that has a low mobility for both electrons and holes, making the electrodes less sensitive (about 40-50% compared to the main active area) to incident radiation and their diameters must therefore be as small as possible in order to maximize the sensitivity. Meanwhile, the wafer thickness must be reasonably thick, preferably no less than 230 µm in order to have a good signal-to-noise ratio since the signal induced by ionising particles are proportional to the thickness of the substrate that the ionising particle traverses. Having an efficient deep reactive ion etching (DRIE) process that results in high aspect ratio is thus crucial in the fabrication of 3D detectors. SINTEF MiNaLab owns a class 1000 clean room with several state-of-the-art DRIE etchers and has the ideal in-house facilities to develop and to fabricate 3D detector in production volumes. The first production attempt was tested and trial at SINTEF MiNaLab in 2007, through-wafer holes with aspect ratios of up to 15:1 and trenches of 36:1 were demonstrated [16]. These were etched by an Alcatel AMS-200 I-Speeder etcher [17] using a modified Bosch process [18].

During the second on-going fabrication run of 3D detectors at SINTEF began in January 2009, a DRIE process was developed to fabricate detectors with 14 µm holes and 5 µm trenches through a 285 µm thick substrate in order to improve the chip sensitive area and electrical performance even further. Several test runs using a newly installed Alcatel AMS-200 I-Productivity etcher were completed and the results were promising with an average etch rate of 6.1 µm. Aspect ratios of 20:1 in 14 µm round holes and 58:1 in 5 µm trenches were achieved. In addition, high selectivity was achieved by using aluminium masks and notching at oxide interface was reduced by using low frequency (LF) bias.

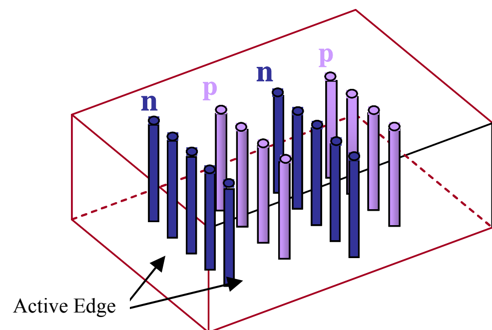

Fig. 1. *3D detectors with both p and n electrodes penetrating through the entire silicon substrat, the 'active edge' electrode is also a through-wafer trench that surrounds the entire detector to allow edgeless capability.*

II. Experiment

A. High Aspect Ratio Etching

A new Alcatel AMS-200 I-Productivity etcher has recently been installed at SINTEF MiNaLab, an etcher that is more suitable for high aspect ratio etching. The improved etch rate and selectivity is ideal to achieve high aspect ratio DRIE structures with little sidewall damages in a shorter process time. A process was developed to etch narrow trenches and 14 µm round holes through 285 µm thick wafers. This would be used in the second 3D detector run at SINTEF. No previous 3D detectors were thicker than 255 µm, this would

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allow the study of signal-to-noise ratio and capacitance in 3D detectors with respect to the substrate thickness.

A batch of 24 test wafers was etched using different process parameters to identify an optimised process required in 3D fabrication. A 2 µm thermal oxide was grown on all 24 test wafers prior to any deep reactive ion etching. This oxide was also used as the etching mask on 12 wafers, while the remaining 12 wafers had an additional aluminium layer (1.5 µm thick) as their etching masks, sputtered on top of the 2 µm thick thermally grown oxide. Both masks were patterned by standard lithography.

Following the DRIE process, the wafer must be cleaved or diced for inspection of the process results. Dicing, however, can create cracks along the diced edge and distort the actual profile of the holes. On the contrary, cleaving is preferred and results in smooth edges, but is rather difficult in the presence of through-wafer holes. For the purpose of inspection, the thickness of the test wafers were thicker than 285 µm, same as the thickness in the process wafers in the second 3D run, and 500 µm thick test wafers were used in this test to allow easy cleaving and inspection.

B. Suppression of Notching at dielectric interfaces

In 3D detector processing, the sensor wafer is oxidised and bonded to a support wafer, as shown in Fig.2. Through-wafer trenches are first etched and filled to form the 'active edge' electrode that surrounds the entire sensor to allow edgeless capability. During the DRIE process, a bonded wafer is required to keep all sensors in place and processable. Without the support wafer, the sensors would consequently be detached from the process wafer, not possible for further processing

When the sensor wafer is etched through, charging occurs in the oxide layer between the two wafers. This charged oxide can then re-direct the etching plasma which attacks the sidewalls, causing severe notching at the bottom of the etched structures [19]. This effect was previously observed in the first SINTEF 3D detector run, as shown in Fig. 3 [16]. In this first run, the etching time was carefully tuned to minimise the amount of notching, but some degree of notching was inevitable as the holes must be slightly over etched in order to compensate for any variations in both the wafer thickness and the etch rate across the wafer.

Pulsing the bias power on the substrate allow the dielectric to discharge when the bias is off, and when low frequency (LF) pulsing is used, the dielectric can then have a longer time to discharge reducing the re-directed ions, thus reducing the notching. Low frequency pulsing was not available in the tool used in the first run, but is available in the new Alcatel AMS-200 I-Productivity etcher. Several bonded wafers were tested to investigate the notching effect and its reduction by low frequency pulsing.

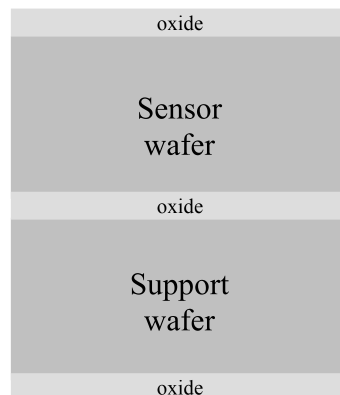

Fig. 2. *Through-wafer trenches surround the sensor and a support wafer is required to keep the sensors in place after DRIE in order to keep the sensors in place and the wafers processable. The support wafer can be removed once all fabrication steps are completed.*

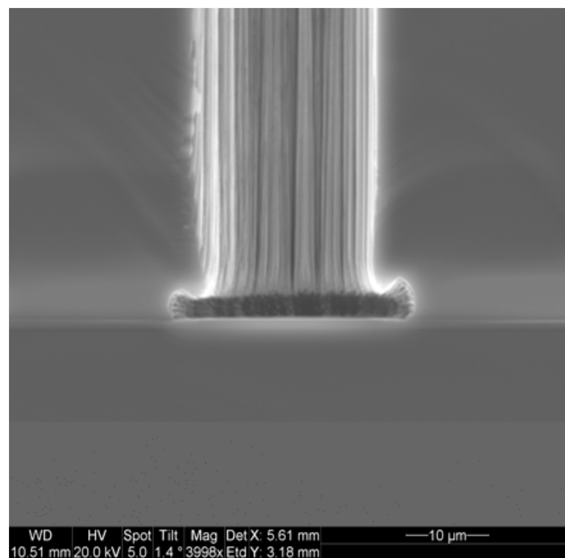

Fig. 3. A SEM-micrograph shows how over-etching can cause notching at the bottom of the holes due to charging in the oxide, which deflects the ions which then attack the side walls.

III. RESULTS

A. High Aspect Ratio Etching

A short etching time of 20 minutes was first used to test the Alcatel I-Productivity etcher and to evaluate the results obtained from the two different masks, oxide and alumnium. Fig. 4a and Fig. 4b show the SEM images of the DRIE holes, resulting from an identical DRIE process when using the two different masks. Fig. 4a corresponds to a process that used an oxide mask, while Fig. 4b was resulted from using an aluminum mask. The results were identical and the average etch rate was 10 µm per minute. Both profiles have a diameter of 15 µm and are 155 µm deep. The size of the holes was increased from 14 to 15 µm after the DRIE process.

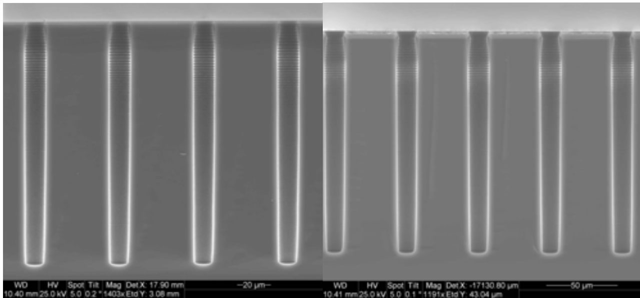

Fig. 4a. (left) *SEM image of DRIE 14 µm round holes with an aspect ratio of 10:1 resulted from using a 2 µm thick oxide mask.* Fig. 4b. (right) *SEM image of DRIE holes with an aspect ratio of 10:1 resulted from using a 1.5 µm thick aluminium mask.*

In order to have an aspect ratio of 20:1, a longer etching time was required. In this test, the oxide mask was shown to have a lower selectivity than the aluminium mask. After 45 minutes of DRIE, the oxide was etched through and the silicon substrate was severely damaged. The selectivity of oxide masks was therefore not high enough to etch 14 µm round holes through a 285 µm thick silicon substrate. The damages on the surface can be seen clearly in the SEM image shown in Fig. 6.

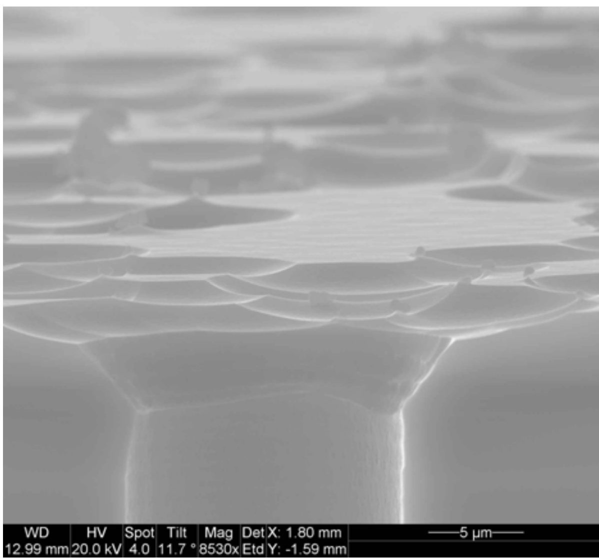

Fig. 6. *SEM image of DRIE holes resulted from a process in attempt to achieve 14µm round holes with an aspect ratio of 20:1 using an oxide mask. Limited by the selectivity of oxide mask, the mask was etched away and the substrate underneath was damaged by the plasma.*

Due to the edge bead removal in photolithography, the aluminium mask did not cover the wafer all the way to the wafer edge. Slight damages were observed on the edge of the wafers where the aluminium was etched away during the standard lithography and the edge was only protected by the 2 µm thick thermal oxide. The integrity of the wafer was, however, preserved and remained processable after the DRIE process. Fig. 7 shows the results from an aluminium mask after an etching time of 45 minutes. The holes were 305 µm deep with a diameter of 15 µm, giving an aspect ratio of more than 20:1.

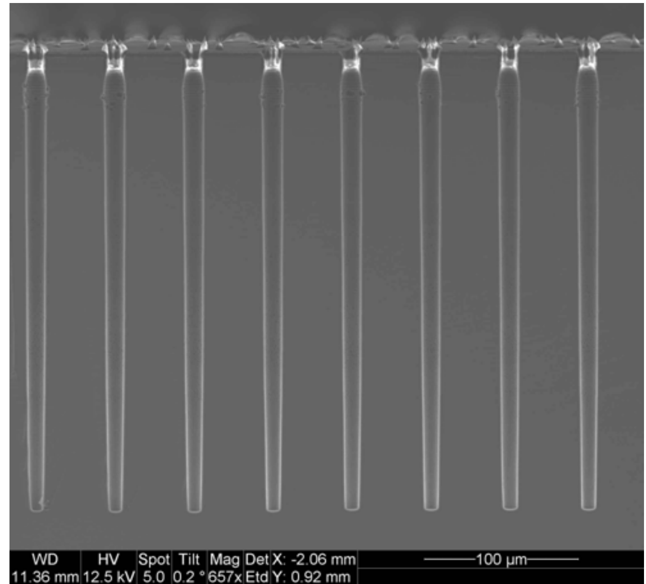

Fig. 7. *SEM image of DRIE holes with an aspect ratio of 20:1 using a 1.5 µm thick aluminium mask. The substrate surface was protected by the aluminium mask, which has a higher selectivity when compared to the oxide mask as shown in Fig. 6.*

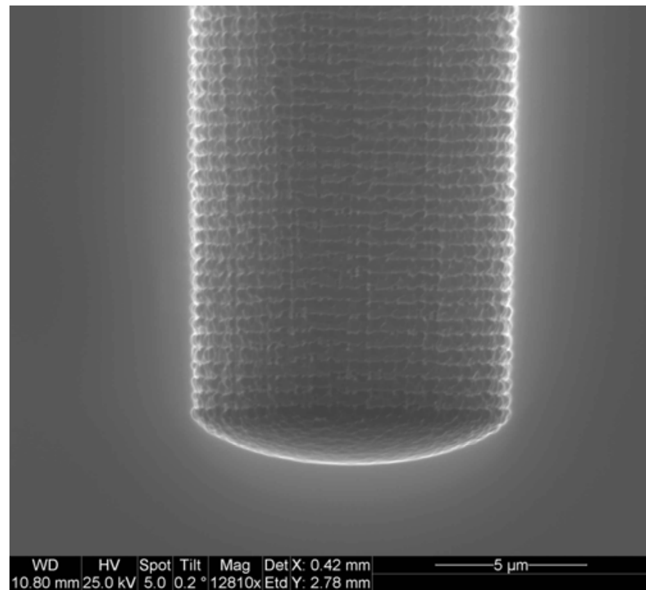

Fig. 8. The bottom of the holes as shown in Fig.7 is clearly narrower than the top and the etch rate is clearly slower towards the end of the process. Another process was used to improve the uniformity in the etch rate throughout the process.

The profiles of these holes show the etch rate in the lateral direction is not uniform throughout the process. As shown in Fig.8, the bottoms of the holes are only 8 µm wide and are narrow compared to the 15 µm round holes at the top. For our applications, the profile of the holes should be as cylindrical as possible and narrow bottoms should be avoided. A second process was then used to produce wider bottoms by gradually

increasing the LF bias in a 3-step procedure during the DRIE process. The lateral etch rate as suggested by Fig. 8 decreases as the process progresses. The etching power in each step was therefore increased progressively, to improve the uniformity of the etch rate throughout the process.

Fig. 9 and 10a shows the resulting holes to be more cylindrical and the diameter at the bottom was measured to be 11.8 µm. The sidewalls were also very well protected by the polymer and no wall damage was observed (Fig. 10b).

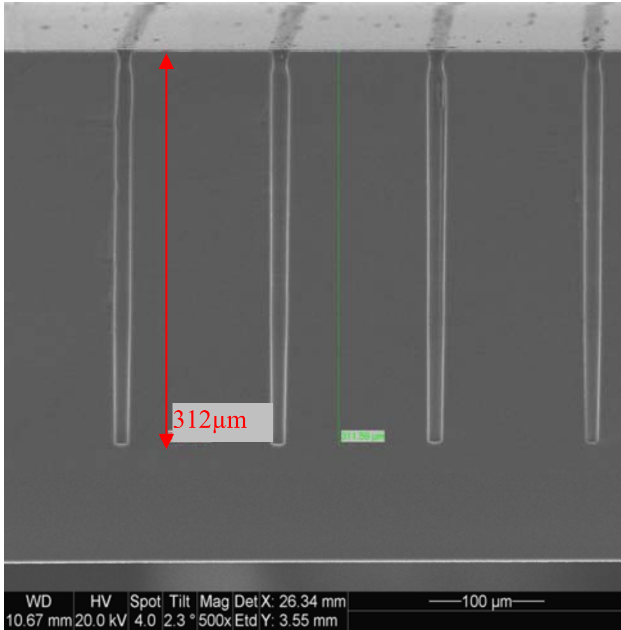

Fig. 9. Uniformity of etch rate was improved by increasing the etching power towards the end of the process. The aspect ratio of the DRIE holes is 20:1.

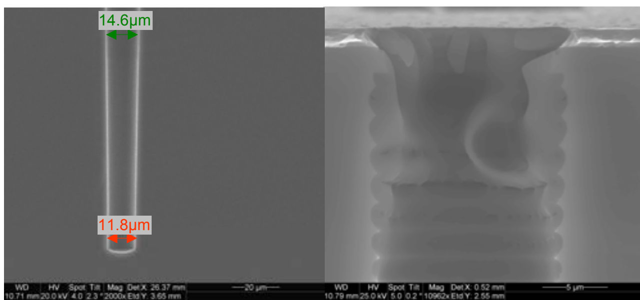

Fig. 10a (Left) The bottom of the hole was measured to be 11.8 µm wide, making the holes more cylindrical than using the process shown in Fig.9. Fig. 10b (Right) A close up SEM image shows the scalloping effect resulting from the DRIE process with zero wall damages.

In the processing of 3D detector, the trenches are filled with highly doped polysilicon after DRIE and form an 'active edge' electrode surrounding the entire detector. They are also etched simultaneously with the holes to minimise the number of process steps required for polysilicon deposition and doping of the electrodes. The etch rate of the trenches should therefore be similar to that in the holes to avoid excessive over etching. This can be controlled by choosing trenches with suitable dimension since the total area exposed to the etching plasma affect the overall etch rate.

In order to determine the suitable width for the trenches, trenches of different widths (1, 2, 5, 7, 10 and 20 µm) were etched. Using the same process used to etch round holes shown in Fig. 10, the set of trenches were etched and different etch depths were resulted for different trench width as shown in Fig. 11. The resulted 5-µm trenches were 290 µm deep, having an aspect ratio of 58:1.

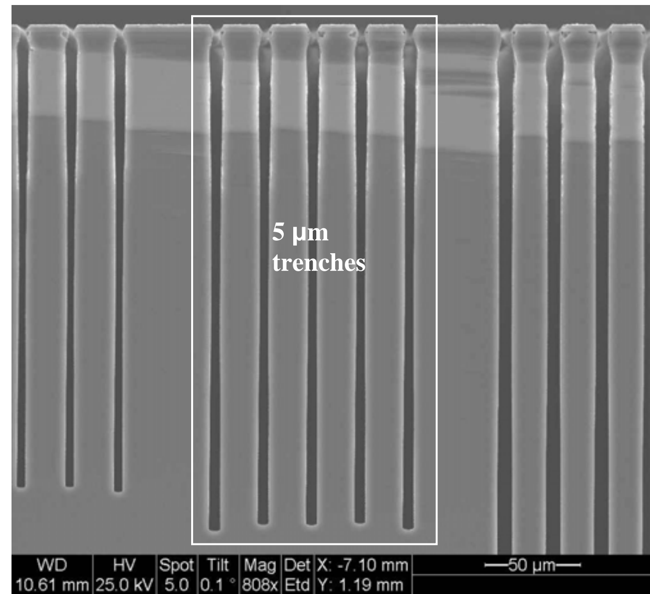

Fig. 11. SEM image of DRIE trenches, which are necessary for fabricating p+active edge electrode. The 5 µm wide trenches are 290 µm deep, giving an aspect ratio of 58:1.

B. *Suppression of Notching at the oxide interface*

The low frequency pulsing available in the new DRIE tool allows longer time periods for the oxide to discharge. This reduces possible attacks on the side walls by the re-directed ions due to the charges built up in the oxide interface. A bonded wafer was etched using the same DRIE process shown in Fig.10 to observe any notching effect at the interface. The sensor (top) wafer was 285 µm thick, 20µm thinner than the DRIE process aimed to etch. The over etch of the process was employed to compensate for any variations in the etch rate and wafer thickness across the wafer. The etching result shown in Fig. 12, displays some slight damages on the side walls caused by the over etch. Besides these small damages, no notching is observed at the bottom of the holes and its suppression using low frequency switching was shown to be effective.

IV. Conclusion

DRIE holes with 15 µm diameter and aspect ratio as high as 20:1 were etched by deep reactive ion etching (DRIE) using the new Alcatel AMS-200 I-Productivity etcher at SINTEF MiNaLab. Aluminium masks were used for the first time using low frequency (LF) bias and were shown to have a higher selectivity when compared to the oxide masks. In the

case of through-wafer trenches, the achieved aspect ratio was as high as 58:1 and suppression of notching was also demonstrated by using LF bias.

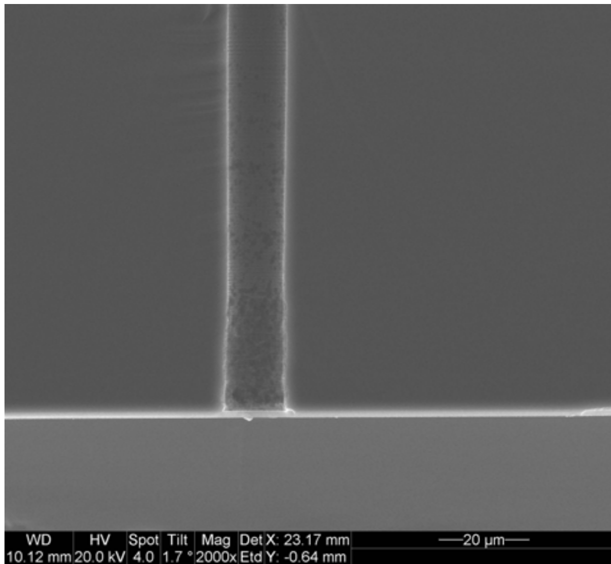

Fig. 12. SEM image of DRIE trenches, which are necessary for fabricating p+active edge electrode. The 5 µm wide trenches are 290 µm deep, giving an aspect ratio of 58:1.

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