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3D Integration Technologies

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***Abstract*-3D integration is a key solution to the predicted performance problems of future ICs as well as it offers extreme miniaturization and cost-effective fabrication of More than Moore products (e.g. e-CUBES®). Through Silicon Via (TSV) technologies enable high interconnect performance at relatively high fabrication cost compared to 3D packaging. A post backend-of-line TSV process is introduced as optimized technology for More than Moore products: The ICV-SLID process enables 3D integration of completely fabricated devices. Reliability issues, as thermo-mechanical stress caused by TSV formation and bonding are considered. The technology choice for the e-CUBES automotive application demonstrator is described.**

I. INTRODUCTION

Performance and productivity has been increased continuously over more then four decades due to the enormous advances in lithography and device technology. However, today it has become questionable if this so-called "More Moore" development alone will overcome the predicted performance and cost problems of future ICs. Moore's law will encounter the "red brick wall" somewhere in the 32 - 22 nm nodes. On one hand there are simply cost concerns e.g. related to extreme UV lithography. On the other hand, one of the fundamental issues of advanced devices is RC delay caused by the on-chip wiring. This objective leads to a major challenge for future IC fabrication requiring e.g. implementation of ultra low-k dielectrics for multilevel metallization. Unfortunately, the introduction of the corresponding technologies was delayed several times and SEMATECH stated in 2008: "Materials selection to the RC problem are drawing to close" [1].

The ITRS roadmap [2] shows 3D integration as a key technique to overcome this so-called "wiring crisis". The corresponding solution will most probably be based on through silicon via (TSV) technology as part of the Backend-of-Line rather than Frontend-of-Line related 3D integration or 3D packaging concepts (without TSVs). In addition to the enabling of further improvement of transistor integration densities ("More Moore"), 3D integration is a well-accepted approach for so-called "More than Moore" applications. Wireless sensor networks (e.g. e-CUBES® [3]) represent a typical example for such systems with the need for smart system integration of ICs, passive components and MEMS.

II. DEFINITIONS AND MOTIVATIONS

3D integration is generally defined as fabrication of stacked and vertically interconnected device layers. The large spectrum of 3D integration technologies can be reasonably classified mainly in three categories:

1. Stacking of packages (or substrates)
2. Die stacking (without TSVs)
3. TSV technology

According to the "Handbook of 3D Integration" the first two categories can be catalogued under "3D Packaging" and the latter is distinguished in "via first" and "via last" TSV technologies. "Via last" means fabrication of TSVs after stacking of devices [4]. What are the criteria for the technology choice? Naturally, cost will always be a main criterion for 3D integrated products (see Fig. 1). Besides form factor improvement, the key driver for TSV technology is certainly not low cost fabrication (estimated >400 US$ per wafer [5]) but the obtainable high performance enhancement compared to 3D packaging (3D SiP). On the other hand, TSV technology has the potential to be less costly than today´s state-of-the-art for mixed technologies products, monolithically integrated systems-on-a-chip (2D SoC).

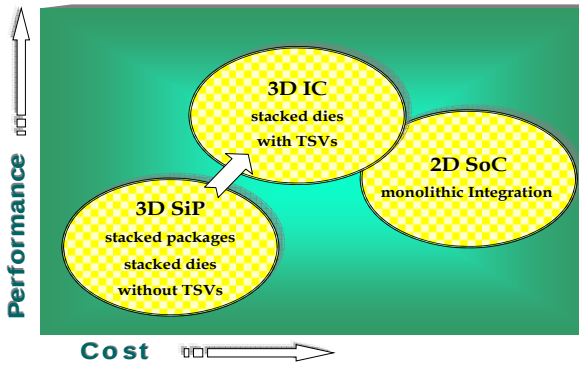

Fig. 1. Qualitative comparison of different system integration technologies in terms of interconnect performance and fabrication cost

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III. TECHNOLOGIES

In more than two decades, great research efforts were made in the area of 3D integration, starting in the 1980´s by e.g. IBM, NEC, Siemens and Fraunhofer. Since the early 90's Fraunhofer Munich has worked on stacking technologies using vertical inter-chip vias - ICVs (today´s common term: through silicon vias - TSVs), focusing on 3D integration concepts which take advantage of wafer level processing to achieve the highest miniaturization degree, excellent electrical performance and enable high volume cost-effective fabrication [6].

A "via first" post backend-of-line 3D integration technology (see Fig. 2) based on TSVs and stacking of devices by intermetallic compound bonding (ICV-SLID) has been developed and evaluated [6]. The enabling processes show up as more sophisticated while looking at production requests (e.g. TSV formation on fully processes IC devices with complex BEOL layer structures). Several characteristic features of deep reactive ion etching, deposition of dielectrics and metallization can result in reliability problems of high aspect ratio TSVs unless optimized processes, specific for TSV technology, are applied.

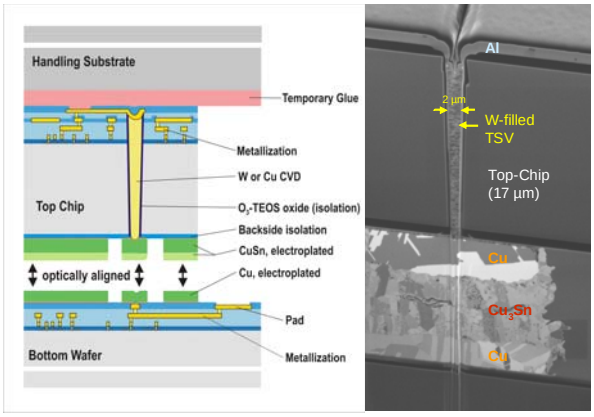

Fig. 2. ICV-SLID technology – a "via first" post BEOL TSV process [6]
Left: Schematic for aligned stacking of the thinned and stabilized top chip (with completely processed TSVs) to the bottom device wafer.
Right: FIB of a 3D integrated device stack, showing a cross section with CVD-W filled TSVs and the Cu_3Sn intermetallic compound bond layer which provides both the electrical and mechanical interconnect.

Especially for More than Moore products (which are fabricated by chip-to-wafer stacking of non-identical devices) the basic conditions for the application of intermetallic compound bonding have to be considered: critical topics are e.g. topography issues of devices and high mechanical stress which can be built into 3D-IC stacks by TSV formation and bonding processes. Corresponding process optimization is necessary to overcome these limiting conditions.

The qualification process for introduction of these new technologies into fabrication has to be accompanied by reliability evaluations, e.g. thermo-mechanical simulations taking into account the successive evolution of mechanical stress during processing [7]. The locations of highest loading during processing and operation (thermal cycling test) have been identified by monitoring stress and plastic strain building up due to thermal mismatch. It can e.g. be shown that in the case of W-filled TSVs, the maximum stresses and strains are observed in the upper part of the via between the IC metal layer and the tungsten filler. However, if W is replaced with Cu, the maximum stresses are located within the TSV itself. In consequence, process steps are adjusted to minimize stress in order to assure higher reliability.

Besides the TSV formation, the wafer bonding process can as well build high mechanical stress into a 3D-IC stack. This is of particular importance for More than Moore systems where in general ready-processed and thinned devices with different backend-of-line compositions (metals/dielectrics compound on thin silicon) are stacked. Variations of the lateral die dimensions will be "freezed" at the specific bonding temperature as a result of different thermal expansions. Depending on choice of technology, the bonding temperature can be far above room temperature (e.g. up to 400 °C for Cu-Cu bonding).

In general, not only *one* 3D integration technology is suitable for the fabrication of the large variety of 3D integrated systems. Moreover, even one single More than Moore product may need several different technologies for a cost-effective fabrication. Wireless sensor systems represent an excellent example for the need of a suitable mixture. Consisting of MEMS, ASICs, memories, antennas and power modules they can only be fabricated in a cost-efficient way by application of specifically optimized 3D technologies for the integration of the different sub-modules. Within the European Integrated Project e-CUBES [3] a variety of 3D integration technologies was developed to realise extremely miniaturized wireless sensor nodes. Fig. 3 shows schematics of three of the 3D integration concepts that were implemented in application demonstrators (processes and characteristics are described in [3]).

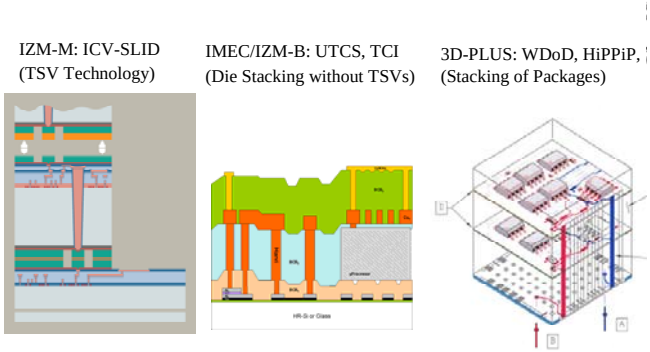

Fig. 3. 3D integration concepts for the fabrication of e-CUBES application demonstrators (miniaturized wireless sensor nodes)

The enabling technologies are optimized for the 3D integration of the application layer, consisting of a processing unit and a sensor function. The sensor node which has been selected for the demonstration of a 3D integration concept for

automotive application represents a tire pressure monitoring system (TPMS) [8]. The key element of the complete system is a three-layer die-stack composed of a microcontroller, an RF transceiver and a pressure sensor as shown in Fig. 4. The transceiver die and the cap of the sensor die are processed with TSVs and matching routing and interconnection layers on relevant sides. The ICV-SLID technology was optimized for fabrication of e-CUBES processing units (3D-ICs). Au stud bump bonding (SBB) and silicon TSVs in silicon-glass compound wafers were applied and evaluated for stacking of sensor devices to 3D-ICs (see Fig. 4). Au SBB combined with TSVs based on silicon is cost-effective for devices with low I/O counts and moderate demands for conductivity.

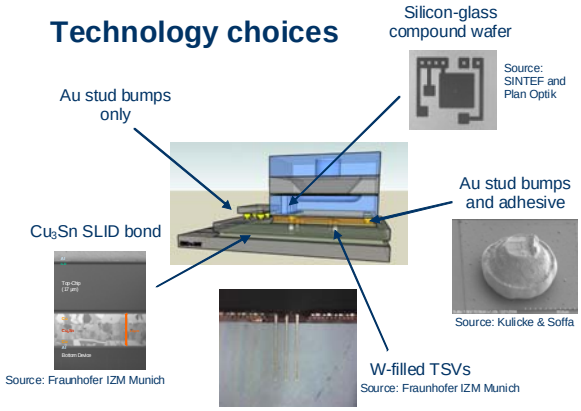

Fig. 4. Enabling technologies for the e-CUBES® automotive application demonstrator – 3D-IC/sensor stack of a TPMS wireless sensor node

IV. CONCLUSIONS

Cost is certainly a key driver for 3D integrated products, but primarily on a long term, as e.g. for More than Moore systems. The situation will depend strongly on application and markets. Performance and density of functionality are expected to be the short and/or mid term drivers. However, manufacturability and reliability of 3D fabrication processes are the basic requirements that guide the choice of the technology. Although there are significant challenges regarding the introduction of 3D integration technology to production lines, no real "show stopper" has been identified.

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