3D DETECTOR ACTIVITIES AT SINTEF MINALAB – WAFER BONDING AND DEEP REACTIVE ION ETCHING

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ABSTRACT

Near term and future experiments in high-energy physics and molecular biology will require radiation hard and fast detectors with sensitive border to cope with the increasingly stringent research requirements. 3D detectors, with vertical electrodes penetrating through the entire silicon substrate have drawn high interests for these applications due to their unique advantages such as ultra-fast time response, edgeless capability and radiation hardness. In addition, the through-wafer electrode technology can provide the possibility to connect 3D detectors on a wafer level via 3D interconnects [1, 2]. Since its introduction by S. Parker and C. Kenney in 1995 [3], several laboratories have begun research on 3D processing technology. Besides their advantages, fabrication of 3D detectors remains non-trivial and has only been possible since the successful developments in wafer bonding and deep reactive ion etching (DRIE). The edgeless capability is achieved by etching a through-wafer trench that surrounds an entire detector, and is then filled with highly doped silicon to form an active edge electrode. The process wafer must be bonded to a support wafer prior to the etching. Moreover, following polysilicon deposition, the process wafer is subject to severe mechanical stress and risk of cracking, making the support wafer even more necessary. At SINTEF MiNaLab, the first prototype run started in 2007, with an emphasis to demonstrate the feasibility to fabricate full 3D detectors with active edge on a production scale. During this run, wafer bonding was used to facilitate the etching of trenches and to provide mechanical support to the process wafer. A deep reactive ion etching process was also developed to etch 14 μm round holes through 250 μm thick silicon wafer. The first run is now fully completed and preliminary results are promising. Good p-n junction characteristics have been shown, and a leakage current of less than 0.5 nA per pixel was measured on selected devices. SINTEF is now the second laboratory who has successfully fabricated 3D detectors with active edge and is the first who attempted to fabricate on a production scale. This paper discusses the processing issues encountered in this first prototype run, with a focus on two important processes; wafer bonding and deep reactive ion etching (DRIE).

Keyword: 3D detector, wafer bonding, deep reactive ion etching, 3D interconnect, silicon sensor

INTRODUCTION

Many future experiments in high energy physics and molecular biology require fast signal response, high radiation tolerance and full area sensitivity. These applications include X-ray imaging for molecular biology and particle tracking using silicon detectors, such as those used in the Large Hadron Collider [21] at CERN, Switzerland. In some experiments, the sensitivity of the detector has to be within 50 μm from its physical edge, which is almost 10 times smaller than the established standard planar detector technology [15]. 3D detector (Fig.1), with vertical electrodes penetrating through the entire silicon substrate has drawn high interests in these applications due to their unique advantages. In addition, the through-wafer electrodes offer the possibility to connect the detectors to readout electronics via 3D interconnects. Such interconnects contribute less parasitic capacitance and inductance than conventional wire bonding and flip chip bump-bonding to the overall detector system, reducing the necessary signal processing time [22].

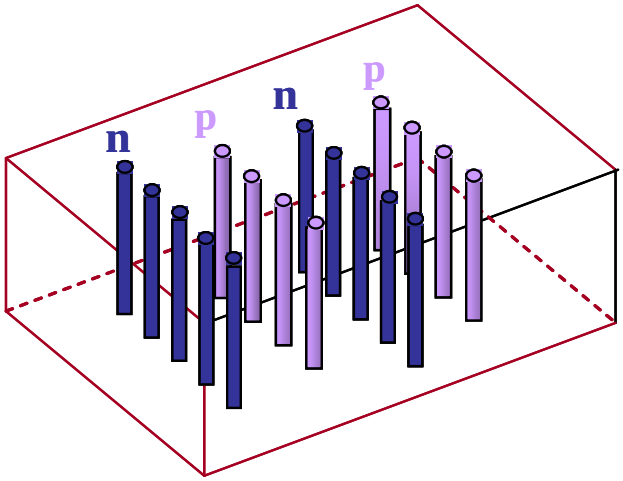

Fig.1: The concept of 3D detector is to have both the p and n electrodes penetrating through the entire substrate.

The distance between the n and p electrodes in a conventional planar silicon detector is limited by the wafer thickness. In simple terms, the induced signal generated by an ionising particle is proportional to the thickness of the detector that the particle traverses through. In most applications, the detector thickness ranges between 300 μm and 500 μm in order to maintain an acceptable signal-to-noise-ratio. The p to n electrode distance is therefore also 300-500 μm in a planar silicon detector. On the contrary, the inter-electrode distance in a 3D detector is independent of the wafer thickness and can be made to be as short as 50μm, resulting in much shorter average drift lengths for the generated electrons and holes upon incident radiation. Moreover, the ionisation path of the incident particle is also parallel to the collecting electrodes as shown in Fig.2. Ignoring some diffusion spreading, the arrival of all charges is simultaneous, inducing a signal that is much faster when compared to that in a planar silicon detector. Preliminary test results have verified the fast signal response in 3D detectors and can be found in ref. [12] and [16].

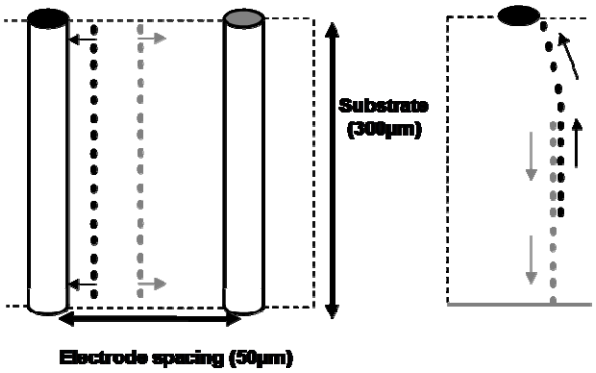

Fig.2: Collecting electrodes of 3D detector (left) are almost parallel to the particle track and all charges generated from the track have similar collection times while induced signal is spread out in time for a planar device.

The second advantage of 3D detector is radiation hardness. Having radiation hard silicon detectors remains a challenge for many future particle experiments [14]. Upon irradiation, the silicon lattice is damaged and defects are formed, which act as trapping sites for mobile charge carriers that are generated by incident particles. The effective drift length of the mobile charge carriers therefore reduces to less than 50 μm after heavy irradiation [9]. As a result, the induced signal becomes smaller and would most likely be lost in a conventional planar detector where the electrode spacing is typically 300μm. In contrast to planar detectors, the inter-electrode spacing in a 3D detector is comparable to the reduced effective drift length while keeping the wafer thickness at 250-300 μm, to have a good signal-to-noise ratio [9].

Another advantage of 3D detector full area sensitivity right up to the detector's physical edge. In conventional planar detector, a guard ring is necessary to maintain a uniform electric field and to prevent breakdown along the edges, as shown in Fig.3c. The necessity of the guard ring is due to the chips and cracks along the edges of the detector from traditional saw dicing. In 3D-active edge detector, the detectors can be separated by plasma etching a through-wafer trench that surrounds the entire detector. The resulting physical edge is smooth and the trenches are

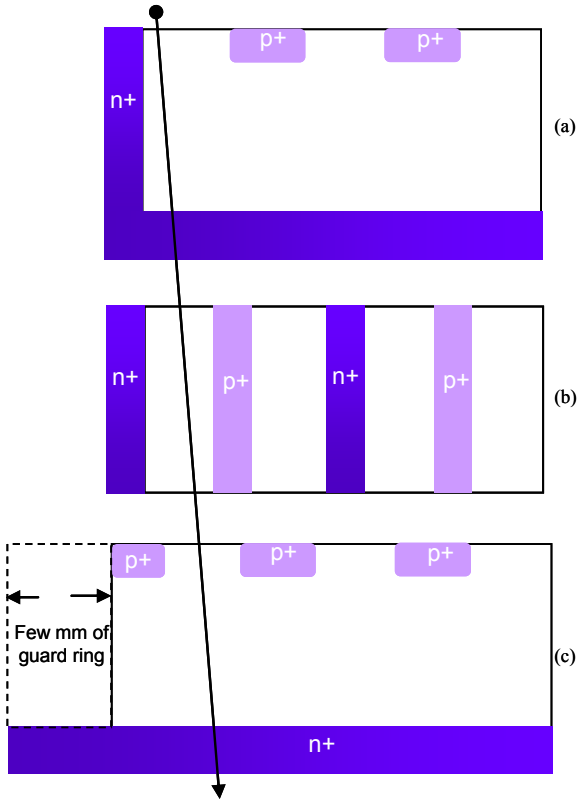

Fig.3: (a) Planar 3D – active edge combined with a conventional planar detector; (b) 3D detector with active edge (c) conventional planar detector with a few mm of guard ring which is insensitive to radiation particles.

doped and filled with polysilicon, forming an electrode all around the physical edge of the detector. Incident radiation particles that traverse close to the physical edge can therefore be collected efficiently by the so-called 'active edge' electrode shown in Fig.3 [7, 8]. This technology can also be combined with conventional planar technology, the so-called 'planar-3D' (Fig.3a), which can be used in applications where radiation hardness is not the main issue, but are crucial to have full area sensitivity. The unique property of 3D detector and active edges has been tested. Earlier results and further details can be found in Ref. [3-13].

3D TECHNOLOGY OVERVIEW

3D detector was proposed by C. Kenney and S. Parker in 1995, and was successfully fabricated in 1997 [4]. Since then, many laboratories have begun research on 3D detector technology. However, the combination of MEMS, wafer bonding, thick poly deposition, implies a great challenge if to produce on a production scale, and C. Kenney et al remain as the only successful fabricator of full 3D detectors with active edge. The feasibility to transfer the technology to a production environment is therefore of great interest to many but yet to be explored. SINTEF MiNaLab owns several state-of-the-art plasma etching tools, and together with other well-established in-house silicon processing techniques, MiNaLab is an ideal laboratory to fabricate 3D detectors on a production scale.

The first 3D detector prototype at SINTEF MiNaLab began in 2007, after collaboration with C. Kenney et al was established in 2006. The process developed by C. Kenney et al [4] was adapted, but in order to transfer the technology to a small production scale where most processes are well controlled and handled by automatic robots, modifications to the original process were necessary. In this first run, 25 double-sided polished n-type (100) wafers with a resistivity of 2000 Ωcm were used. A 1µm thick thermal oxide was first grown on the process wafers, necessary for further processing. The process consisted of wafer bonding, 7 lithography steps and 2 separate deep reactive ion etching steps. The n-type electrodes were first etched and filled, and were protected by a 3000Å thermal oxide barrier while processing the p-type electrodes. Once the electrodes were formed, a metal layer was deposited and patterned. A passivation layer consisted of 0.5 µm PECVD oxide and 0.25 µm PECVD nitride was then deposited and patterned as the final step. Fig.4 summarises the entire process.

WAFER BONDING

Bonding to a support wafer relieves some of the mechanical stress suffered by the process wafers after deep reactive ion etching and thick polysilicon deposition. It is also necessary to have a support wafer when fabricating detectors with active edge, where the detectors would detach from the process wafers once the active trenches were etched away without the presence of a support wafer.

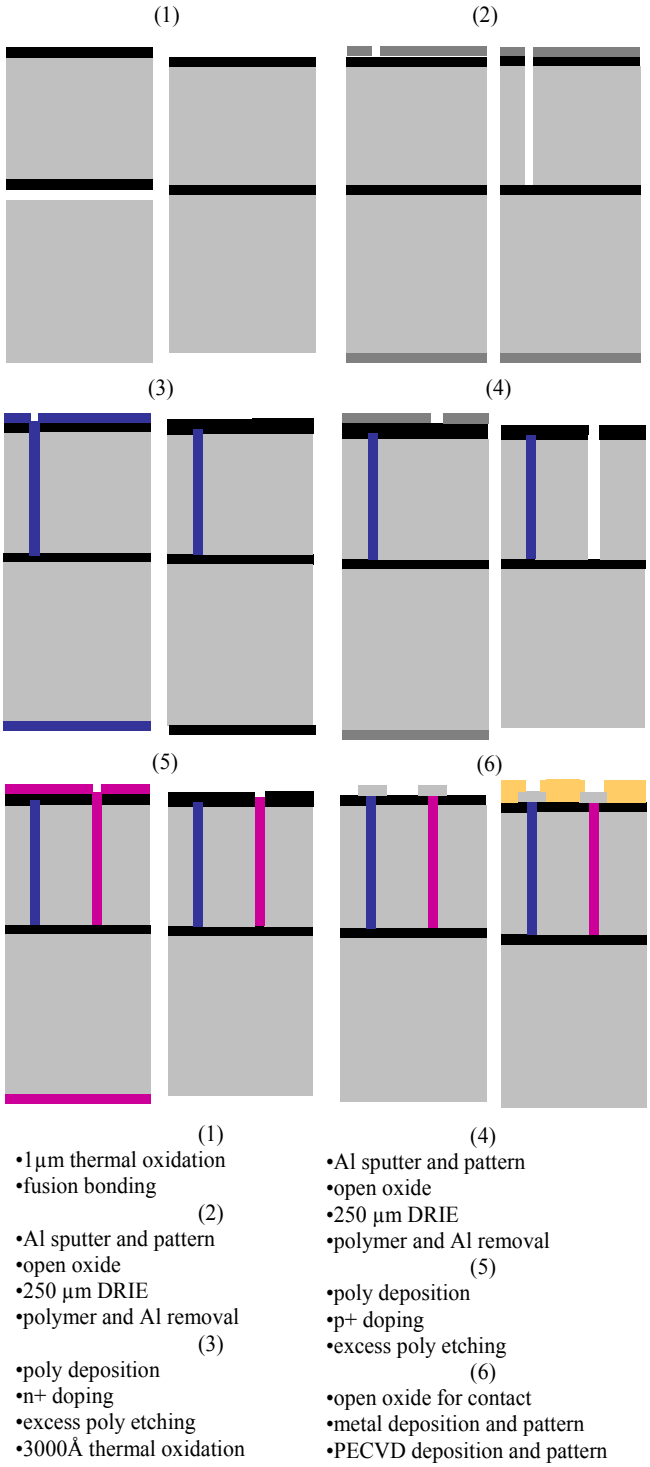

Fig.4: Summary of fabrication steps for the first 3D prototype run at SINTEF.

Prior to wafer bonding, a 1 μm thermal oxide was grown on the process wafer surface, and the support wafers remained non-oxidised, which were 350 μm thick. Direct fusion bonding of hydrophilic surfaces was used, which is a well-established process at SINTEF MiNaLab [17]. The hydrophilic surfaces were first prepared by a standard RCA clean, removing any organic and inorganic substances from the surfaces. The wafers were then rendered to be even more hydrophilic by immersion in a piranha bath which contained sulphuric acid and hydrogen peroxide at 130°C for 15 minutes. This was then followed by a 15 minutes rinse in deionised water. An additional rinse with deionised water in the SUSS cleaner CL6 was then given right before the pre-bonding took place in the SUSS substrate bonder SB6. Once the wafers were aligned, the SUSS bonder clamped the two wafers together until the pressure was pumped down to below 5 E-3 mbar. A standard temperature of 50°C was kept on the chuck throughout the pre-bonding process. The pre-bonded wafers were then annealed in a diffusion oven filled with nitrogen at 1050°C for 2 hours.

Fig.5 shows the infra-red images taken before and after annealing of a pre-bonded wafer using our custom made infra-red lamp set up. The voids and the poorly bonded regions were improved after annealing as shown in Fig.5b. 9 wafers in this batch had one small void. Each void contributed less than 1% of the total surface area. One typical example is shown in Fig.5c. In some cases, the wafers became perfectly bonded after annealing, such as that shown in Fig.6a and Fig.6b. In the entire batch of 25 wafers, 10 wafers were perfectly bonded after annealing, and 9 wafers had one small void, giving an overall high bonding yield.

Although the bonding results were excellent, precaution was taken in all subsequent high temperature oven processes by ramping up and down the temperature over a period of several hours, in order to avoid damages caused by thermal expansion of any trapped air or humidity in the bonding voids. By the end of this prototype run, no wafer breakage occurred in any high temperature process, confirming the high quality of wafer bonding. The wafer

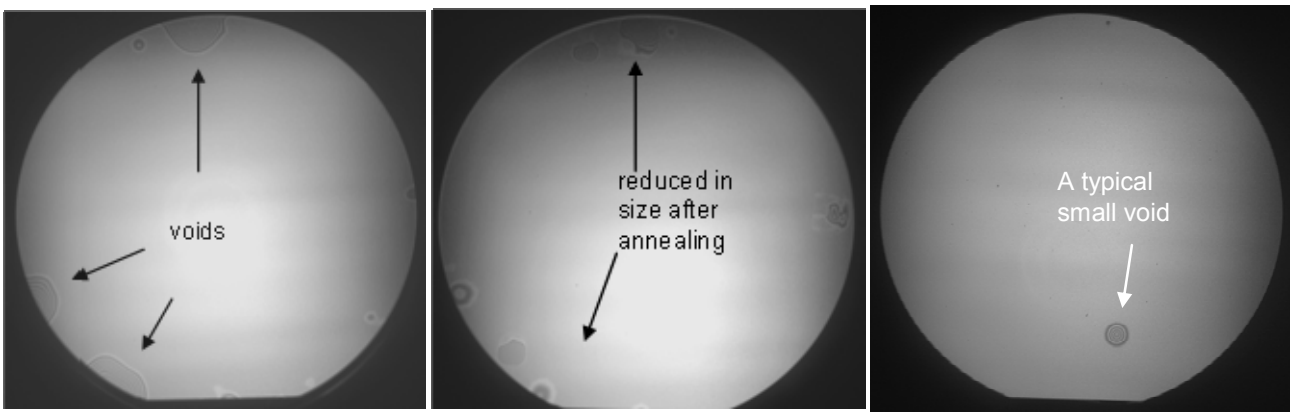

Fig.5a (left): Several poorly bonded areas were clearly observed after pre-bonding. **Fig.5b (centre):** The bonding improved after an annealing time of 2 hours at 1050°C, the voids became significantly small. **Fig.5c (right):** The small void shown is a typical void observed in the 9 wafers where small defects were found after annealing.

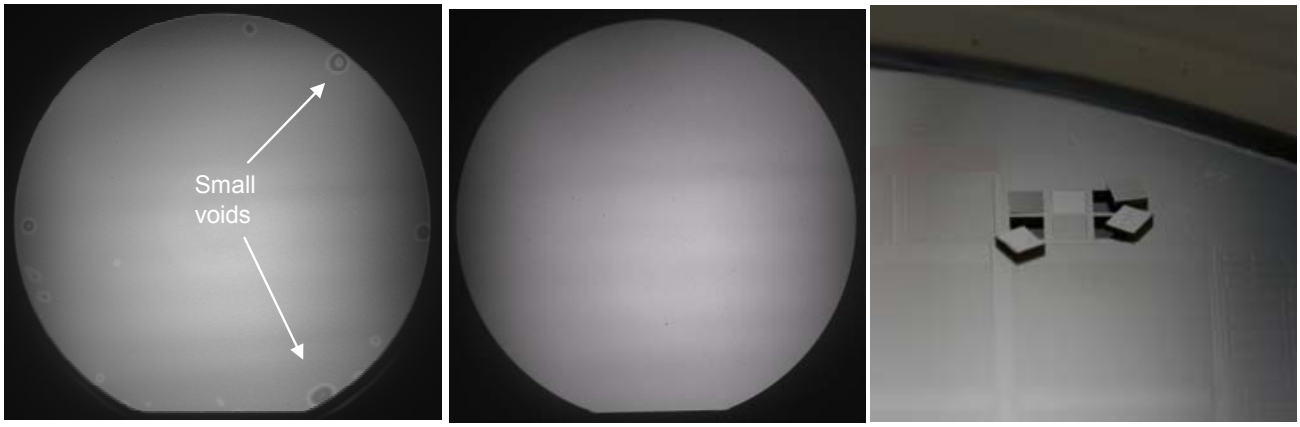

Fig.6a (left): Small voids were observed before annealing. **Fig.6b (centre):** The wafer appeared to be perfectly bonded after 2 hours of annealing at 1050°C in nitrogen. **Fig.6c (right):** Detectors detached from the bonded wafer where bonding was poor.

bonding was also tested when the through-wafer trenches were etched. Once the through-wafer trenches surrounding the detector were etched, any sensors that were on top of a void in the poorly bonded region would immediately detach from the support wafer once the trench was etched through. Fig.6c shows how some sensors detached from the support wafer. This, however, only occurred in 2 wafers in the entire batch, indicating that the majority of wafers were very well-bonded. Fig.6c is also a perfect demonstration of how plasma etching can be used to separate the final detector. In addition, one wafer was successfully diced using traditional sawcut dicing to reassure the wafers were well bonded.

DEEP REACTIVE ION ETCHING (DRIE)

Deep reactive ion etching (DRIE) is the key technology in 3D detector processing. At SINTEF MiNaLab, through-wafer holes with an aspect ratio of up to 15 were previously demonstrated using an Alcatel AMS-200 etcher [20] with a modified Bosch Process [19]. The process parameters are usually altered according to the requirements for each specific application. The design of 3D detectors had round through-wafer electrodes with a diameter of 14 µm. A 1.5 µm thick aluminium was used as the etchmask and was patterned using standard lithography with edge bead removal. The wafer edge was then protected by a custom made metal clamp placed inside the etching chamber. Once patterned, the round holes in the aluminium masks became 16 µm wide due to

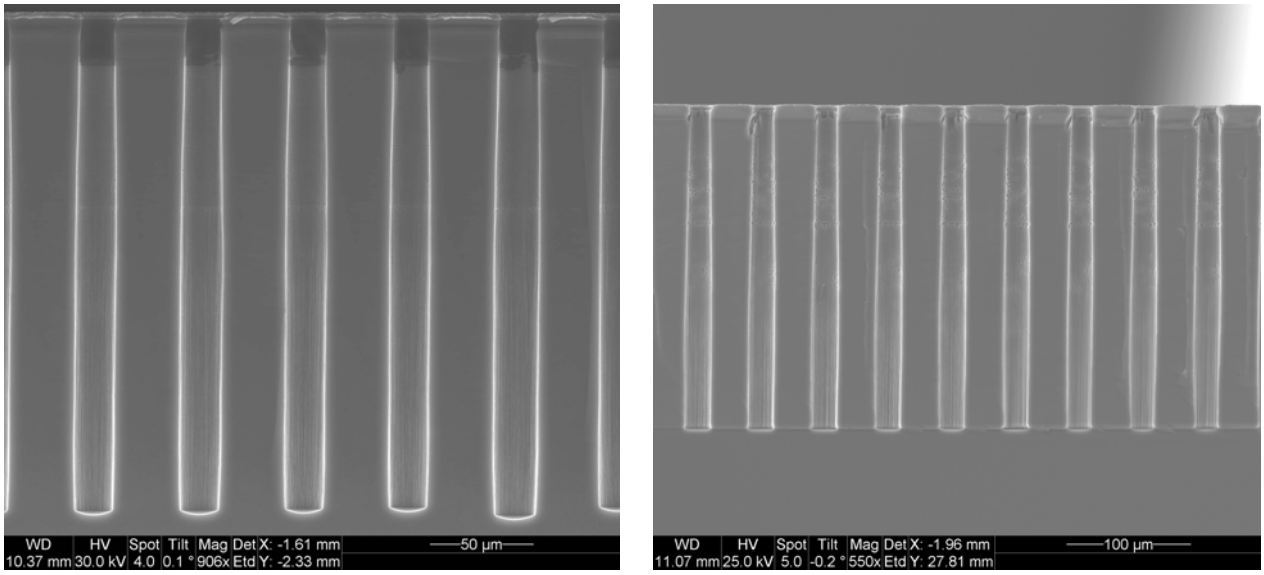

Fig. 7a (left): Cross section of 250 µm deep round through wafer holes in a 500 µm thick test wafer. **Fig.7b (right)**: Cross section of through holes in a 250µm thick wafer bonded to a support wafer.

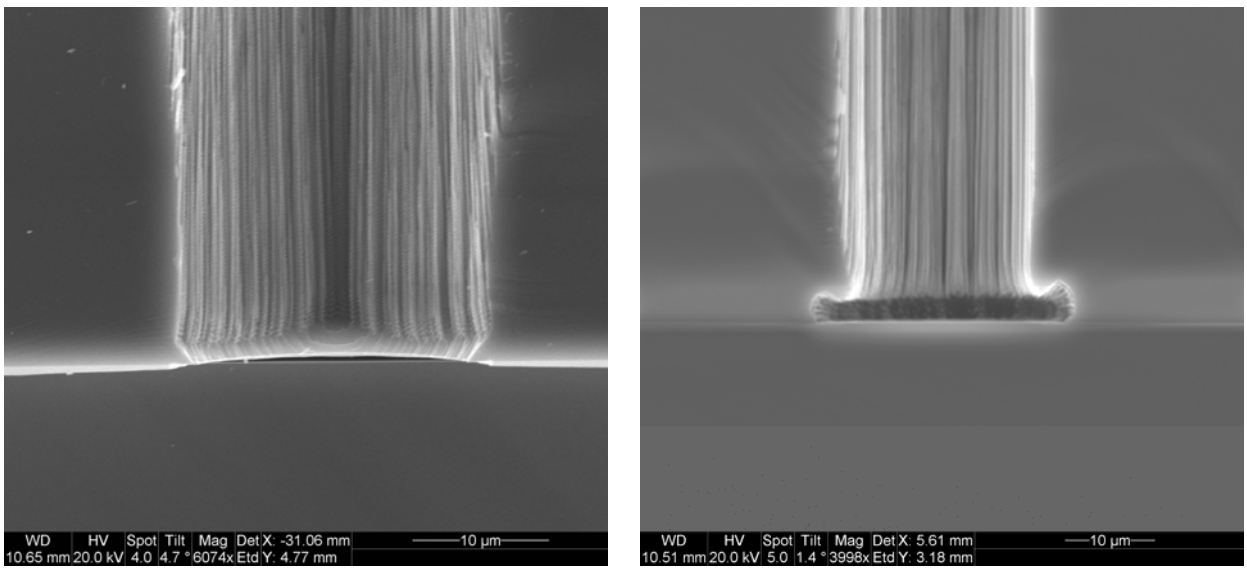

Fig.8a (left): A very smooth profile at the bottom of the hole attached to the support wafer when the etch time was just long enough to etch through. **Fig.8b (right):** Severe notching was observed when the etching was 10 minutes longer.

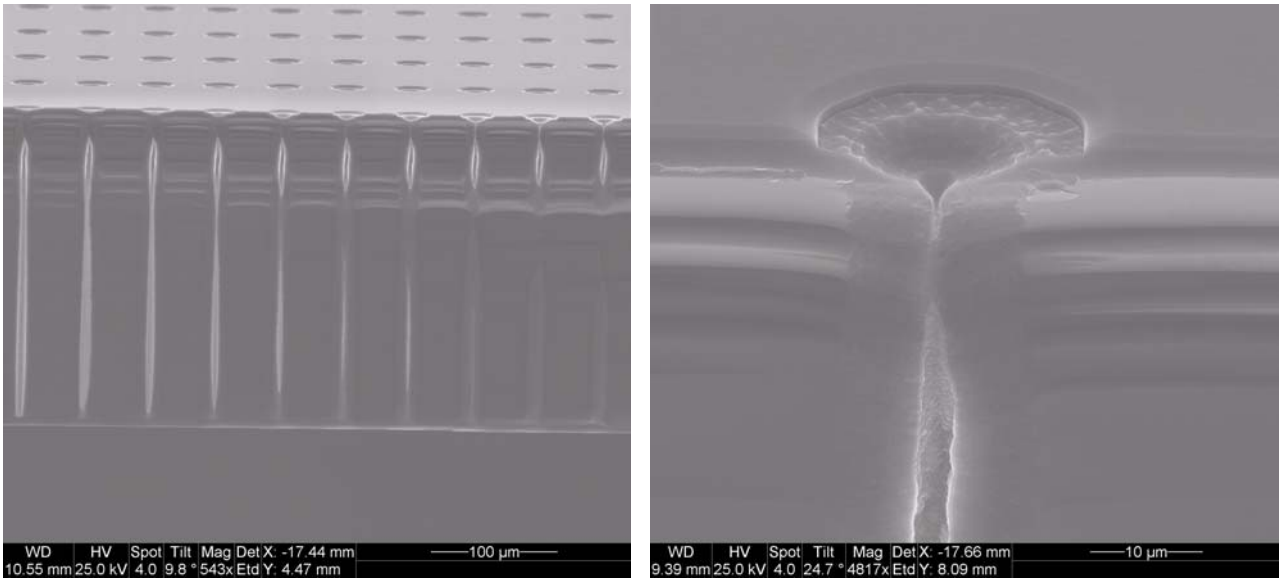

Fig. 9a (left): Due to the holes profile, a void in the poly was observed in the cross section of the filled through holes. **Fig.9b (right):** A cross section which shows the topography on the top of the hole after the removal of poly on the surface using plasma etching. The void in the poly was also clearly observed.

the isotropic nature of a wet chemical etch. These round holes were then further widened after the DRIE process and became 18 µm wide, giving an overall aspect ratio of 14:1. Fig.7a shows a SEM image of 250 µm deep through holes in a 500µm thick test wafer. Considering the measurement error, both the bottom and the top of the holes had a diameter of approximately 18 µm, the profiles were rather cylindrical. All polymer residues were removed by O_2 plasma stripping and the aluminium mask was removed by a piranha rinse.

The same process was then tested on a 250 µm thick wafer bonded to a 350 µm thick support wafer. The etching profiles were similar (Fig.7b) to those obtained in a 500 µm thick wafers, except at the bottom of the holes. Once the process wafer was etched through, the 1 µm oxide between the process and the support wafer was charged up by excess ions. The oxide charge then deflected the etching ions, and the ions etched the sidewalls at the bottom, resulted in severe notching at the bottoms if over-etched excessively, as shown in Fig.8b. Such notching could form regions of high electric field, and could easily result in high leakage current and low breakdown voltage, thus lowering the detector's performances. Several test runs were used to determine an etching time that was long enough to etch through the wafer while keeping the notching effect to a minimum. Fig.8a shows how the notching was reduced after reducing the etching time by 10 minutes.

POLY DEPOSITION

The n and p-type electrodes were formed by filling the through-holes with highly doped polysilicon. A layer of 1 µm poly was first deposited and was doped by gas-phase doping. Several subsequent layers of 2 µm poly were then run separately until the holes were fully filled. The LPCVD furnace at SINTEF MiNaLab can currently deposit a layer of polysilicon up to 1 µm at a time. Filling the through holes with polysilicon was estimated to take a minimum of 70 hours. The etched holes were therefore filled at Stanford Nanofabrication Facility where our collaborator was able to deposit a layer of polysilicon up to 2 µm at a time. Fig.9 shows the results of the polysilicon deposition. Although the polysilicon deposition was known to be rather conformal, voids and keyholes were observed in the cross section of the holes, mostly caused by the variation in the etching profiles.

FABRICATION ISSUES

Difficulties in lithography steps were experienced once the wafers were filled with polysilicon, mainly in resist coating and in the handling by automatic tools.

The excess polysilicon on the wafer surface was etched by plasma etching, which was rather isotropic in order to have a uniform etch rate across the wafer surface. This, however, created topography on top of the electrodes and the active trenches. Coating a uniform resist layer over such topography was challenging and a high viscosity resist had to be used.

In this first run, the support wafer was not oxidised prior wafer bonding. The oxide could act as an etch stop during the etching of excess poly and could preserve the integrity of the backside of the wafers. Without this oxide, the wafers suffered from high mechanical stress due to any poly residue on the backside and an uneven oxide distribution between the front side and the back side. Fig.10 compares the warping of a 3D wafer to a standard pre-processed wafer, and the 3D wafer had a

curvature 10 times larger than the standard wafer. Handling such wafers was difficult when using automatic robots. As a result, many wafers were broken, reducing the yield significantly.

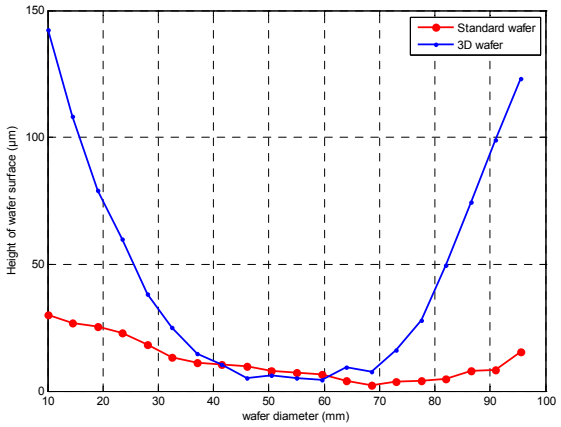

Fig.10: A 3D wafer after polysilicon deposition bowed at a curvature 10 times larger than a pre-processed standard silicon wafer.

ELECTRICAL MEASUREMENTS

Despite the difficulties towards the end of the process, two wafers are now fully completed. The IV characteristics of several full-size (8 by 9 mm^2) ATLAS [23] pixel detectors have been measured. Each full size ATLAS detector contains more than 1000 pixels, and each pixel consists of 4 n-type electrodes. The p-type electrodes and the active edge are joined together by a single metal connection. Fig.11 shows how the electrodes and active edge were arranged. The IV characteristics for 4 selected detectors are shown in Fig.12, when the detector was reversed biased. The leakage current increases gradually and reaches a plateau at about 15 V, showing a good p-n junction characteristic. These detectors were made on an n-type substrate. Thus, the total dark current for the entire detector including the active edge was picked up when measuring on a single n-type pixel. The measurements shown here have been scaled, and correspond to the current per pixel. In these 4 particular detectors the leakage current when fully depleted is about 1 nA, which is fully compatible with the designed readout electronics for this particular application. The breakdown voltage was also measured to be 80 V. A leakage current of less than 0.5 nA per pixel was measured on a detector with a slightly different design where each pixel consists of 3 n-type electrodes, as shown in Fig. 13. 10 detectors from this wafer are currently being bump-bonded to the ATLAS readout electronics for further characterisation later this year.

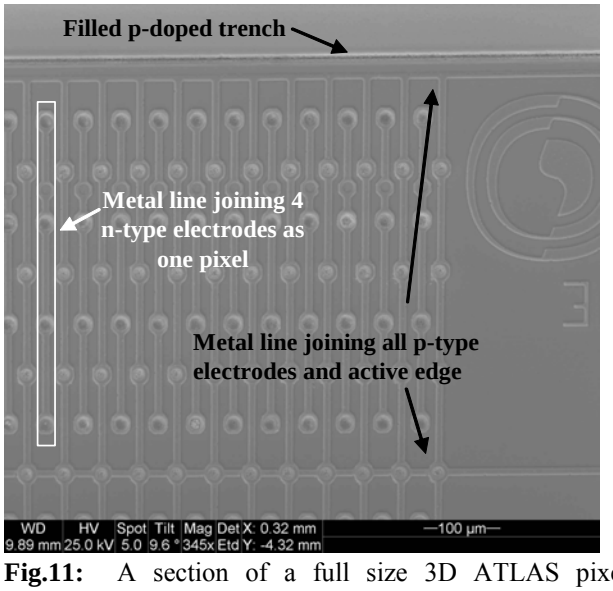

Fig.11: A section of a full size 3D ATLAS pixel detector, showing a pixel consists of 4 n-type electrodes. The p-electrodes and the active edge are joined by a single metal connection.

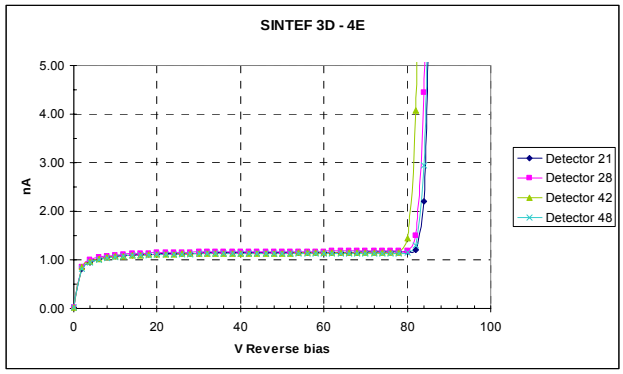

Fig.12: IV curves measured on 4 different detectors. All pixels consist of 4 electrodes and the leakage current is about 1 nA.

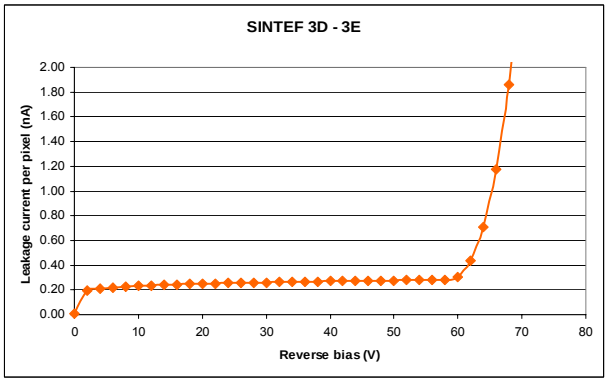

Fig.13: An IV curve measured on a pixel consists of 3 electrodes and the leakage current is lower than 0.5 nA.

CONCLUSIONS

3D detectors with active edge were successfully fabricated at SINTEF MiNaLab. Measured results show a good diode characteristic with a leakage current of less than 0.5 nA per pixel on selected devices. Wafer bonding was shown to be extremely successful, contributing a small

portion of failed chips. In the batch of 25 wafers, 19 were either perfectly bonded or with one tiny void, when inspected using an infra-red lamp. An overall high bonding yield was achieved. Excellent deep reactive ion etching process was also developed to provide electrodes with good profile as well as excellent aspect ratio. Several modifications must however, be introduced in order to fabricate 3D detector as a small production effectively. This will be explored in our next run, for example by having a thermal oxide on the support wafer prior wafer bonding to reduce the stress subject by the bonded wafer. Chemical mechanical polishing (CMP) can also be used to have a smoother surface on top of the electrodes. If this is successfully demonstrated, SINTEF offers a possibility to fabricate a high-performance detector at an affordable cost for many large silicon detector systems, such as the ATLAS [23] inner tracker at CERN in Switzerland. Further characterisations using ATLAS silicon tracker readout electronics are scheduled later this year where we will explore the active edge characteristic and signal formation in 3D detector. In addition, our next fabrication run is due to begin this fall.

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