Latest Results From 2nd SINTEF 3D-Run

3D-Processing Meeting November 26, 2009

T. E. Hansen, A. Kok, T. A. Hansen, N. Lietaer,
G. U. Jensen, A. Summanwar

MASK LAYOUT FOR 2nd RUN

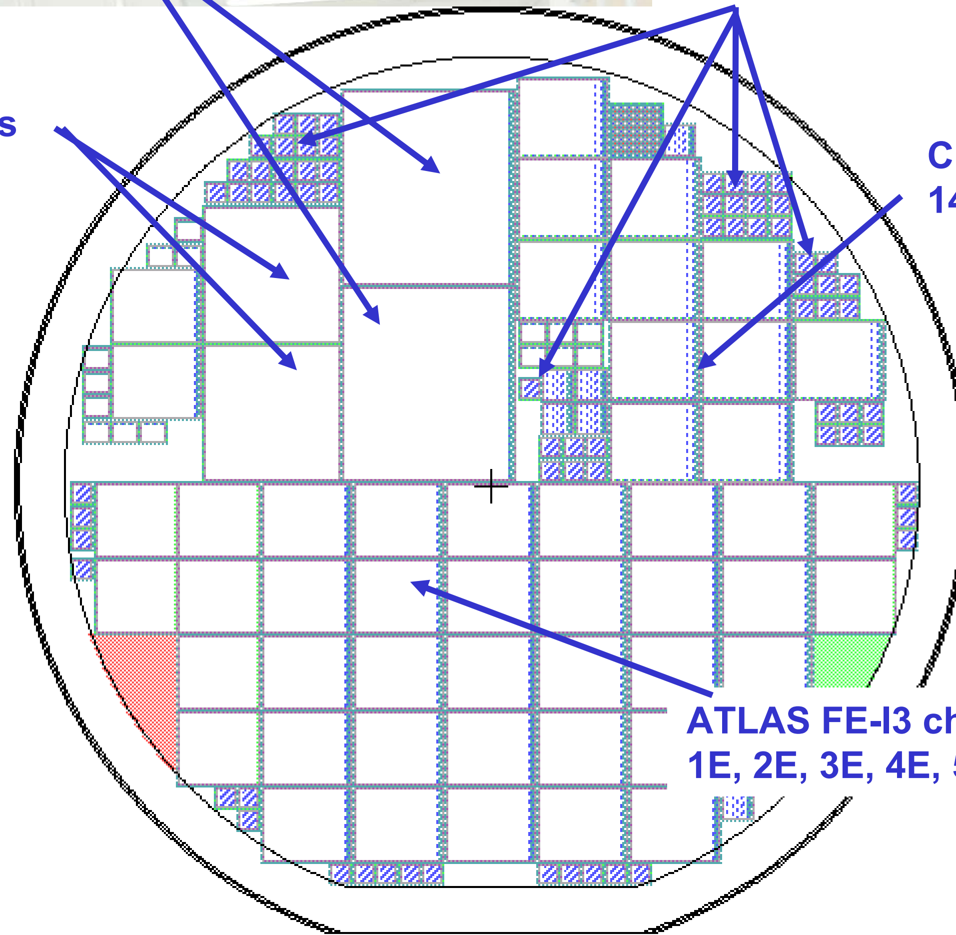
Includes ATLAS, CMS and Medipix type devices.
1E, 2E, 3E, 4E and 5E configurations

Atlas FE- I4 chips
2E configuration

1E, 2E, 3E, 4E, 5E test structures

Medipix chips

CMS 1ROC, 2E, 4E configurations
14.6 % of wafer area



ATLAS FE-I3 chips
1E, 2E, 3E, 4E, 5E configuration

ATLAS pixels: 4E -, 3E -, 2E – configurations

2.nd run also included 1E and 5E configurations

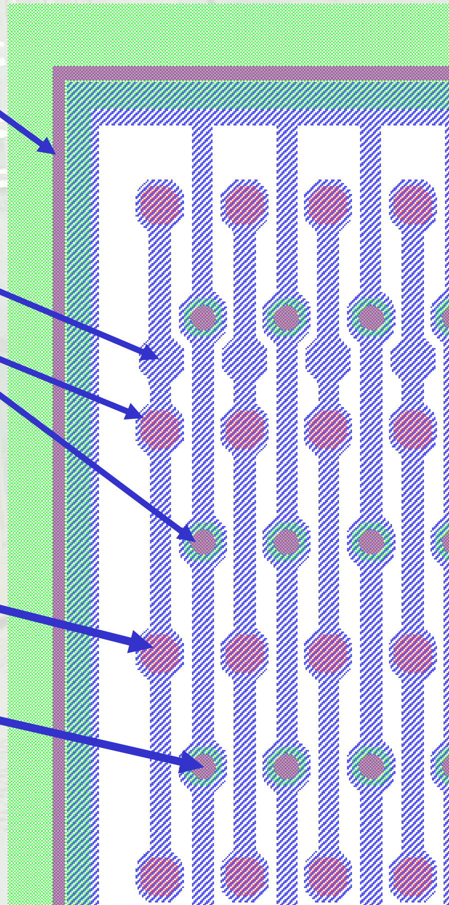
4 or 7 µm trench (active edge)

pad for bump-bonding

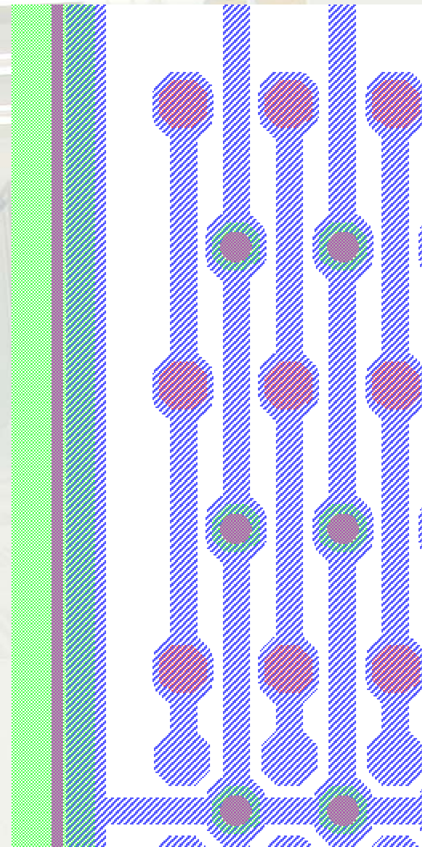
14µm holes

n-readout electrodes

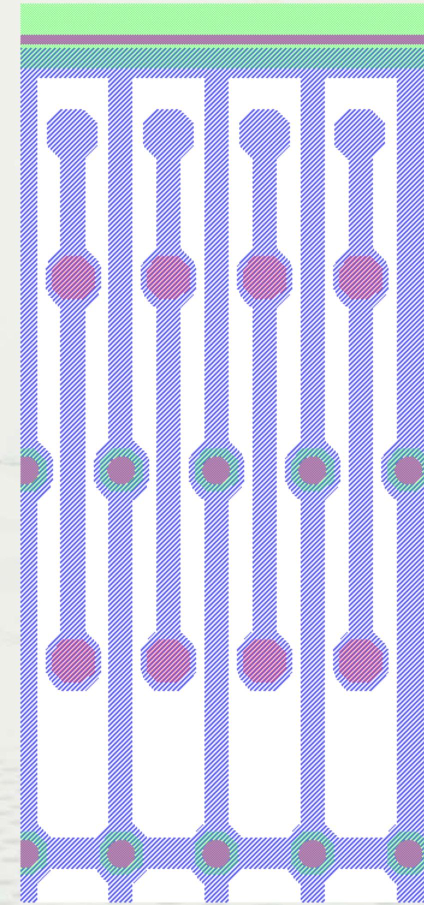
p-bias electrodes



4 electrodes per pixel – 4E



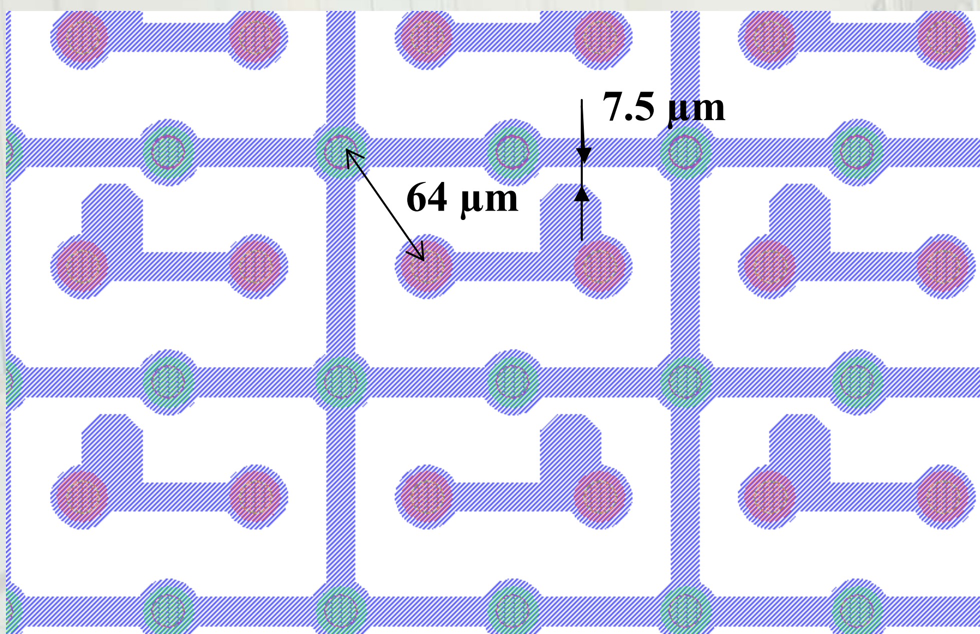
3 electrodes per pixel – 3E



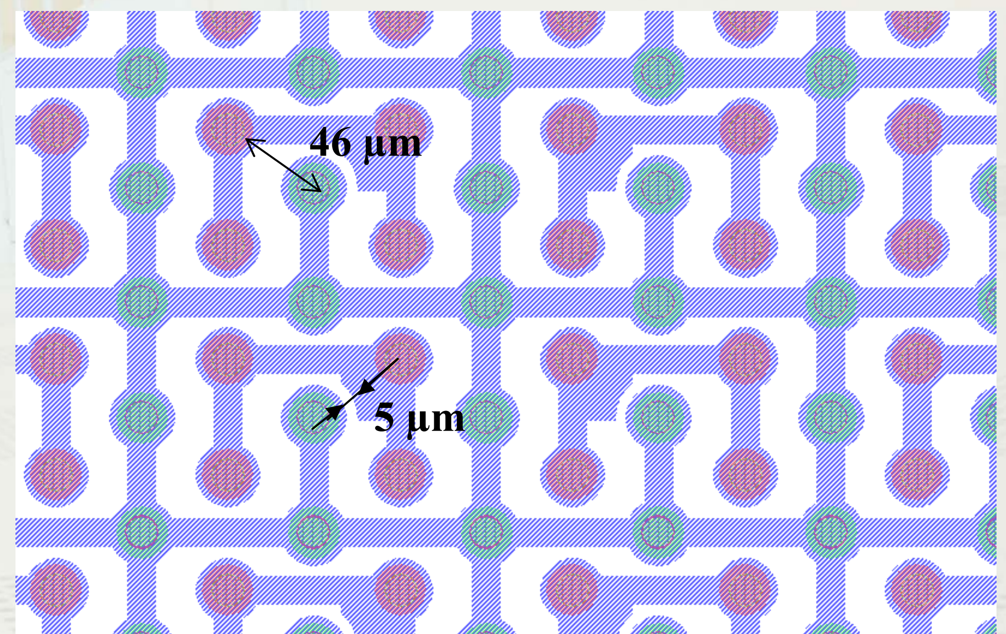
2 electrodes per pixel – 2E

CMS 1ROC 2E and 4E configurations

Original design by Gino Bolla, slightly modified by SINTEF



2E configuration



4E configuration

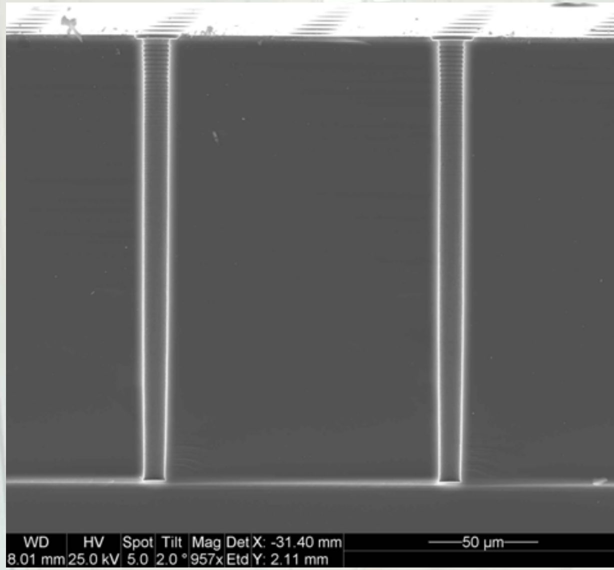
Configuration geometries and estimated depletion voltage

Substrate specific resistivity: ≥ 10000 Ωcm							
Configuration	ATLAS					CMS 1ROC	
	1E	2E	3E	4E	5E	2E	4E
n - p electrode distance (μm)	201	106	76	54	47	64	46
Max depletion voltage planar model	40.5 V	11.3 V	5.8 V	2.9 V	2.2 V	2.2 V	4.1 V
Max depletion voltage square cell model [1]	190 V	32 V	11.8 V	3.9 V	2.4 V	6.9 V	2.4 V [2]

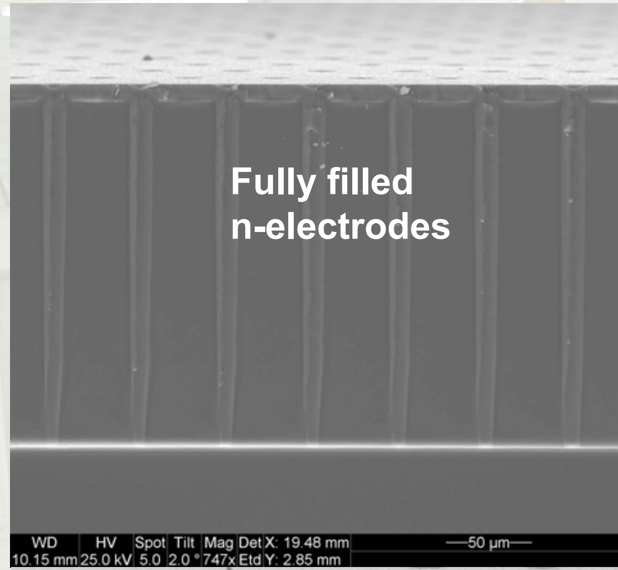
1. V. Eremin, E. Verbitskaya, “Analytical Approach for 3D Detectors Engineering”, 2008 IEEE Nuclear Science Symposium conference Record
2. Square cell model should apply well to 1ROC 4E configuration

Fabrication steps – second 3D-run

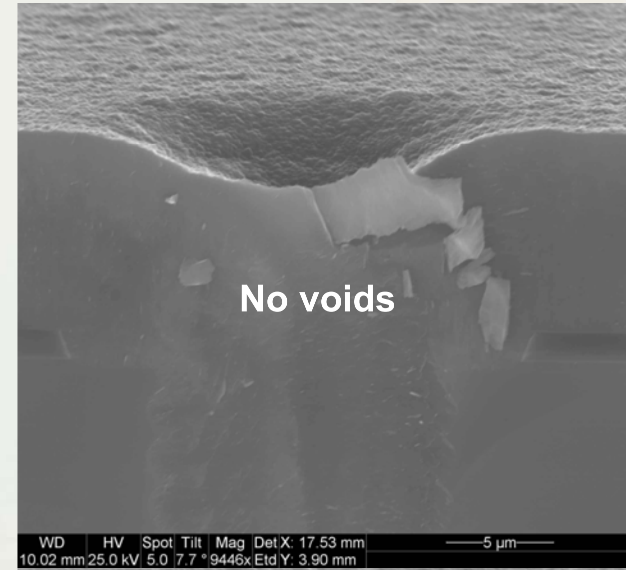
After DRIE

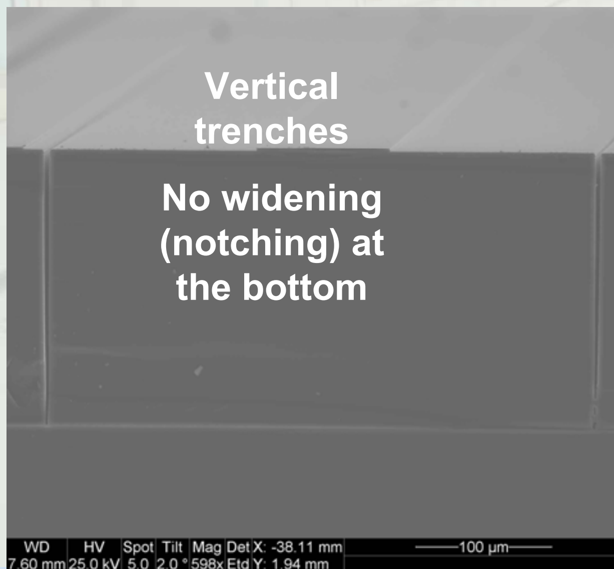


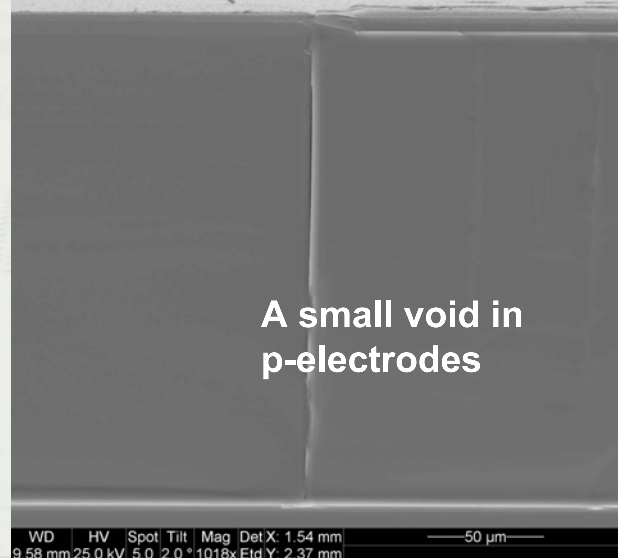
After poly filling

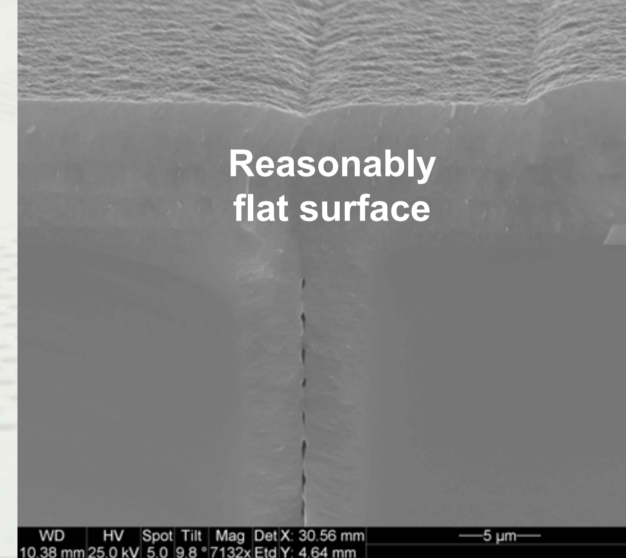


After poly filling



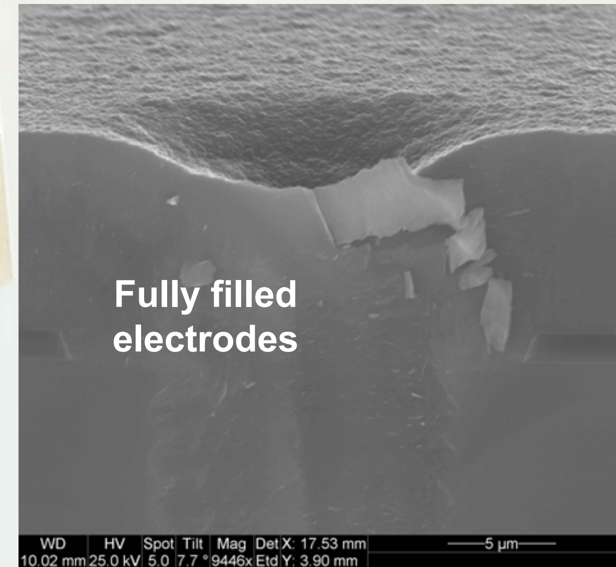


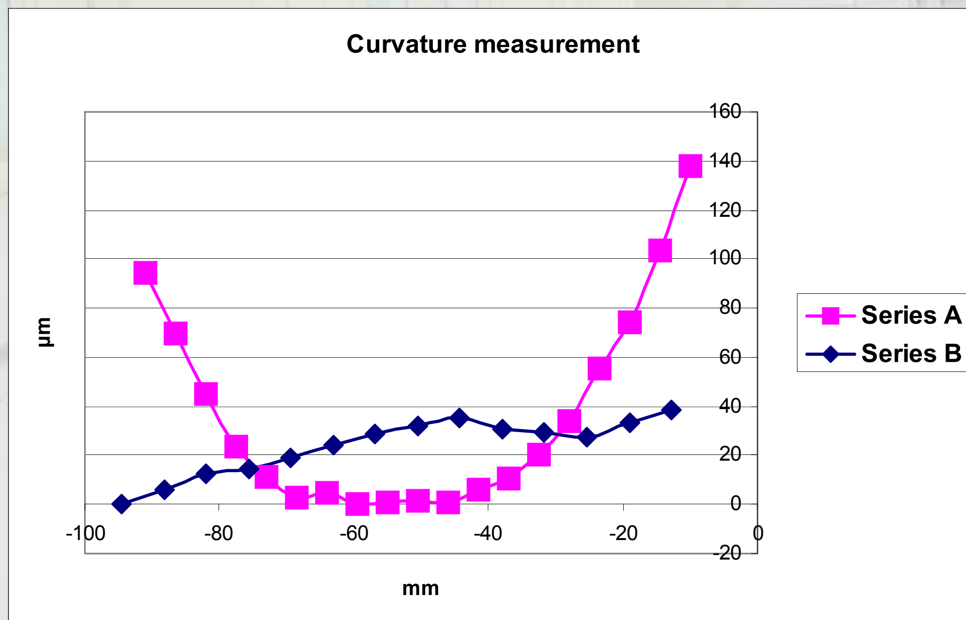




SINTEF 3D: Series B improvements

- P-type wafers
  - Active edge will serve as depletion stop
  - More robust configuration
- Narrower trenches (4 µm)
- Improved hole profiles
- Extra nitride layer
  - A better doping barrier
  - Protects the field oxide
  - Keeps symmetry on both back and front side





Result of improvements

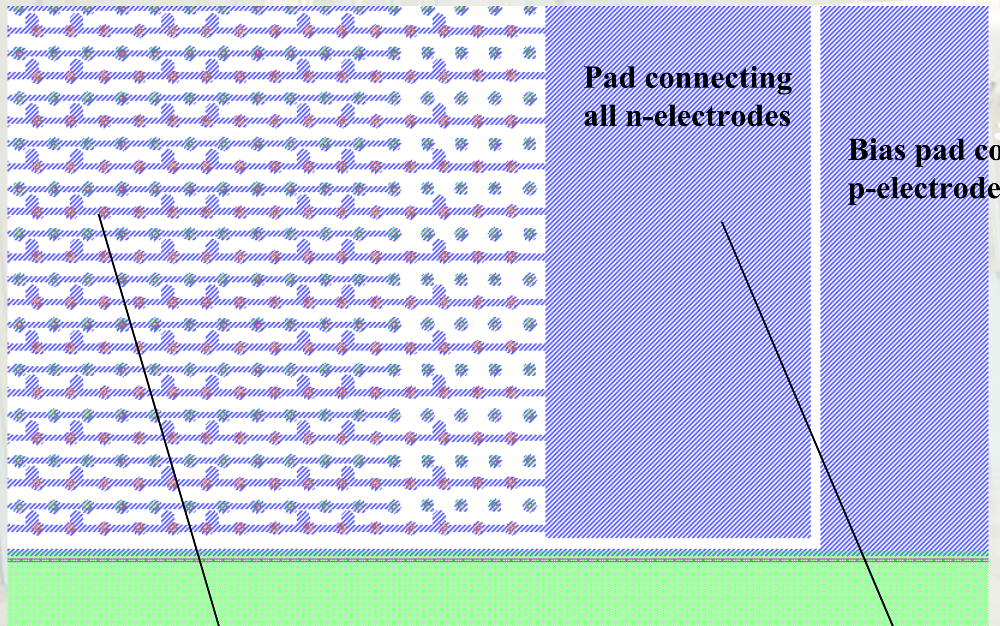
Much reduced stress, bow and breakage

Wafer yield: 18 out of 23

Improved electrode filling reduce topography and allow easier and better lithography

Test metal for electrical measurement

Short circuits all n-electrodes. Later removed and replaced by final metal



Detail of CMS 1ROC chip 2E test metal

Test metal allows measurement of total chip leakage in one measurement. However, the positive potential on the metal pads / lines induces surface inversion ("MOS" effect). This may cause a large and possibly dominating contribution to the total leakage. May also determine breakdown. Thus the measurements are only indicative.

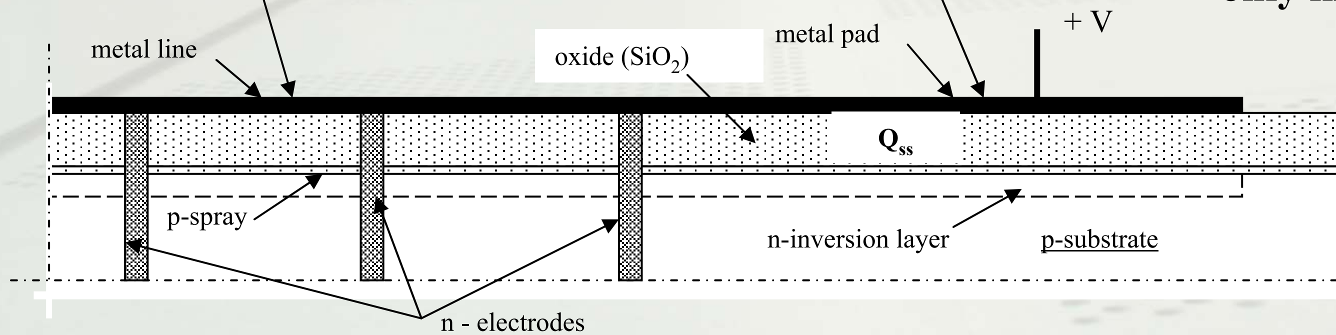
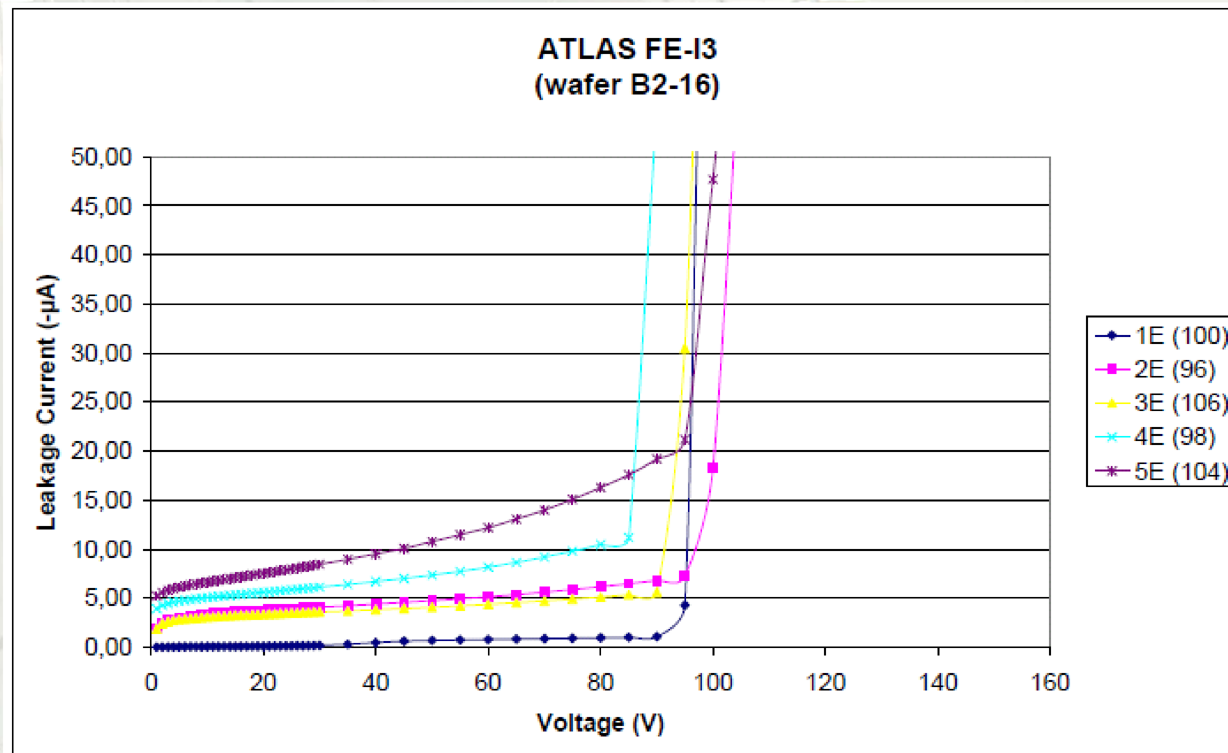


Illustration of MOS effect
Turns on between 5 and 30 V depending on p-spray and oxide charge Q_{ss}.

Measured IV-characteristics ATLAS FE-I3 chips

Summary of measurements of good chips on wafer B2-16 (200 µm thick). Measured with test metallization which short circuits all pixels (n-electrodes).

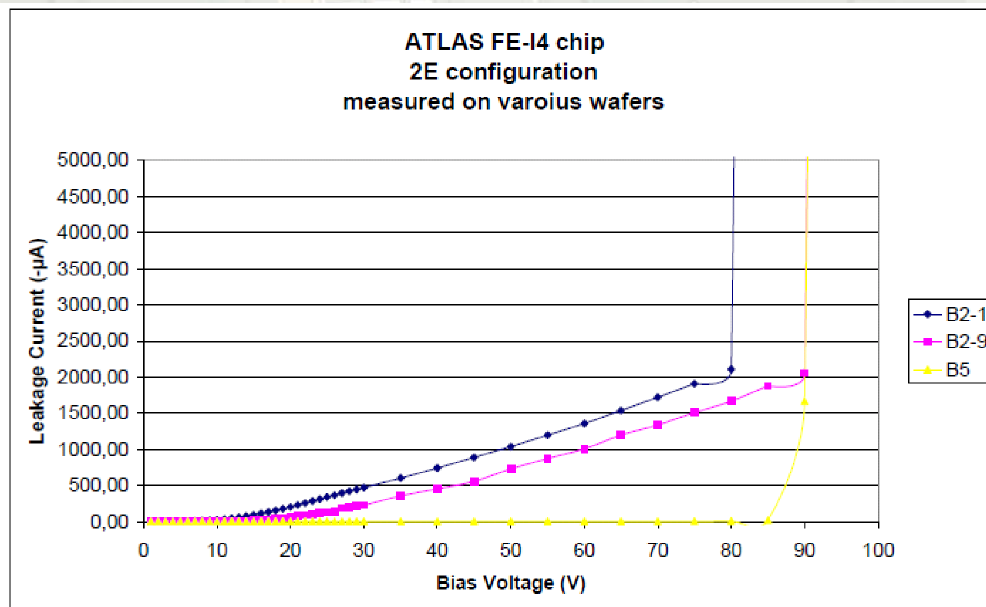


Total leakage from ≈ 2700 pixels as function of bias.
Corresponds to ≈ 2700 (1E) to ≈ 13500 (5E) electrodes.
Leakage Includes “MOS” effect and possible bad electrodes.

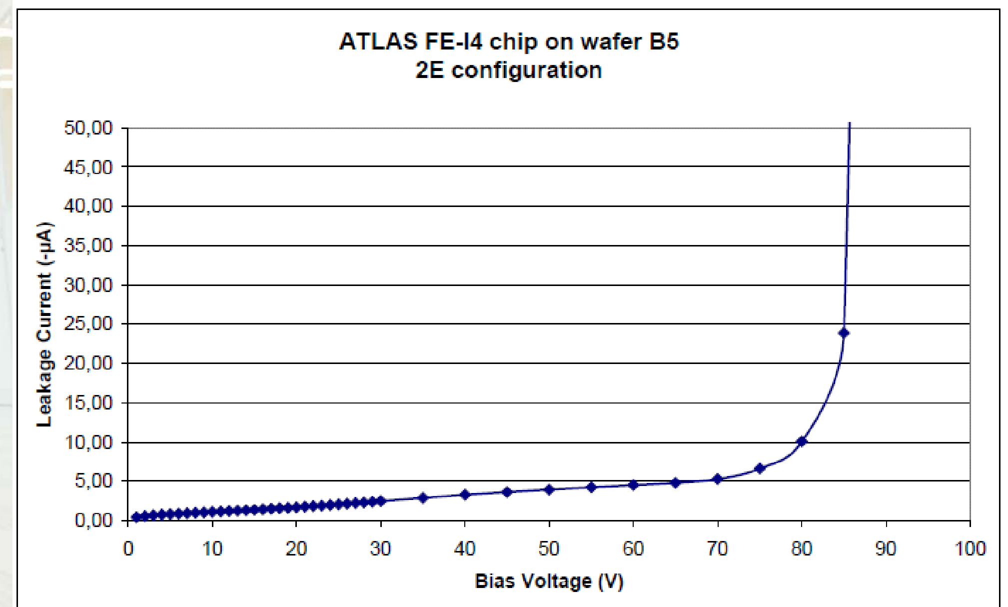
Yield of chips measured on all on wafer typically 40% with BV 80 - 100V.
Real yield higher as full depletion voltage is much lower

Measured IV-characteristics on ATLAS FE-I4 chips

Total leakage from 20376 pixels (40752 electrodes) including MOS effect and possible bad electrodes



I-V measurements on FE-I4 chips from wafers B2-1, B2-9 (200 µm thick) and B5 (280 µm thick)



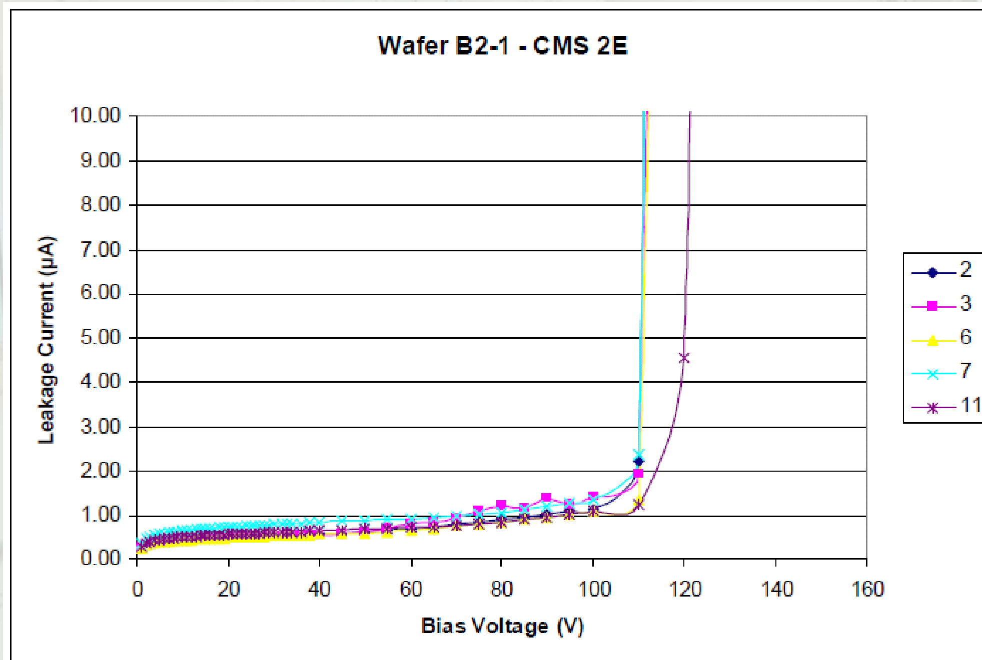
I-V measurements on FE-I4 chip from wafer B5 (285 µm thick). Chip at wafer edge.

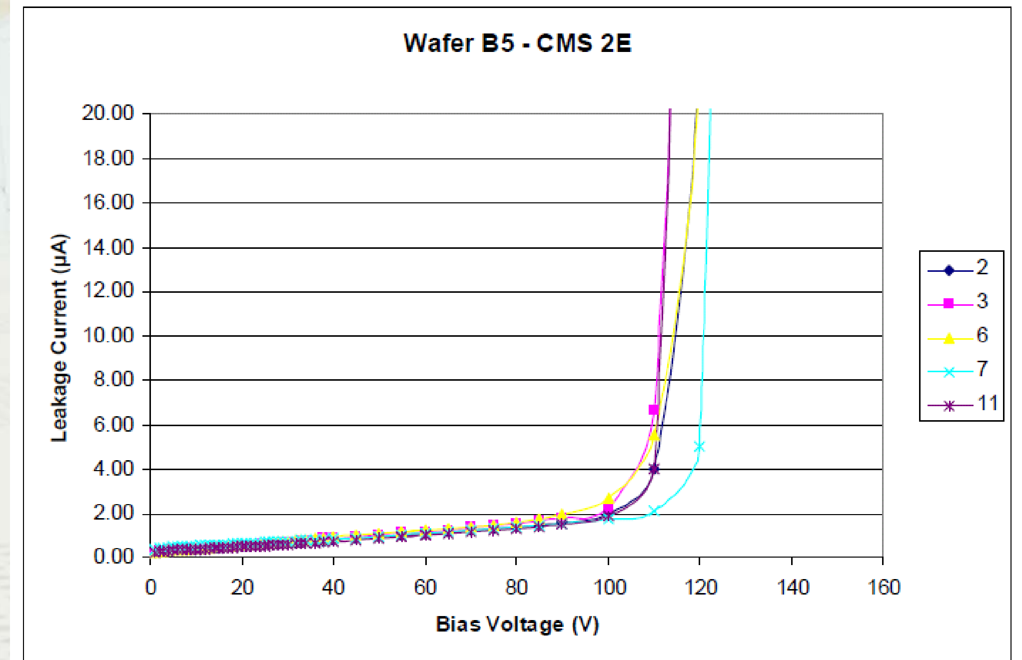
Active edge trench and electrodes not opened in upper left corner due to masking ring. Probably only ≈ 34000 electrodes opened (17000 pixels). < 100 pA / electrode in full depletion including MOS effect.

Measured IV-characteristics CMS 1ROC chips
2E Configuration

5 good chip from wafer B2-1 (200 µm thick) and B5 (280 µm thick)
Measured with test metallization which short circuits all pixels (n-electrodes).
Total leakage includes contribution from “MOS” effect and possible bad pixels

Chip includes ≈ 2000 pixels (≈ 4000 n-electrodes)





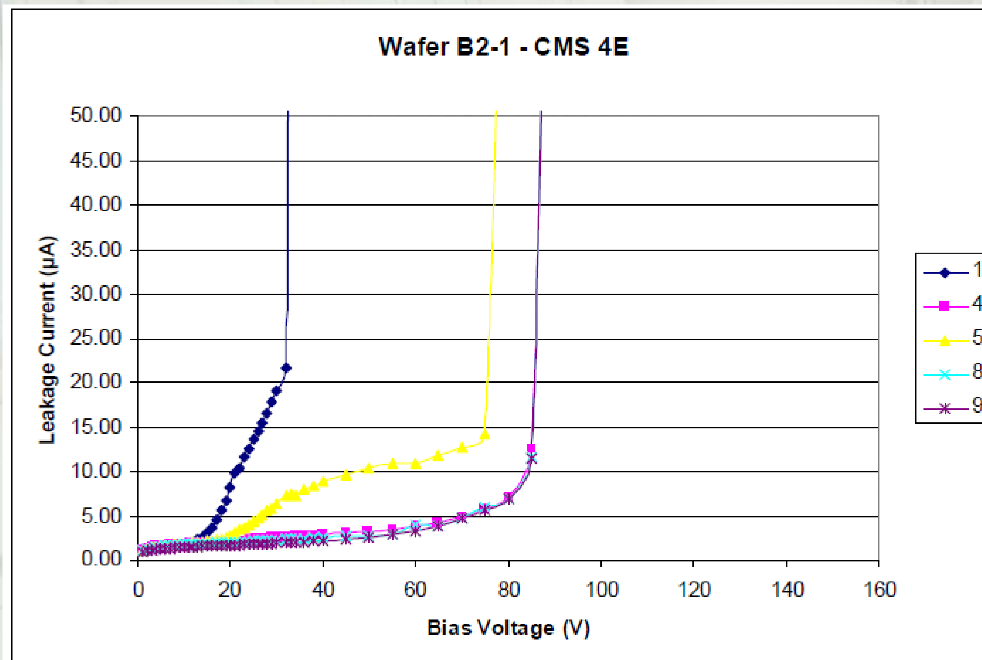
Wafer B2-1
200 µm thick

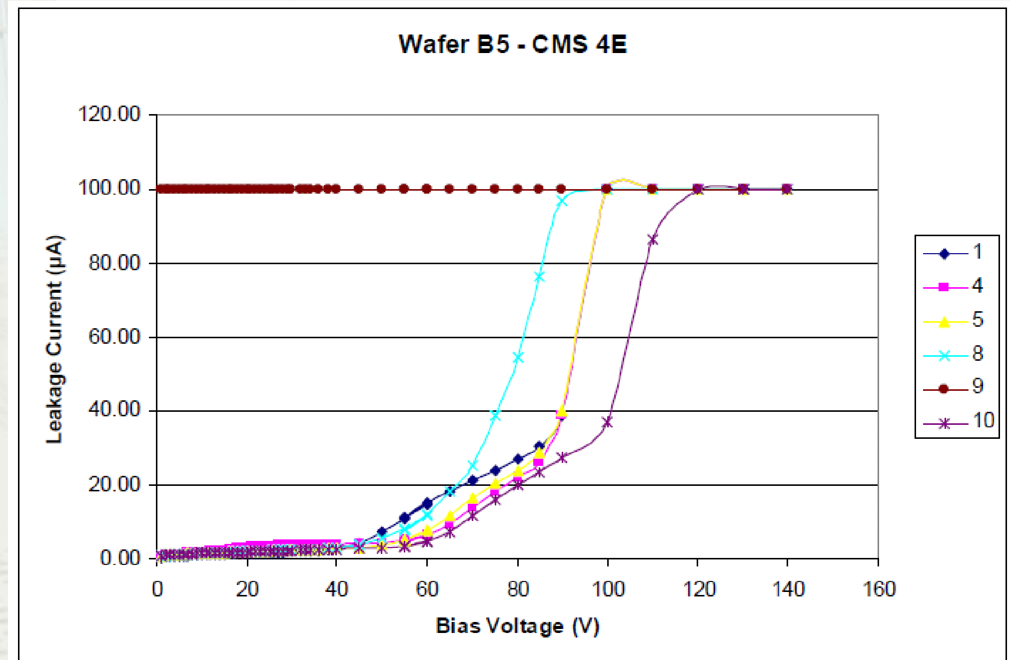
Wafer B5
280 µm thick

Measured IV-characteristics CMS 1ROC chips 4E Configuration

5 chips from wafer B2-1 (200 µm thick) and B5 (280 µm thick)
Measured with test metallization which short circuits all pixels (n-electrodes).
Total leakage includes contribution from “MOS” effect and possible bad pixels

Chip includes ≈ 2000 pixels (≈ 8000 n-electrodes)



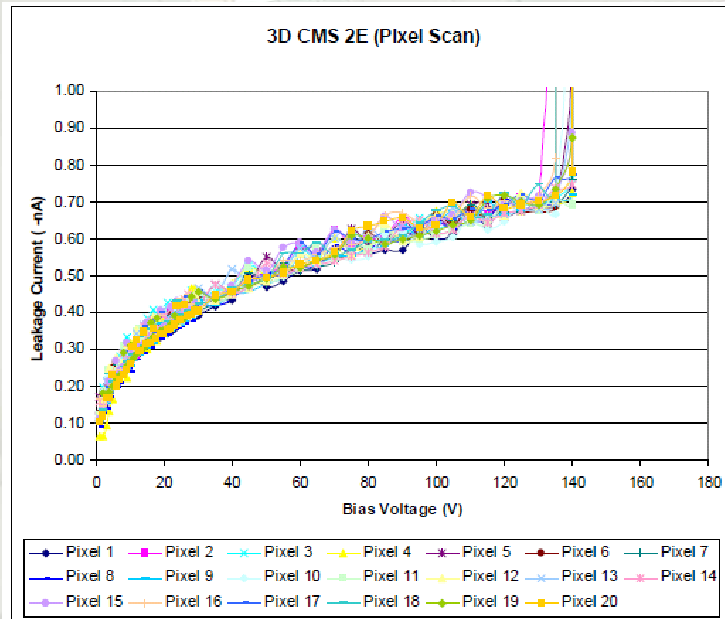


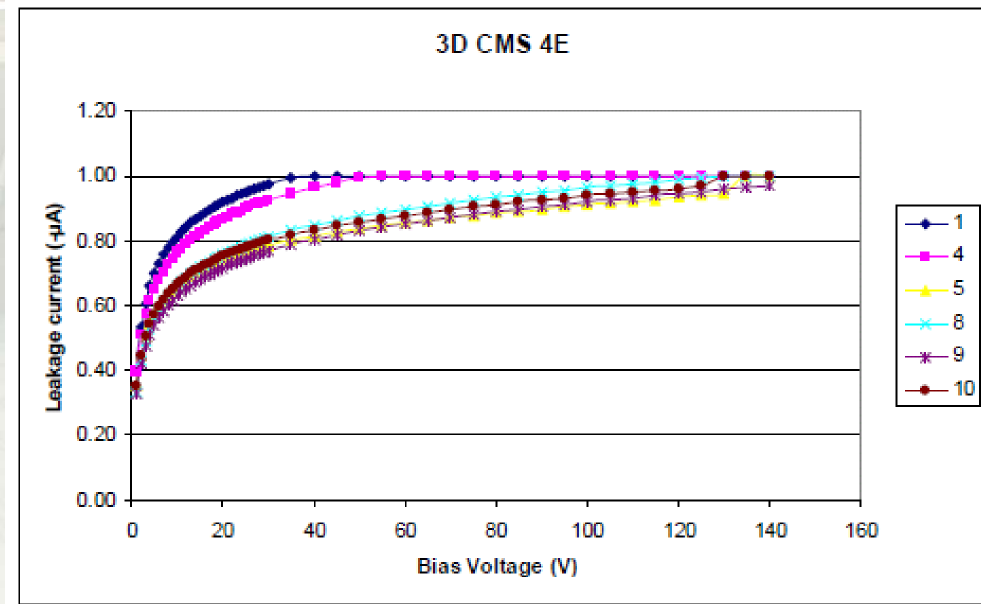
Wafer B2-1
200 µm thick. Full depletion < 5 V

Wafer B5
280 µm thick. Full depletion < 5 V

CMS 1ROC 2E and 4E Configurations

Single pixel IV-measurements on chips with final metal.
Other pixels floating and measurement include pick up from adjacent pixels.
Chip include ≈ 2000 pixels (4000 – 8000 n-electrodes)



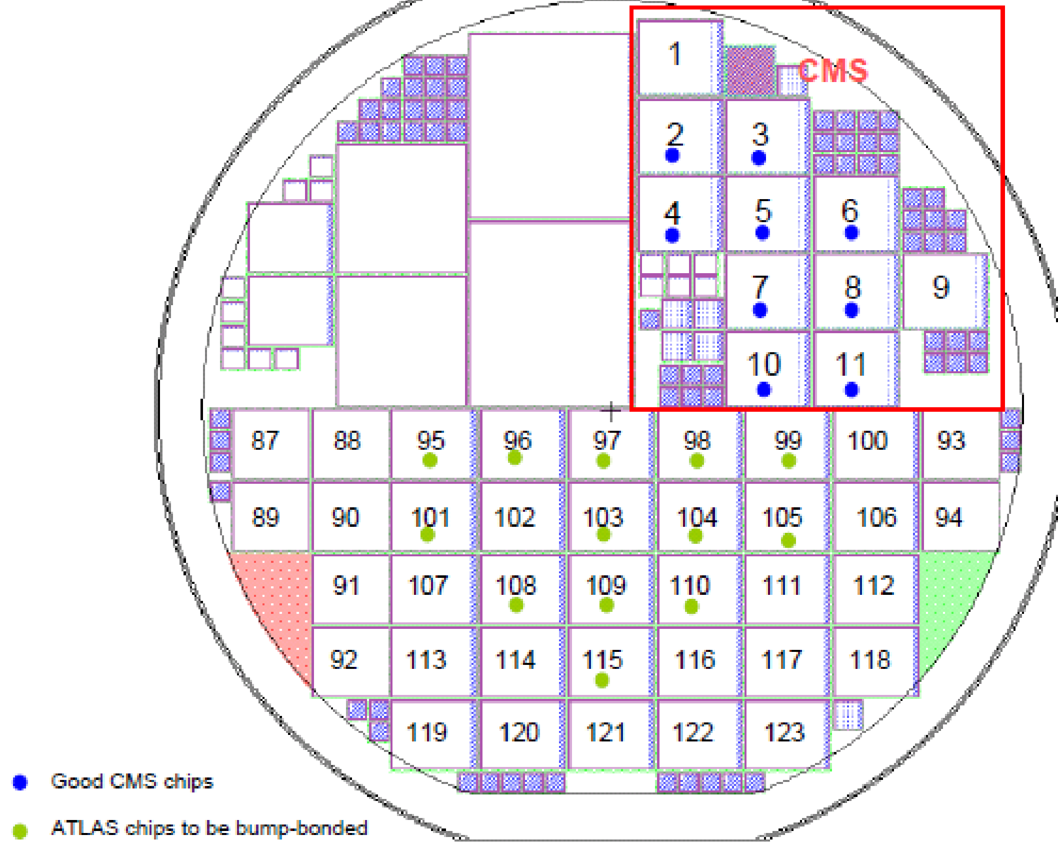


2E configuration

IV-Measurement on 20 pixels from same chip. Very uniform leakage. Includes pick up from adjacent pixels

4E configuration

IV-Measurement on 6 pixels from same chip. Includes pick up from most of chip area



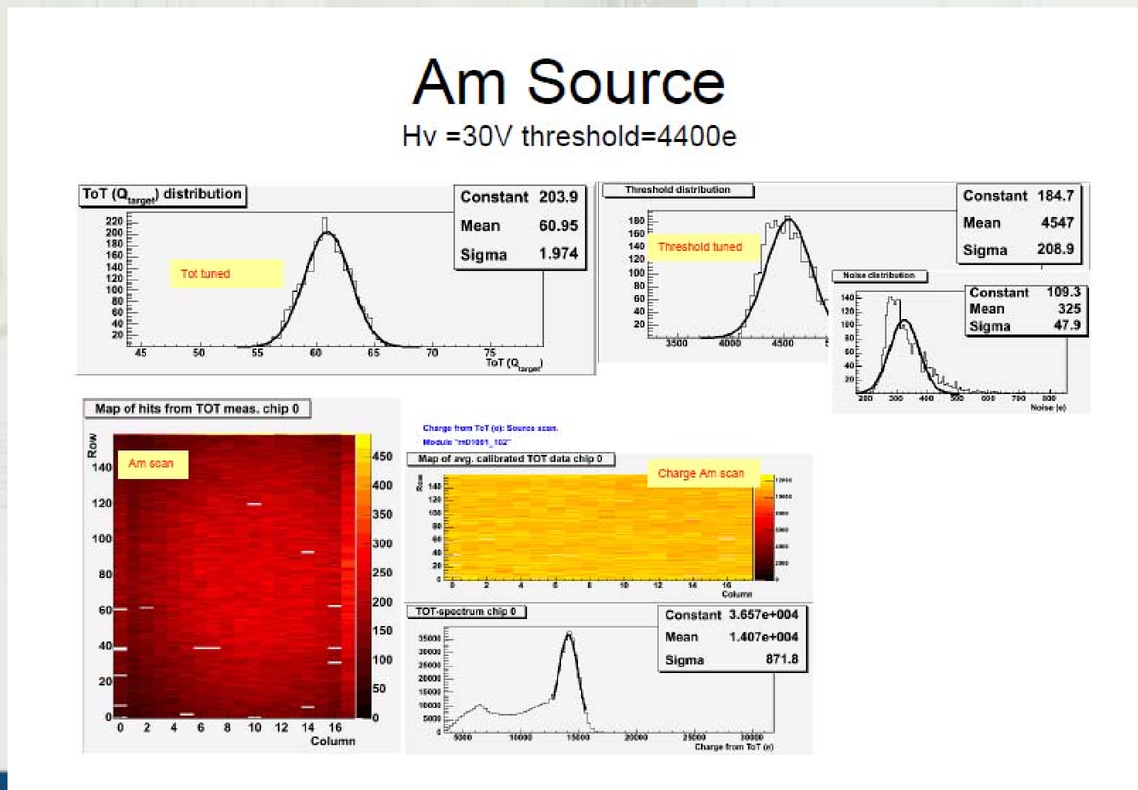
Wafer sent to IZM for Bump-bonding. Illustrates yield of FE-I3 and CMC 1ROC chips at wafer stage

Conclusions and further work

1. Technically 2nd SINTEF 3D-lot did run smoothly. New IPROD DRIE tool gives high quality electrode holes and fast etch times. However, reliability of IPROD tool not convincing with 3 long down periods. Large delays compared to project plan
2. Process changes considerably reduced wafer stress and warping, improved electrode filling and lithography compared to first run. Low breakage and much improved wafer yield, 18 out of 23 wafers survived the process.
3. Typical pixel average leakage current 0.5 to 1 nA in full depletion measured with a test metallization that short circuits all pixels (n-electrodes) and includes possible bad electrodes and a contribution from the “MOS” effect. Confirmed by single pixel measurements on chips with final metallization. Real pixel leakage probably ≤ 100 pA.
4. Medipix chips do not work. Seem to be no pn-junction. Must be investigated further.

Conclusions and further work

5. 4 wafers sent to IZM for bump bonding:
   2 wafers completed. Full FE-I3 assemblies made in Genoa.
   Several bad assemblies, but at least one good.
   Sent to CERN for beam test
6. Assembled unit successfully beam tested at CERN on 21.11.09, showed good Landau distribution



Test by
Alessandro Rovani
Claudia Gemme

Conclusions and further work

7. 2 wafers deposited with UBM only. Have been returned to SINTEF for removal of support wafer and dicing by DRIE

8. Funds needed for common floor plan processing:

Total processing cost	?????? [1)]
SINTEF internal funds	≈ € 75k (TBC)
Additional funding	??????

Note 1: The processing cost will be evaluated within a few weeks