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## 3D silicon detectors for neutron imaging applications

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## 3D silicon detectors for neutron imaging applications

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**ABSTRACT:** Neutron detection is of great importance in many fields spanning from scientific research, to nuclear science, and to medical application. The development of silicon-based neutron detectors with enhanced neutron detection efficiency can offer several advantages such as spatial resolution, enhanced dynamic range and background discrimination. In this work, increased detection efficiency is pursued by fabricating high aspect ratio 3D micro-structures filled with neutron converting materials (B<sub>4</sub>C) on planar silicon detectors. An in-depth feasibility study was carried out in all aspects of the sensor fabrication technology. Passivation of the etched structures was studied in detail, to ensure good electrical performance. The conformal deposition of B<sub>4</sub>C with a newly developed process showed excellent results. Preliminary electrical characterisation

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of the completed devices is promising, and detectors have been mounted on dedicated boards in view of the upcoming tests with neutrons.

**KEYWORDS:** Neutron detectors (cold, thermal, fast neutrons); Solid state detectors; Detector modelling and simulations I (interaction of radiation with matter, interaction of photons with matter, interaction of hadrons with matter, etc.); Detector modelling and simulations II (electric fields, charge transport, multiplication and induction, pulse formation, electron emission, etc.)

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## 1 Introduction

Neutron detection has historically been achieved using  $^3\text{He}$  or  $\text{BF}_3$  gas detectors. The scarcity of  $^3\text{He}$ , and the toxicity of  $\text{BF}_3$ , have driven detector research into finding new solutions for efficient neutron detection. For applications in neutron imaging with thermal neutrons, planar silicon detectors coated with neutron converting materials ( $^{10}\text{B}$  and  $^6\text{Li}$ ) have shown promising results in terms of spatial and time resolution [1]. Neutrons interacting with  $^{10}\text{B}$  and  $^6\text{Li}$  converter layers create two different reactions. The first results in the generation of  $\alpha$ -particles and lithium-ions ( $^{10}\text{B}$ ) and the second in  $\alpha$ -particles and tritium-ions ( $^6\text{Li}$ ). The limitations in neutron detection efficiency of coated planar detectors come from non-optimised converter thickness (self-absorption of the conversion products in the film) and geometrical effects resulting in loss of conversion products [2], ultimately reducing the overall detection efficiency. SINTEF has previously produced silicon neutron detectors with pyramidal micro-structures coated with  $\text{B}_4\text{C}$  in an attempt to increase the detection efficiency of the sensor [3]. This approach offered a 38% relative increase in detection efficiency when compared to standard planar coated detectors.

The recent advances in silicon micro-machining promise to eliminate many of the issues identified in solid-state neutron detectors, by creating high aspect ratio micro-structures to house the converter material. This will increase both the neutron conversion probability and the chances of detecting the conversion products [4]. Many research groups have investigated novel 3D neutron

detectors by means of single and double-sided trenches, pillars, and single-sided matrices of micro-structures in different configurations [5]. Experimental neutron detection efficiency over 40% were reported for some micro-structure configurations [5].

Several aspects are mentioned in the literature as limiting factors of the current solid-state 3D neutron detectors technology: (i) non-optimized micro-structure geometry (diameter/width, depth, and pitch), (ii) inactive layers at the silicon/converter interface, and (iii) difficult conformal deposition of the neutron converters inside the micro-structures.

The sensors described in this paper aim at addressing several of these limitations. The sensors were designed and fabricated at SINTEF MiNaLab, Oslo, Norway. The basic sensor architecture is conceptually similar to the one reported in [6]. A number of modifications were made to the sensor geometry based on SINTEF's expertise on sensor design and 3D detector technology, with the intent of further increasing the overall neutron detection efficiency. In this paper, we report on the sensor design aspects, micro-structure geometry and their fabrication/passivation, neutron converter depositions and preliminary electrical characterisation of the fabricated devices.

## 2 Sensor architecture

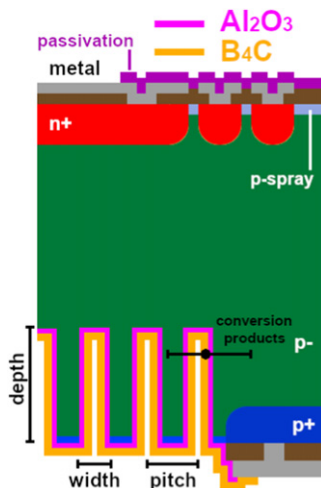
The sensors were fabricated with a standard planar process, on both N-type and P-type FZ silicon wafers of 150 mm diameter and resistivity in the range 5 to 12 k $\Omega$  cm. A thin entrance window was created on the back of the sensors to increase the detection efficiency of the planar regions of the detector. The wafer layout includes diodes, strip detectors and Medipix/Timepix pixel detectors. P-type wafers feature a p-spray implantation for inter-electrode isolation.

After completion of the planar fabrication, high aspect ratio 3D micro-structures were etched on the back of the detectors by means of Deep Reactive Ion Etching (DRIE). The micro-structures were not doped to reduce the extension of the interface dead layers that could negatively affect the detection of the neutron conversion products. Passivation of the etched structures was instead achieved by Atomic Layer Deposition (ALD) of Al<sub>2</sub>O<sub>3</sub> [7] (for P-type wafers), and using native silicon oxide (for N-type wafers). The ALD process was studied in detail at the University of Oslo with Quasi Steady-State Photo Conductance (QSSPC) lifetime measurements and with C-V measurements on MOS capacitors with Al<sub>2</sub>O<sub>3</sub> dielectrics [8, 9].

Given the high aspect ratio of the 3D micro-structures, the deposition of the neutron converter must occur with a highly conformal process. Amongst the most popular neutron converter materials, B<sub>4</sub>C deposited by Chemical Vapour Deposition (CVD) was chosen. Linköping University (Sweden) has recently developed a new CVD process that ensures conformal deposition of B<sub>4</sub>C with good topography coverage, into high aspect ratio 3D structures [10]. The deposition process was successfully characterised on test structures fabricated at SINTEF.

The geometry of the 3D micro-structures was designed with the aid of Geant4 simulations carried out at the University of Bergen using the NCrystal library [11]. Different combinations of structure shape, size, depth, and pitch were investigated to study their effect on neutron conversion probability and detection efficiency.

A cross-section of the fabricated devices is shown in figure 1. The following sections discuss the main challenges encountered during the development of this technology. The preliminary electrical characterisation is also discussed.



**Figure 1.** Cross section of the sensor concept highlighting all the critical aspects.

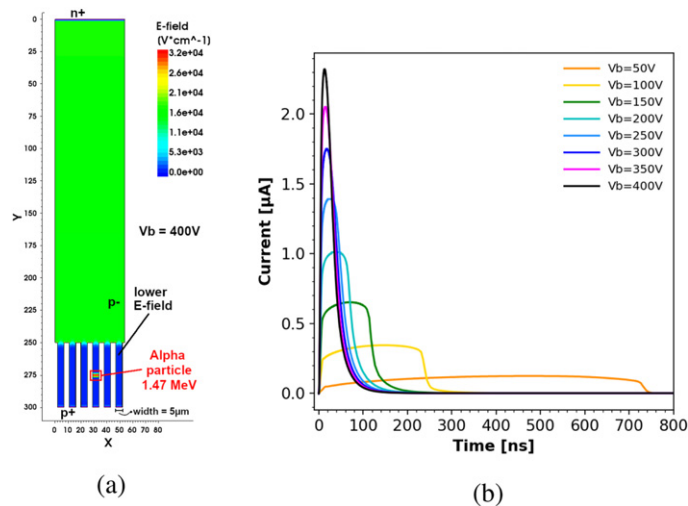
### 3 Numerical simulations

Modern numerical simulation tools offer high accuracy on detector modelling and are important tools for the design and characterisation of new detector technologies. The detectors discussed in this paper were designed and simulated using two different tools. The electrical properties of the sensors and the expected charge collection behaviour were simulated using the Synopsys TCAD tools [12]. The neutron detection efficiency was studied with Geant4 simulations using the NCCrystal library [11].

#### 3.1 TCAD simulations of the full sensor

The detector structure reproduced in Synopsys TCAD is shown in figure 2(a). It is representative of a planar diode with 50  $\mu\text{m}$  deep micro-structures. The passivation of the micro-structures is modelled with a dielectric layer with negative fixed charge and low interface traps, as expected for  $\text{Al}_2\text{O}_3$ . The detectors is biased by grounding the junction electrode of the diode, while ramping the potential of the back side electrode. Figure 2(a) shows the distribution of the electric field at a bias voltage of 400 V. The electric field between the micro-structures is low, indicating that full depletion of the silicon bulk is difficult to achieve. This suggests that charge carriers generated in this region will have to rely on diffusion until they reach a higher electric field region, resulting in relatively slow charge collection. This was demonstrated by studying the transient evolution of the current pulse generated by the release of an alpha particle with energy of 1.47 MeV horizontally between two micro-structures (see figure 2(a)). The simulated charge collection as function of applied bias voltage is shown in figure 2(b). The detector response at low bias is slow, but becomes

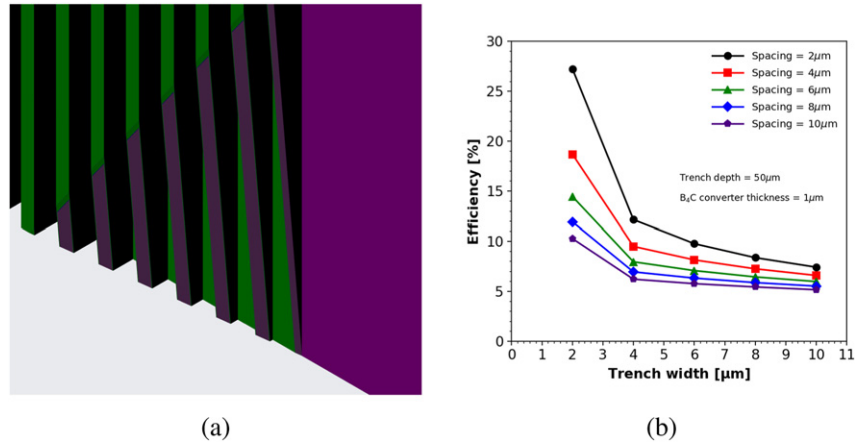
considerably faster at higher biases. The depth of the micro-structures negatively affects the speed of the charge collection, and the correct balance between neutron detection efficiency, etched depth and charge collection efficiency must be investigated by Geant4 simulations and experimentally.



**Figure 2.** TCAD simulations of a diode with 3D micro-structures. Electric field distribution at 400 V (a) and current pulses in response to a 1.47 MeV alpha particle as function of bias voltage (b).

### 3.2 Geant4 simulation of the 3D micro-structures

The geometry and depth of the micro-structures housing the neutron converter can have a large impact on the neutron detection efficiency of the sensor. Several aspects must be considered. Avoiding self-absorption of the conversion products into the neutron converter is crucial and the thickness of the converter layer must therefore be chosen carefully. Width and spacing between the micro-structures are also important, as well as the type of geometry implemented (e.g. trenches, holes, etc.). Several types of micro-structures were simulated in Geant4. The baseline structures are circular holes (3  $\mu\text{m}$  diameter) and trenches (3  $\mu\text{m}$  width). The neutron converter was  $^{10}\text{B}_4\text{C}$  ( $^{10}\text{B}$ -enriched  $\text{B}_4\text{C}$ ). Figure 3(a) shows a structure with equally spaced trenches. The violet regions represent silicon, while the green regions represent the neutron converter. The passivation layer of the micro-structure is also present but it is difficult to visualize due to its reduced thickness. Monte Carlo simulations were performed by changing converter thickness, depth, width and spacing of the etched structures. The simulation was carried out with a beam of  $10^7$  neutrons, and by counting the number of conversion products that could reach the silicon. Events for which both the  $\alpha$ -particle and Li-ion reached the silicon were only counted as one event (to avoid double counting). The results for 50  $\mu\text{m}$  deep trenches with a 1  $\mu\text{m}$  layer of  $^{10}\text{B}_4\text{C}$  are shown in figure 3(b). For wide structures with large spacing, the simulated neutron detection efficiency is only around 5%. The most promising results are obtained with 2  $\mu\text{m}$  trenches separated by 2  $\mu\text{m}$  of silicon, reaching roughly 28% efficiency. Further increasing the depth of the trenches to 100  $\mu\text{m}$  suggests that the conversion efficiency of the sensor can further improve, but, as discussed in subsection 3.1, this can result in a degradation of the charge collection properties of the sensor.



**Figure 3.** Geant4 simulations of 3D micro-structures in a long trench configuration (a) and the resulting simulated efficiency (b).

## 4 Fabrication challenges and preliminary characterisation

The planar part of the sensor fabrication process was achieved using standard silicon fabrication technology. The key challenges are all related to the fabrication of the 3D micro-structures. Due to the small feature size and high density, the photolithographic process is demanding. Ensuring a successful lithography is crucial to achieve good control on micro-structure fabrication.

### 4.1 Fabrication of 3D micro-structures

Etching of silicon using DRIE requires a highly selective masking layer. Several options are available: (i) aluminium delivers high selectivity but the diameter/width of the mask opening is difficult to control; (ii) photoresist delivers good accuracy of the geometries created, but suffers from poor selectivity and difficulty in controlling the vertical profile of the etched structures; (iii) PECVD SiO<sub>2</sub> offers good geometry definition and etch selectivity sufficient to have good control of the etch profile. In this fabrication run, PECVD SiO<sub>2</sub> was used as DRIE masking layer.

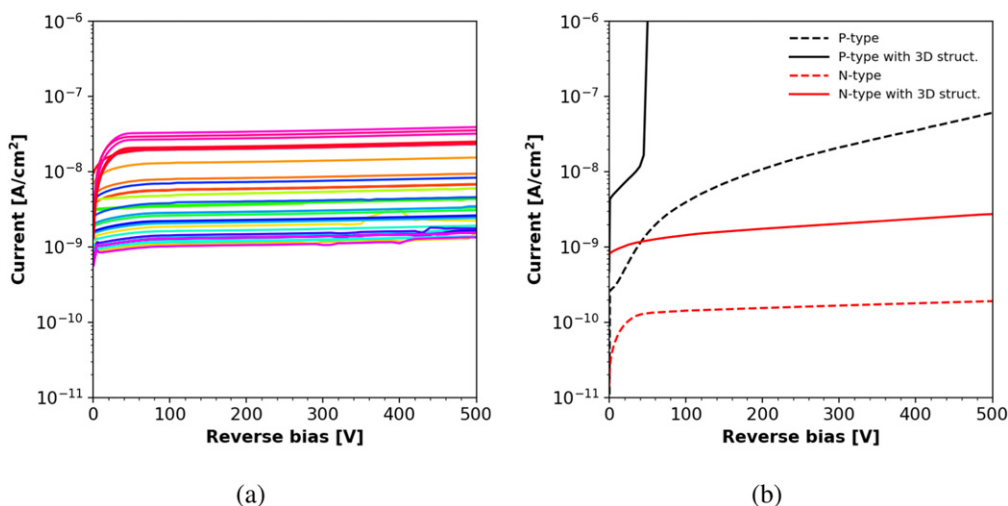
After deposition of 2  $\mu\text{m}$  of PECVD SiO<sub>2</sub>, the lithographic process was carried out using a standard mask aligner. Due to the small feature size and pitch between the structures, light diffraction caused the unwanted exposure of the resist between the micro-structures. This issue was not present on all wafers, and the majority of the structures could be created correctly. More advanced lithographic machines, such as mask-less aligners, or stepper lithography, will in the future allow for better control of this step.

After the photolithography, the PECVD SiO<sub>2</sub> was etched to expose the silicon underneath, the photoresist was removed, and the micro-structures were etched into the silicon. Process splits were performed on the etch depth, in order to validate the results obtained from Geant4 simulations. The chosen etch depths were 20, 40, 60 and 80  $\mu\text{m}$ , with the highest aspect ratio equal to roughly 27:1 (depth to width).



## 4.2 Preliminary electrical characterization

A preliminary electrical characterisation of the fabricated detectors was carried out at critical steps throughout the process. The I-V of a subset of diodes was measured at the end of the planar part of the process on several wafers. The results were satisfactory, with currents ranging between a few hundred pA/cm<sup>2</sup> and a few nA/cm<sup>2</sup> (figure 4(a)). After etching of the micro-structures, the I-V of some diodes was re-measured to evaluate the damage caused by the etching before applying the passivation. Figure 4(b) shows the comparison of the I-V curves before and after etching, for a P-type and a N-type diode. Both devices show an increase in the current by a factor 10, caused by plasma and silicon etch damage, but the P-type device shows a rapid increase in current at around 50 V. This corresponds to the voltage at which the depletion region reaches the micro-structures, confirming the need of passivation of the micro-structures using Al<sub>2</sub>O<sub>3</sub> for detectors fabricated on P-type material. The N-type detectors seem to operate in a satisfactory manner even without a dedicated micro-structure passivation. This stems from the fact the native SiO<sub>2</sub> layer contains sufficient positive charge for the mitigation of the silicon damage cause by DRIE.



**Figure 4.** Preliminary I-V measurements of a selection of fabricated detectors before etching of the micro-structures (a), and comparison of the currents of two devices before/after etching (b).

## 5 Passivation of silicon with atomic layer deposition of Al<sub>2</sub>O<sub>3</sub>

The passivation of P-type silicon by means of ALD Al<sub>2</sub>O<sub>3</sub> was studied in detail over several years [8, 9]. The Al<sub>2</sub>O<sub>3</sub> layer contains fixed negative charge which attracts holes at the interface with silicon, thus creating an accumulation layer. Two key quantities are important to achieve good silicon passivation: (i) high concentration of negative fixed charge, and (ii) low concentration of interface defects. These quantities were extracted from C-V measurements of MOS capacitors for the different process variations tested. Table 1 offers a summary of the most promising results for a Al<sub>2</sub>O<sub>3</sub> thickness of 20 nm. Two process splits were shown to have the most impact on the quality

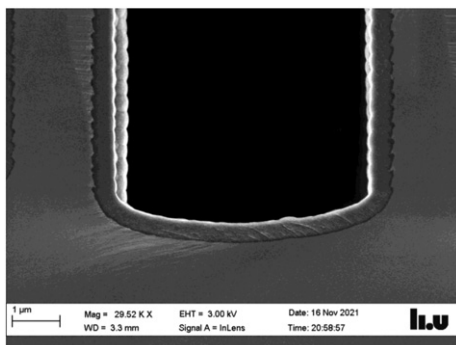
of the passivation. A pre-treatment removing the native  $\text{SiO}_2$  by means of 3 min HF dip, and the post-deposition anneal performed in forming gas (FG) at  $435^\circ\text{C}$ . The post-deposition anneal allows to reduce the interface defects while leaving the amount of fixed charge almost unchanged, while the removal of the native oxide layer at the silicon interface, causes a slight increase in interface defect concentration. This indicates that leaving the native oxide in place is beneficial.

**Table 1.** Fixed charge and interface defects for ALD  $\text{Al}_2\text{O}_3$  deposited with different processes, extracted from C-V measurements on MOS capacitors.

Pre-treatment	Annealing	$Q_{\text{fix}}$ [ $\text{cm}^{-2}$ ]	$D_{\text{it}}$ [ $\text{eV}^{-1} \text{cm}^{-2}$ ]
3 min HF dip	—	$-4.0 \times 10^{12}$	$2.7 \times 10^{12}$
—	—	$-4.7 \times 10^{12}$	$2.0 \times 10^{12}$
3 min HF dip	10 min FG $435^\circ\text{C}$	$-3.6 \times 10^{12}$	$2.7 \times 10^{10}$
—	10 min FG $435^\circ\text{C}$	$-3.3 \times 10^{12}$	$1.0 \times 10^{10}$

## 6 Neutron converter deposition

The CVD process for deposition of  $^{nat}\text{B}_4\text{C}$  was characterised at Linköping University with excellent results in terms of conformality and thickness control. The current precursor only allows for the deposition of  $^{nat}\text{B}_4\text{C}$ , but the process for  $^{10}\text{B}$ -enriched  $\text{B}_4\text{C}$  is under development. A SEM picture of the bottom of a  $6\ \mu\text{m}$  wide and  $60\ \mu\text{m}$  deep trench is shown in figure 5. A film of  $^{nat}\text{B}_4\text{C}$  of  $420\ \text{nm}$  thickness was deposited into the structure, at a temperature of  $450^\circ\text{C}$ . This process was tested on structures with aspect ratios up to 27:1, and was implemented on the fabricated detectors.



**Figure 5.** Scanning electron microscope image of the bottom of a 3D trench microstructure (aspect ratio 10:1) after CVD deposition of  $\sim 400\ \text{nm}$  of  $\text{B}_4\text{C}$ .

## 7 Future work

The development and characterisation work performed, led to a good understanding of the technology. Diodes with different micro-structure geometries and two different thicknesses of neutron converter (0.5 and 1.2  $\mu\text{m}$ ) will be tested with neutrons at PSI, at the end of October 2022. Electrical characterisation will continue at SINTEF to gain more insight into the effect of the passivation of 3D micro-structures by means of ALD  $\text{Al}_2\text{O}_3$ . The development of conformal coatings of  $^{10}\text{B}$ -enriched  $\text{B}_4\text{C}$  is on-going, aiming at higher conversion efficiency. Strip detectors are available for testing and will undergo converter deposition in the near future. Pixel detectors will require bump-bonding, flip-chip, and further development for the deposition of the neutron converter on bump-bonded assemblies. The use of the timing capabilities and energy resolution of the TimePix readout chips family could further improve the accuracy in the calculation of the neutron conversion efficiency.

## 8 Conclusions

The production of advanced 3D silicon neutron detectors required the in-depth study of several aspects of the technology. The sensor fabrication process is sufficiently mature. Crucial aspects of the technology like passivation of the micro-structures and conformal deposition of the neutron converter were studied in detail with excellent results. Modelling of the detector with advanced simulation tools helped design and develop the technology further. Testing of the fabricated devices is under way and the first results with neutrons will be available by the end of 2022.

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