SUPPORTING INFORMATION

Charge Transport in 2D MoS_2, WS_2 and MoS_2-WS_2 Heterojunction-Based Field Effect Transistors: Role of Ambipolarity

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A. Electrical connections

For a typical n-type MS channel with electrons as majority carriers and p-gate, the connections are shown in the Figure S1a and Figure S1b, respectively. The majority charge carriers which are injected from the source are collected at the drain. The WS channel device with both n and p-type charge carriers and a p-gate has the source-drain connections as shown in Figure S1c and Figure S1d for the typical n-channel and p-channel conditions, respectively. Similar connections can be seen for the HS device having both n and p-type charge carriers and a p-gate for n-channel and p-channel in Figure S1e and Figure S1f, respectively. The bottom gate to semiconductor (2D material) junction with an intermediate dielectric (SiO_2) layer defines the generated electric field and changes in drain current produced due to the field effect. For the bias applied to MS device in Figure S1a, positive charge carriers build up at the SiO_2 – Si interface with increasing gate bias, attracting oppositely charged negative carriers in MoS_2 channel thereby forming a parallel plate capacitor with electric field directed from positive to negative electrode. With increasing positive gate bias, an increasing electric field develops causing an increase in carriers injected from the source and collected at the drain terminal. This condition is similar in WS and HS devices for Figure S1c and Figure S1e. As the polarity of the bias is reversed for MS (Figure S1b), the electric field direction is reversed causing a depletion of electrons, hence a decreasing current. An increasing current for WS and HS device for increasing negative V_G indicates a possible development of hole channel and carrier conduction between source and drain due to the minority charge carriers.

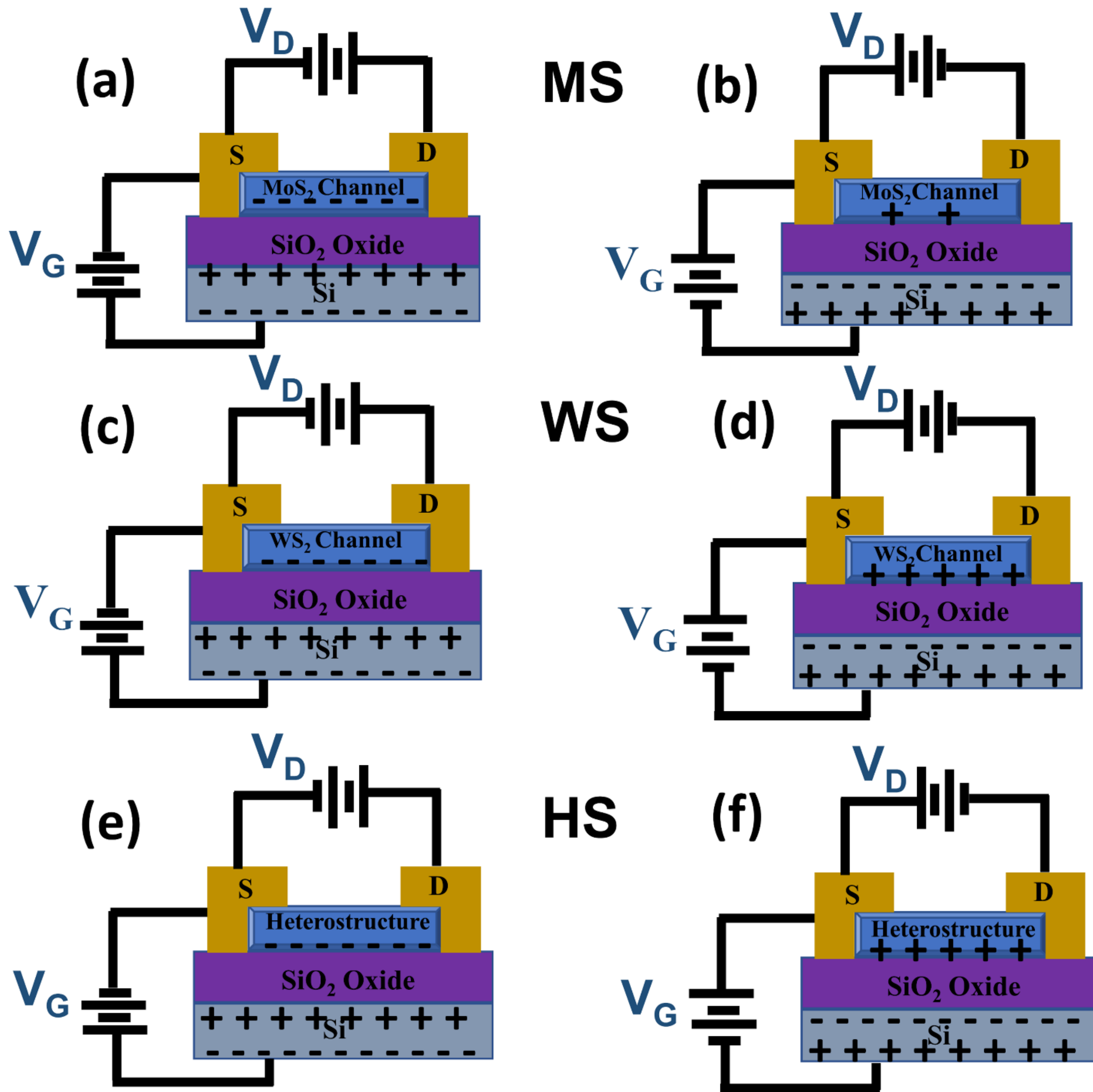

Figure S1. Circuit diagram showing the electrical connections between source – drain and gate – source with corresponding charge distribution for MS in (a) & (b), WS in (c) & (d) and HS devices in (e) & (f) for n-channel and p-channel operation under different gate biases.

B. Drain and Gate voltage range optimization

In our study we carried out initial tests on samples from the same batch as MS, WS and HS to find the optimum range of drain voltages for our devices. A typical example of MoS_2 FET has been shown in the figure below. The saturation is observed to occur at V_D ~ 2V.

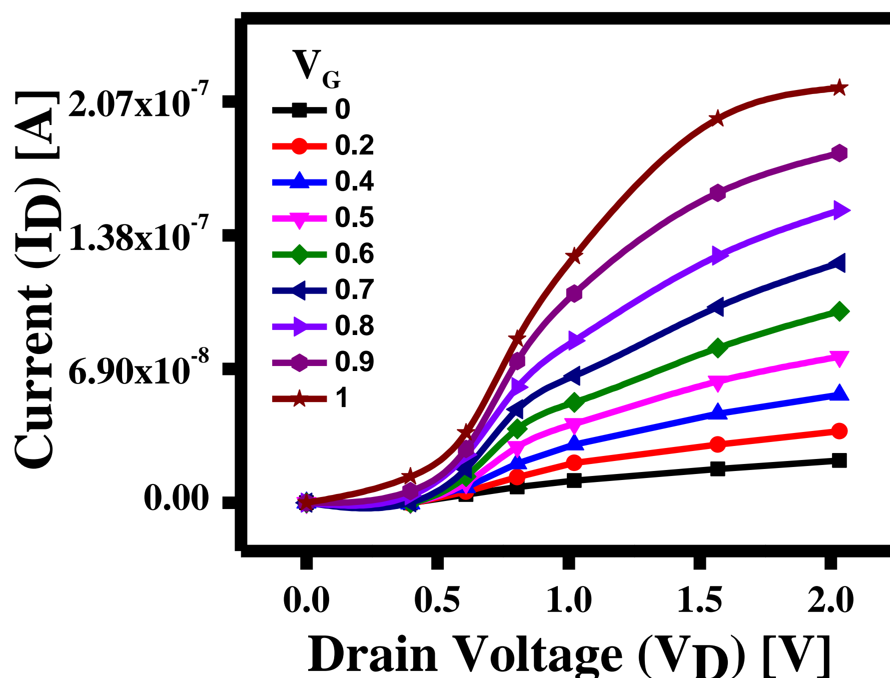

Figure S2. Plot of I_D vs. V_D showing saturation of drain current.

In view of the above initial tests, the drain bias in the present work for the three devices, namely, MS, WS and HS was varied from -1 to +1 V. Also, the gate voltage range was determined by taking a typical example of an MoS_2 FET as shown in the attached graph for reference. We found that with increased gate voltages device rupturing starts to occur at ~ 15 V due to which the devices were tested with gate voltages within the stipulated range, i.e., < 15 V, since the aim of this work was to understand the charge transport properties of the channel materials.

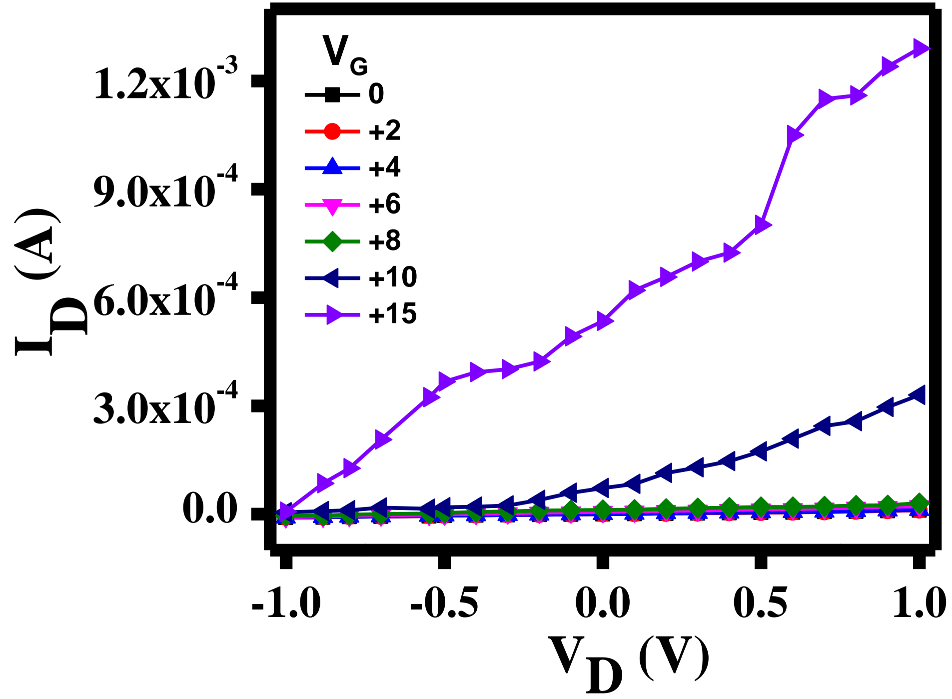

Figure S3. Plot of I_D vs. V_D at various values of V_G showing a device rupturing.

C. Mobility calculation

In the linear region of transfer characteristics, the field effect mobility is given as,

$$\mu = \frac{L}{W * C_{(j)}} * \frac{d(g_m)}{d(V_G)} \tag{1}$$

wherein I_D can be expressed as,

$$I_D = \frac{W}{L} \mu C_j V_D (V_G - V_{th}) \tag{2}$$

which results in

$$I_{D,\max} = g_{m,\max} (V_{G,\max} - V_{th}) \tag{3}$$

Here the contribution of contact resistance is assumed to be zero. In order to understand the role of contact resistance (R_C), V_D taken as V_D-I_DR_C is replaced in the above equation and solved for I_D, the resulting expression for I_D is:

$$I_D = \frac{\frac{W}{L}\mu_0 C_j V_D (V_G - V_{th,0})}{1 + \frac{W}{L}\mu_0 C_j R_C (V_G - V_{th,0})} \quad (4)$$

where μ_0 and $V_{th,0}$ represent the values of mobility and threshold voltage corrected by exclusion of the effect of contact resistance, R_C. The transconductance $g_m = dI_D/dV_G$ is expressed as,

$$g_m = \frac{\frac{W}{L}\mu_0 C_j V_D}{\left[1 + \frac{W}{L}\mu_0 C_j R_C (V_G - V_{th,0})\right]^2} \quad (5)$$

Hence from the above equation (6), the ratio, $I_D/\sqrt{g_m} = \sqrt{W/L\mu_0 C_j V_D}(V_G - V_{th,0})$ is independent of R_C. Thus, the slope of the linear region of I_D / $g_m^{1/2}$ vs. V_G gives the value of corrected field effect mobility and the intercept with x-axis gives the value of the threshold voltage.

The following figures illustrate the variation of I_D, g_m and I_D / $g_m^{1/2}$ with the gate voltage, V_G for a typical case of MS device.

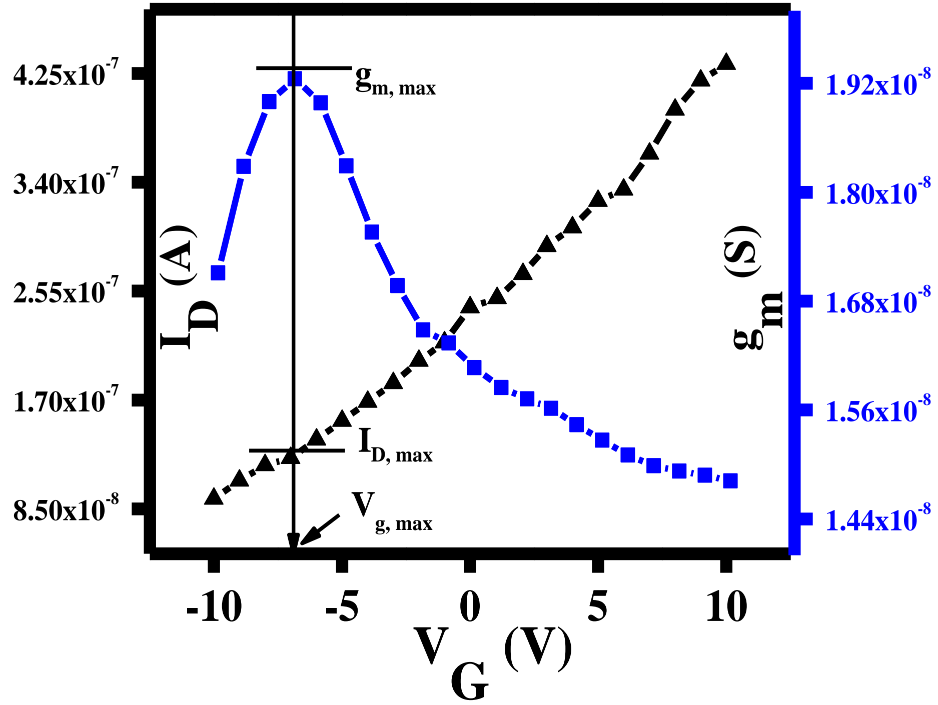

Figure S4. Linear scale plot of I_D (left axis) vs. V_G and transconductance g_m (right axis) vs. V_G.

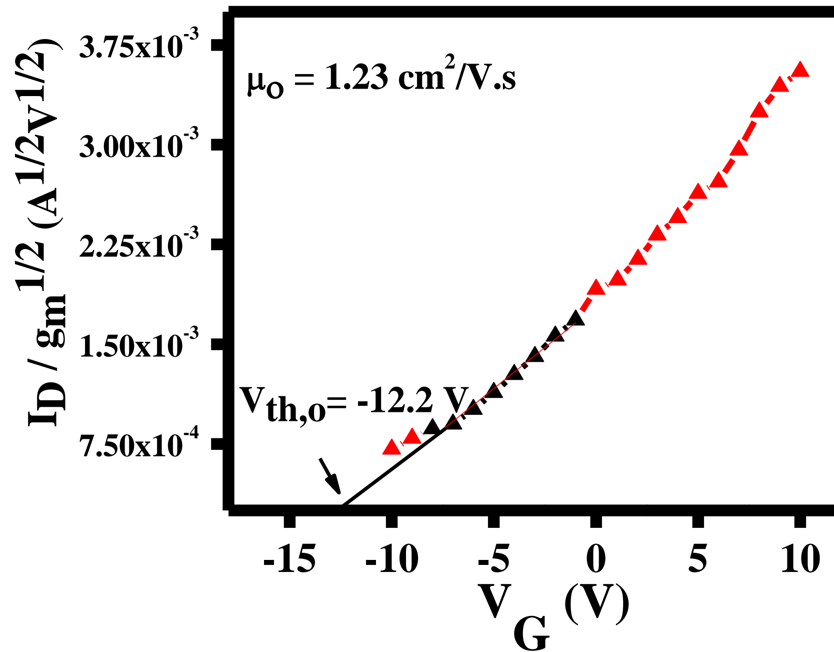

Figure S5. Plot of $I_D/g_m^{1/2}$ vs. V_G with extraction of corrected mobility (μ_0) and threshold voltage ($V_{th,0}$).