Charge Transport in 2D MoS_2, WS_2 and MoS_2-WS_2 Heterojunction Based Field Effect Transistors; Role of Ambipolarity

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ABSTRACT: Electrical and optical characteristics of few layered (3-4 L) CVD grown MoS_2, WS_2 and $MoS_2 – WS_2$ heterostructure based back gated field effect transistor (FET) devices have herein been studied. The structure, stoichiometry and work function of the two-dimensional (2D) materials which comprise the channel region have been comprehensively characterized. The MoS_2 device exhibits a unipolar n-type behavior with a high field-effect ON/OFF ratio ($> 10^3$) and a low subthreshold swing of 668 mV/decade at room temperature. The WS_2 and $MoS_2 – WS_2$ heterostructure devices exhibit gate driven ambipolarity due to chemically active defect sites, offering precise control on carrier type necessary for realization of logic devices. Record high room temperature electron mobility (19 $cm^2/V.s$) exhibited by MoS_2-WS_2 heterostructure device displays an improved electrical performance of almost one order of magnitude higher than already existing 2D devices. Prototype of a 2D complementary metal oxide semiconductor (CMOS) logic inverter switch integrating high electronic and optical response of the $MoS_2 – WS_2$ heterostructure junction owing to ambipolar FET operation has been demonstrated. The achieved results encompassing superior photo absorption, atomically thin thickness and high performance indices suggest that soft 2D heterostructure devices may open a new paradigm in artificial retinal implants and photoelectronics.

1. INTRODUCTION

Transition metal dichalcogenide (TMDC) nanomaterials, such as, MoS_2 and WS_2 have attracted significant attention due to the diversity of applications offered owing to their unique electronic, mechanical, thermal and optoelectronic properties.[1] They are a class of 2D materials with a sizable band gap and layered characteristics, proving to be key materials in efficient switching devices like FETs.[2-4] The present-day silicon technology uses the CMOS logic architecture utilizing the conventional digital logic for which 2D transistors may serve as a boon in terms of both material and device structure. Similar to MoS_2, which is the most well known TMDC comprising of S−Mo−S (S-W-S; in case of WS_2) triple layers, already been explored for its wide band photoresponse,[5-7] WS_2 too is garnering attention in optoelectronic devices due to its high stability, interesting electrical behavior, favorable band gap and higher carrier mobilities. TMDCs can be stacked laterally or vertically to form heterostructured devices with desired and improved functionalities. The crystal structure of 2H-MoS_2 and 2H-WS_2 favors low lattice mismatch (~1.3%) for forming epitaxial heterostructures and results in interesting excitonic attributes having immense utility in optoelectronic applications.[8-10]

In contrast to the extensive studies carried out on pristine 2D materials, heterostructures which combine the properties of individual materials in a single system are yet to be explored comprehensively. Also, the central question of the difference in electronic and optical properties of TMDC heterostructures from the individual materials, dependent on their heterojunction interfaces has been addressed in the present work. Nonetheless, these heterojunctions have demonstrated special carrier transfer behaviors with novel properties due to the interlayer quantum coupling effect.[11] The present study, hence, addresses one of the critical issues in the field of 2D based heterostructures by understanding the charge dynamics at the interface region separating the

individual 2D materials. These systems exhibit novel properties and new phenomena that could trigger a revolution in the architecture design of heterostructures for integrated optoelectronic applications.[12-14]

Heterostructures of 2D TMDC's have previously been designed and evaluated for applications in solar cells, photodetectors, and field effect transistors.[15-18] Owing to the advantages offered, such as, variable band gaps, high ON/OFF switching ratios and a superior immunity to short channel effects compared to bulk materials, low dimensional materials and their heterostructures are much more adaptive in the design of practical FET devices.[19-21] Tunneling FET devices designed by Britnell et al. utilize the single atomic layer property of graphene with vertical transport possible through thin boron nitride and molybdenum disulfide.[22] The characteristic high mobility of graphene and high ON/OFF ratios (~10^5) of MoS_2 are integrated to form novel transistors, as studied by Tian et al..[23] Chen et al. combined chemical vapor deposition (CVD) and thermal evaporation to grow single crystal WS_2 and fabricated FET arrays with mobilities ranging from 0.2 – 4 $cm^2/V.s$.[24] 2D MoS_2, WS_2 and MoS_2 – WS_2 heterostructures have previously been analyzed for their gate-tunable output characteristics, with applications in optoelectronics.[25-26] Interlayer coupling for 2D MoS_2, WS_2 and ambipolarity is previously reported for pristine WS_2 and WS_2 – graphene heterostructures. However, one of the biggest challenge lurking in the effective implementation of 2D semiconducting materials in complementary semiconductor logic circuits is controlling and realizing the desired carrier type. Literature lacks report on precise tuning between unipolarity and ambipolarity during synthesis procedure, with the aid of ionic impurities, addressed in the present study.[26-29]

The behavior of 2D material based heterojunctions when subjected to external strain or under light irradiation can be significantly altered, hence, combining the understanding developed

previously, the present study focusses on the role played by an external electric field on the properties of few layered (3-4 layers) 2D FET devices.[6, 30] The present study reports on the performance of MoS_2, WS_2 and MoS_2 – WS_2 heterostructure devices in back-gated FET configuration, with improved performance indices for optoelectronic applications. The fabricated FET's exhibit novel rectifying and unipolar behavior with ON/OFF switching ratio as high as 10^3 for MoS_2 device and interesting ambipolar transport, enabling both electrons and holes to conduct for WS_2 and heterostructure devices with high mobilities. The electrical behavior has been explained on the basis of band alignment. The designed heterostructure exhibits an unusual optoelectronic property having potential in high efficiency, self-driven CMOS devices.

In a vision to replace the existing state-of-the-art silicon based retinal implants which are rigid, fragile and unable to replicate the natural curvature of the eye, 2D materials are emerging as a thinner, more flexible, curved and high efficiency substitute for artificial biocompatible technologies. The hybrid FET phototransistor switch fabricated in the present study amalgamates the essential electrical and optical characteristics to serve as a prototype for a flexible CMOS inverter device, utilizing the ambipolar behavior of the heterostructure and efficient photoresponse. Hence, the present study focusses on the precise synthesis of high-quality, unipolar and ambipolar single-crystalline domains of pristine TMDC materials and their heterostructures. A comprehensive understanding of the charge transport behavior for the fabricated devices having potential to replace the state-of-the-art synaptic devices has been established.

2. EXPERIMENTAL SECTION

2.1. Synthesis. Single crystalline MoS_2, WS_2 and MoS_2 – WS_2 heterostructure domains were synthesized on degenerately doped P<100> Si substrates (resistivity ≈ 0.001-0.005 ohm-cm) coated with a 300-nm-thick SiO_2 over layer, using chemical vapor deposition techniques. The

growth strategy adopted for MoS_2 single crystalline flakes is the same as discussed previously.[31] Single-crystalline WS_2 flakes with domain sizes of 30-50 μm were grown using sulfur (S) and tungsten trioxide (WO_3) powders (3N purity) as precursors. The substrates were placed with polished side face down in the WO_3 precursor boat. The evaporation temperature of S and WO_3 is 113 °C and 900 °C, respectively. The deposition temperature was maintained at 950 °C. Due to the large vapor pressure difference between MoO_3 and WO_3, it becomes imperative to adopt a catalyst induced growth mechanism, in our case NaCl, to reduce the growth temperature.

A one step synthesis route is adopted to form MoS_2 – WS_2 heterostructure by placing the WO_3 and MoO_3 precursors in the upstream and downstream ends, respectively, relative to the position of the substrate. The MoS_2 – WS_2 heterostructures with spatially graded (vertical) and lateral geometry were synthesized by tuning the position of the substrate relative to the precursor boats. In case of lateral growth, WS_2 domains nucleated initially which then acted as cores for MoS_2 domains nucleating on the edges.

2.2. Fabrication of transistors. Electrical contacts were defined using electron-beam lithography (Elionix ELS-G100) in a PMMA mask (950K and 495K in anisole). After development, e-beam evaporation was used to deposit 110 nm of Au with a 3 nm Ti adhesion layer. Subsequently, the device was annealed to remove resist residue and lower the contact resistance. Titanium has been chosen due to its low work function which reduces the effective contact resistance.

2.3. Measurements and characterizations. The channel width varied between 5-30 μm due to the stochastic variation of single crystalline domains distributed on the substrate. Degenerately doped silicon wafers covered with 300 nm of silicon dioxide serves as the substrate and back gate. Drain and transfer characteristics of the fabricated devices were obtained at room temperature

using a Keithley 2400 Sourcemeter (source-drain) in conjunction with 6517A Electrometer (gate-source) and shielded probe station. The photoresponse characteristics are determined with Keithley 2400 sourcemeter and Oriel cornerstone 260 monochromator, using Xenon lamp for measuring current in light and dark conditions.

Raman and photoluminescence spectra of the samples were obtained using a Renishaw in via confocal Raman microscope from 100-500 cm^{-1}, with a 532 nm laser wavelength excitation source and 1800 lines per mm grating. The diffraction system uses a holographic diffraction grating with confocality control, and the detection system utilizes a high-sensitivity ultralow noise CCD camera. A laser power of <1 mW was employed to minimize sample damage. The optical images of the representative MS, WS and HS samples were obtained with the optical microscope attached to the Renishaw in via spectrometer. The films on silicon substrates were characterized using UV–visible spectroscopy (Perkin Elmer Lambda 35) in diffused reflectance mode. XPS was conducted in an ultra-high vacuum photoemission spectroscopy system (ULVAC-PHI, HAXPES) with chamber pressure less than $4x10^{-9}$ Torr. The topography, thickness and surface potential maps were obtained by AFM (Bruker, Dimension Icon SPM) in tapping mode using a platinum–iridium (Pt–Ir) coated Si cantilever tip (SCM-PIT from Bruker Inc. USA) calibrated against a standard sample for its work function.

3. RESULTS AND DISCUSSION

3.1. Microstructure, topographical and optical studies

The samples studied in the present work shall be named as MS (MoS_2), WS (WS_2), HS (MoS_2 – WS_2 heterostructure). The optical microscopy images of representative 2D MS, WS and the HS samples grown on SiO_2/Si substrates are shown in Figure 1a-c. As is evident from the micrographs,

the 2D flakes corresponding to MS, WS and HS exhibit a triangular morphology with sharp edges. However, the HS sample appears to be composed of triangular domains in lateral and vertical heterostructured configurations as is evident from Figure 1c. The vertical heterostructure (studied in the present work) is marked by two pristine domains of MS and WS with a common overlapping region as shown in the inset of Figure 1c. A typical domain size of ~ 50 μm, 30 μm and 15 μm is observed for MS, WS and HS sample. Since 2D materials offer huge flexibilities in terms of layer dependent tunable properties, individual samples having 3-4 layers (3-4 L) are chosen for further studies. The environmental adsorbates, such as water, hydrocarbons and gaseous products cover the two-dimensional surface. It has been found that few layered 2D devices are less affected by the environmental inhomogeneities, such as, humidity and oxygen in comparison to single layered devices where an encapsulating layer is necessary. It has already been established previously, the mobility and device properties of single layered 2D devices exhibit higher sensitivity to ambient air exposure and gaseous adsorbates in comparison to their few-layered counterparts. Moreover, mild photoreactions of gaseous environment with monolayer 2D flakes strongly impact their electrical and optical properties. Hence, it is more advantageous to fabricate devices based on few (3-4 L) layers due to their robustness and durability.[32-35]

Hence, 3-4L based MoS_2 and WS_2 devices not only retain the exceptional electrical and optical properties of corresponding single layered devices but also have additional associated advantages, including, robustness and stronger durability against environmental instability and degradation. Moreover, it is difficult to synthesize single layered heterostructure sample, i.e., MoS_2-WS_2 in which case the minimum number of possible layers is 3-4. Therefore, the present work was based on study of charge transport properties of 3-4L pristine MoS_2, WS_2 and their corresponding heterostructure sample, MoS_2-WS_2.

As Raman spectra provides signature of the number of layers in 2D TMDCs,[1, 36] the Raman spectra of synthesized samples (MS, WS & HS) were interpreted as shown in Figure 1d. The characteristic Raman fingerprint for MS (Figure 1d) exhibits two prominent peaks at 383 cm^{-1} and 407 cm^{-1}, corresponding to the E_{2g} and A_{1g} resonance modes, respectively, for a sample with 3-4 L. Similarly, the characteristic peaks of WS occur at ~ 351 cm^{-1} (2LA (M) mode) and ~ 421 cm^{-1} (A_{1g} mode) confirming our samples are 3-4 L. Raman spectra taken at the interface of the overlapping region of the vertical heterostructure shows characteristic peaks at 353, 419, 385, 408 cm^{-1}, corresponding to both WS_2 and MoS_2, respectively. The total number of layers in the heterostructure is calculated as a sum of the individual MoS_2 and WS_2 layers which comes out to be 3-4 L.

Figure 1e shows the results of photoluminescence (PL) spectroscopy measurements for MS, WS and HS samples. The optical properties of the materials were probed by diffused reflectance spectroscopy the results of which are shown in Figure 1f. The lowest energy excitation can be related to the excitonic transition corresponding to K and K′ points of the Brillouin zone. This excitonic transition results in two peaks, i.e., 'A' and 'B', due to the valence band maxima splitting at the K point. The pristine 2D MS and WS exhibited the expected spectral features with the lower energy peak 'A' corresponding to the band-edge transition and the higher energy peak 'B' arising due to the splitting of the valence band. The major peak 'A' is located around 677 nm (1.83 eV) for MS along with peak 'B' at around 626 nm (1.98 eV), as shown in Figure 1e.

Peak 'A' for WS as seen in Figure 1e is located at 663 nm (1.87 eV) along with peak 'B' at 620 nm (2 eV). The HS sample exhibits a superposition of peaks corresponding to MoS_2 and WS_2, as observed in Figure 1e. The presence of sharp peaks corresponding to intrinsic MoS_2 and WS_2 domains in the heterostructure sample suggests the presence of a chemically sharp interface

hosting interlayer interactions. Since 2D MoS_2 and WS_2 undergo direct band gap transition in the visible region in case of single layer to few layers, photoluminescence and reflectance spectroscopy can be employed as alternative routes to calculate their band gap. The band gap values observed from PL/ reflectance spectroscopy for MS, WS was 1.8 eV and 2.1 eV, respectively.

3.2. Surface potential studies

Figure 2 shows the topographical and surface potential (contact potential difference) maps, corresponding to MS, WS and HS samples obtained by Kelvin probe force microscopy (KPFM) measurements. The thicknesses of single crystalline domains in samples MS, WS and HS obtained from atomic force microscopy (AFM) topography maps (Figure 2a–c) as indicated by height curves in the inset are observed to be 2.8 nm, 3.8 nm and 5.5 nm, respectively. A clear contrast between two distinct regions in Figure 2c confirms the presence of a vertically grown WS_2 over triangular MoS_2 domain. The surface potential maps have been used to calculate the work function values corresponding to the three samples. In general, the sample work function (ϕ_{sample}) can be calculated from the relation

$$\phi_{sample} = \phi_{tip} - V_{CPD} \quad (1)$$

where (ϕ_{tip}) is the tip work function and (V_{CPD}) the contact potential difference.

The value of ϕ_{tip} was obtained to be 5.5 eV calibrated against standard HOPG, using the procedure outlined earlier.[31] Further, the contact potential difference values for MS, WS and HS calculated from the histograms corresponding to Figure 2d-f were observed to be 380 mV, 230 mV and 280 mV, respectively. The work function value calculated using the aforementioned equation for MS, WS and HS was 5.12 eV, 5.27 eV and 5.22 eV, respectively. The spread in the surface

potential depicting the contact potential difference values for the HS sample lying in between that of MS and WS is as shown in Figure 2g.

3.3. X-ray photoelectron studies

The bonding characteristics and stoichiometry of the MS, WS and the HS domains were studied using X-ray photoelectron spectroscopy (XPS), the obtained spectra are shown in Figure 3. After the subtraction of Shirley background, the spectra were fitted using the sum Gaussian-Lorentzian function (20% Gaussian + 80% Lorentzian). All the spectra were carbon corrected by assuming the C 1s binding energy to be at 284.6 eV. Figure 3a shows the characteristic Mo 3d doublet peak centered at 232.1 and 228.9 eV corresponding to Mo^{4+} $3d_{5/2}$, Mo^{4+} $3d_{3/2}$ confirming the formation of 2H-MoS_2.[37-38] Also, the S 2s peak can be seen centered at binding energy of 226.4 eV and a low intensity peak at 225.4 eV.[39] The marginal peak at 231 eV may correspond to Mo^{6+} $3d_{5/2}$, as reported earlier.[40] The lower intensity peak may exist due to the slight off-stoichiometry of the samples. The S 2p doublet (Figure 3b) can be seen at 163.5 and 162.3 eV and corresponds to the known 2H peaks of MoS_2.[41] The peak centered at 229.3 eV corresponds to MoO_2 which remains unreacted during the synthesis process on the substrate.[42] Similarly, the WS_2 peaks in Figure 3c at 31.9 eV, 34.04 eV and 37.4 eV correspond to the W^{4+} $4f_{7/2}$, W^{4+} $4f_{5/2}$ and W^{4+} $5p_{3/2}$.[43] The peak at 34.9 eV corresponds to the unreacted WO_3. The S 2p doublet peaks with binding energy of 162.4 and 161.2 eV can be assigned to S $2p_{1/2}$ and S $2p_{3/2}$, respectively, as seen in Figure 3d.

In order to understand the oxidation states of Mo and W in the HS sample, the corresponding XPS spectra have been analyzed. The Mo 3d peaks present at binding energy values of 229.1 eV and 232.3 eV shift from the pristine values of 228.9 eV and 232.1 eV present in pure MoS_2, confirming the existence of $3d_{5/2}$ and $3d_{3/2}$ states of molybdenum conforming with the reported difference of $\Delta \approx 3.1$ between the two peaks, as shown in Figure 3e. The S 2s peak is

deconvoluted into two peaks at 226.6 eV and an additional peak at 225.9 eV due to probable off-stoichiometric component. The slight shifting of 0.2 eV of the S2s peak can be attributed to the formation of the heterostructure. Similarly, the W 4f and 5p peaks in Figure 3f, occurring at 32.5 eV, 34.6 eV and 37.9 eV are shifted in comparison to the pure WS_2 peaks at 31.9 eV, 34.04 eV and 37.4 eV, yet maintaining the difference Δ = 2.1 eV between $4f_{7/2}$ and $4f_{5/2}$ peaks. The low intensity peak at 35.5 eV can be attributed to the presence of unreacted WO_3. The S 2p peaks of the heterostructure which occur at 163.2 and 162 eV, as shown in Figure 3g, confirm the presence of S^{2-} species in the heterostructure.

3.4. Energy band diagram

In order to understand the carrier transport and charge transport properties across the heterostructure it is imperative to determine the band offsets and band alignment for MS, WS and HS. To facilitate the above calculations, valence band spectra were obtained using the XPS studies, as shown in Figure 4a-c. The valence band maxima is obtained from the intersection point corresponding to linearly fitted lines ‘a’ and ‘b’ with the horizontal line. The valence band maxima for MS, WS and HS are calculated to be 1.3 eV, 1.2 eV and 1.08 eV, respectively (Figure 4a-c). The valence band maxima, work function and band gap values are used to understand the energy band diagrams of the three samples. Valence band maxima gives the position of the Fermi level (E_F) from the valence band maxima edge, whereas, the work function values calculated from KPFM studies gives the position of the Fermi level with respect to the vacuum level. The bandgap values estimated from PL and reflectance measurements give the position of the conduction band minimum with respect to the valence band maximum. The above parameters have been used to draw the energy band diagrams of MS and WS as shown in Figure 4d. It can be deciphered from the position of the Fermi level that as prepared MS is n-type, whereas, WS is weakly n-type as its

E_F is close to the intrinsic level. In the HS sample, the equilibrium is attained by the movement of electrons from low work function material (MS) to high work function material (WS) and a consequent alignment of the Fermi-level. The resultant heterostructure as shown in the Figure 4d has a type- II band alignment between MoS_2 and WS_2, as predicted in previous works.[44-45] The transistor characteristics of MS, WS and HS devices were also tested.

3.5. Device characteristics

The schematic diagram of the fabricated device in a single-crystalline, top-contact, back-gate configuration can be seen in Figure 5a while the corresponding optical image for MS, WS and the HS device is shown in Figure 5b-d, respectively. Incase of the HS device, the source electrodes are positioned on the WS_2 layer and drain electrodes on the MoS_2 layer which leads to formation of a vertical heterojunction between MoS_2 and WS_2. The overlapping region of the heterostructure, connecting the pristine flakes, can also be seen in Figure 5d. When a bias is applied, the electrons migrate from WS_2 to MoS_2 side to maintain the electron potential at a balance for the formed junction. The I-V characteristics of Figure 5g and Figure 5j are due to the formation of a junction between the two 2D materials. The drain and transfer characteristics of MS, WS and the HS FET devices are plotted in Figure 5e-j. In the present study the authors focused on low voltage (drain and gate bias) operation of the devices for better reproducibility, robustness and power efficient devices. 2D materials due to their exceptional flexibility have potential applications in electronic fibers and smart textiles fabricated on the weave of the textile requiring devices having low power consumption.[46-48] The details of initial tests performed for optimum range selection of drain and gate voltage have been explained in the supplementary information.

At zero gate voltage, when a bias is applied across the source-drain contacts, MS and WS devices show an asymmetrical sigmoidal behavior while the heterostructure device exhibits a

symmetrical sigmoidal nature. The metal-2D semiconductor contacts have been reported to exhibit a non-linear behavior in contrast to the Ohmic contact behavior, expected theoretically on the basis of their work function values.[49-50] In the present case, Au with a reported work function of 5.1 eV should ideally form an Ohmic contact with MS and WS with the experimentally (KPFM) determined work functions values of 5.12 eV and 5.27 eV, respectively. The non-linear asymmetry in the I-V behavior of the pristine 2D devices (MS and WS) can be attributed to the asymmetry between source and drain contacts which may be due to defects, inhomogeneities and Fermi level pinning.[49, 51] Also, the asymmetry due to the geometrical contact area of the metal electrodes on the 2D flakes leads to an uncontrollable difference of surface states, rendering asymmetric source and drain contacts. The HS when brought in contact with the metal electrodes exhibits an equilibrium state. On application of a bias, both the metal-contact barriers and the heterojunction are expected to contribute to the electrical transport. The observed symmetrical behavior in the HS device as opposed to asymmetrical behavior of the pristine devices maybe attributed to the dominant contribution of the junction.

With increasing forward bias of the gate voltage ($V_G > 0$) and at a positive source-drain bias ($V_D > 0$), the drain current increases with increasing gate voltages for MS, WS and the HS devices, as is evident from the drain characteristics shown in Figure 5e-g. At a negative source-drain bias ($V_D < 0$), there is a negligible increase in drain current for MS device with increasing positive bias of the gate voltage. On the contrary, WS and the HS devices show a decreasing drain current at a negative source-drain bias with increasing positive gate voltages. When a negative gate voltage ($V_G < 0$) is increased at positive source-drain bias ($V_D > 0$), the drain current in the three fabricated devices continually decreases. In contrast, for increasing negative V_G values and a negative source-drain bias ($V_D < 0$), a negligibly small decreasing current is observed in MS,

whereas, a linear increase in current is evident in WS and the HS device, respectively. The transfer characteristics corresponding to MS, WS and HS devices can be seen in Figure 5h-j. The transfer curves depict the n-type nature of MS device and an interesting ambipolar behavior of WS and the HS device which is further clarified in the semilog curves discussed later. The source – drain connections for the bottom gate to semiconductor channel region are shown in Figure S1 and vividly described in the supplementary information.

The observed properties of individual devices are understood with the help of semilog transfer curves shown in Figure 6. The MS device shows a typical n-type behavior as seen from the corresponding semilog transfer characteristics shown in Figure 6a. It is evident from the Figure that at different polarities of source-drain bias, a negative gate voltage turns ON the device, thereby, confirming the n-type nature of the device. This result can be correlated to the lower formation energy of sulfur vacancies in MoS_2, resulting in pinning of Fermi level near the conduction band edge of the material leading to the n-type conduction.[52-53] The Fermi level pinning at metal-2D interface owes its origin to metal and disorder induced gap states. This primarily arises due to defects in the crystalline structure of the host semiconductor or due to the induced states as a result of metal interaction. Consequently, the nanoscale defects or inhomogeneities are observed to exist at the metal-2D interface. In addition to the sulphur vacancies, subsurface defects in the transition metal layer have been identified as the main source of Fermi level pinning in the above studies.[54-55]

It may be mentioned that the stoichiometry of the material is found to be $MoS_{1.8}$ from XPS measurements, which supports the contention of sulfur deficiency. The WS device with its nearly symmetric "V"-shaped transfer characteristics at V_D = 0.1 V exhibits an ambipolar nature as is evident from Figure 6b, suggesting that based on biasing conditions both electrons and holes

contribute to the conduction. WS inherently forms a n-type semiconductor with electrons as the majority carriers in the forward biased condition of $V_G > 0$ and $V_D > 0$ V. However, at a particular negative V_G and V_D, channel region gets depleted of electrons and dominating hole current flows from source to drain. XPS analysis confirmed the presence of W:S in a ratio of 1:1.97. The lower concentration of sulfur vacancies results in a weakly n-type nature of WS with Fermi level close to the intrinsic level (see Figure 4d). This is one of the major reasons for the observed ambipolarity in WS, as reported earlier.[56] The "U"-shaped transfer characteristics exhibited by HS device show a typical ambipolar behavior. The individual contribution of Mo and W in the heterostructure is 20% and 18.2%, respectively, as calculated by XPS. At $V_D = \pm 0.1$ V, with changing polarity of gate voltage, equal charge carriers (electrons and holes) flow through the channel region. Further, on application of $V_D = \pm 0.4$ V, the current switches from electron dominated to hole dominated, as seen in Figure 6c. Ease of switching between ambipolar to unipolar conduction or a selective transport of electrons or holes at low gate voltages, due to the asymmetric "U"-shape curves, presents an advantage for use of the designed ambipolar heterostructure in real-time applications.

In order to exploit the optoelectronic properties, understanding the origin of ambipolar behavior of WS and HS becomes imperative. The NaCl precursor assisted growth during WS and HS synthesis results in creation of impurities and defects on the surface of the otherwise defect-free SiO_2 substrate. It is known that during sample preparation SiO_2 adsorbs lighter impurities, such as, Na^+ ions on its surface.[57-58] These impurities manifest as localized charge traps influencing the accumulation of electrons or holes. On application of gate voltage, the energy of these localized gap states is close to either valence band maxima or conduction band minima giving the material its characteristic conductivity. Hence the conductivity shifts from n-type to p-type depending on charge polarity of traps and their energy level alignment within the band gap of the 2D material.

In order to gain further insight into the underlying mechanism of the charge carrier transport in the three devices, it is important to understand the band alignment as a function of V_D and V_G. We draw the energy band diagrams corresponding to the four quadrants spanned by gate (x-axis) and drain (y-axis) voltages. The energy band bending is initiated from the centre point 'o' at $V_D = 0$ and $V_G = 0$ V, with the four quadrants representing different bias conditions. Taking into account the M-S-M structure, the current flow across the Schottky barriers present at the source and drain contacts can be visualized as passing through two Schottky diodes connected back to back. For the first case in Figure 6d, considering the MS device, as the back gate voltage is swept from -10 V to +10 V, the channel varies from completely depleted n-type to an accumulated n-type, being composed of majority electron carriers. With a positive V_G, the conduction and valence bands are bent downwards reducing the barrier width and facilitating the injection of electrons from source to drain at positive V_D. An increase in charge carriers increases the overall current in the channel region in case I. Keeping the polarity of V_G the same, a reverse current with reduced magnitude flows across the channel region at negative V_D in case II. The difference in magnitude of currents for positive and negative V_D maybe due to the asymmetrical source and drain contacts, as discussed earlier. At positive V_D, reversing the gate bias effectively increases the depletion region formed between the channel and gate junction, resulting in a reduced channel current with increasing negative V_G as seen in case IV. At this polarity of V_G if V_D is changed to a negative bias (case III), the channel is completely depleted of its majority charge carriers, resulting in a negligible drain current. For a Schottky barrier existing between the metal - 2D semiconductor contact, carrier injection from a 3D metal into a 2D semiconductor is a result of two competing phenomena, namely, the thermionic emission and thermally assisted tunneling.[59-60] For a constant barrier height, gate voltage changes the corresponding barrier width. As thinner barriers lead to

higher injection of current, the Schottky barrier height increases for lower widths in order to maintain the charge neutrality level.[59]

In the case of WS, spanning the gate voltage from negative to positive value, field effect transistor changes from p-type to n-type at different polarities of V_D as seen in Figure 6e. A positive V_D and a forward biased (positive) V_G as in case I, an injection of majority charge carriers, i.e. electrons, occurs from source to the channel region, thereby, increasing the drain current. Hence, WS behaves as a n-type semiconductor. Keeping the polarity of V_G constant, if V_D is reversed as in case II, injection of electrons from drain to source is counterbalanced by minority carriers injected from source to drain. Hence an overall reduction in drain current occurs with increasing gate bias. At this polarity, if V_G is reversed, contrary to the expected decrease in current due to reduction in charge carriers as a result of widening depletion region and reduced channel width, an increase in current is observed. This may be attributed to the ambipolar nature of the material, resulting in holes becoming the majority charge carriers. With increasing gate voltage, drain current increases due to an effective injection of holes from source to drain. The FET in this bias scenario as seen in case III behaves as p-type with holes as majority charge carriers. At this polarity, reversing V_{DS} as in case IV results in reduced drain current due to counterbalanced flow of electrons as minority charge carriers in the FET.

A similar case of HS ambipolarity can be depicted in the form of band diagrams as shown in Figure 6f. Initially at positive V_D with increasing positive V_G, as in case I, barrier width keeps reducing, increasing number of electrons that are injected from the source into the channel region, resulting in an increasing drain current, supporting the flow of majority charge carriers i.e., electrons. If V_D is reversed in such a biased condition, reduction in current is observed with increasing gate voltage. This may be attributed to counterbalancing by minority charge carriers in

the channel, as depicted in case II. Further reversing the gate polarity from this bias condition, increases the injection of holes in the channel which becomes the majority carriers in this case. Hence the FET turns its conduction from n-type to p-type (case III). Further changing the polarity of V_D results in the flow of minority carriers (electrons) from source to drain, effectively reducing the overall drain current. Due to the fast switching between ambipolarity (at V_D = 0.1 V) and unipolarity (at different V_D) in the HS, a reduced flow of minority carriers is observed which can be essentially manifested in the drain current.

From the semilog transfer curves, the measured ON/OFF ratio comes out to be 10^3 for the MS device with a subthreshold swing of 668 mV/decade, at room temperature. For WS device, the ON/OFF ratio is 10^2 with a subthreshold swing of 826 mV/decade. The ON/OFF ratio for the heterostructure device is 10^1 with a subthreshold swing of 4.35 V/decade. In the linear region of transfer characteristics, the field effect mobility is given as,

$$\mu = \frac{L}{W * C_{(j)}} * \frac{d(g_m)}{d(V_G)} \tag{2}$$

where, μ is the mobility, L and W, are the length, width of the channel, C_j is the gate capacitance, V_G is the gate to source voltage and g_m, the transconductance, is given as dI_D/dV_G. However, considering the effect of Schottky-barrier induced contact resistances which result in a voltage drop at the source and drain end, a Y-function defined as $I_D/\sqrt{g_m}$ which is independent of R_C, is given as,

$$\sqrt{\frac{W \mu_0 C_j V_D}{L}} (V_G - V_{th,0}) \tag{3}$$

where μ_0 and $V_{th,0}$ represent the values of mobility and threshold voltage corrected by exclusion of the effect of contact resistance R_C, L and W, are the length, width of the channel, C_j is the gate capacitance, V_G is the gate to source voltage and V_D is the source to drain voltage. Thus, the slope of the linear region of $I_D / g_m^{½}$ vs. V_G gives the value of corrected field effect mobility and the intercept with x-axis gives the value of the threshold voltage. Using the stated analysis, the electron mobility for MS device is obtained as 1.23 cm^2/V.s. The electron and hole mobility for the WS device is calculated to be 3.32 cm^2/V.s and 3.64 cm^2/V.s, respectively. For HS device, a high electron mobility of 19 cm^2/V.s and a high hole mobility of 20 cm^2/V.s is obtained.

It is important to highlight that the gate voltages needed to turn the device ON (or the threshold voltages) are the lowest for WS device followed by the HS and the MS device. Threshold voltage (V_{th}) calculated at the point of maximum transconductance at V_D = +1 V is -12.2 V for MoS_2. The ambipolar devices exhibit threshold voltages corresponding to both electron and hole current. For instance, the WS device has threshold voltage values of -0.28 V and +0.27 V for V_D = ±1 V. Similarly, for the HS, V_{th} = -2.9 V and V_{th} = +3.14 V for V_D = ±1 V. Any transition from the neutrality point at V_G = 0V shifts the FET behavior from ambipolar to unipolar due to the carrier injection with application of source-drain bias. In the case of the HS, switching from ambipolarity towards unipolarity occurs with improved electron and hole currents. The corrected values of mobility and threshold voltages have been tabulated in Table 1, respectively. For further understanding additional figures which illustrate a typical example of the calculations of corrected mobility and threshold voltage for the MS device have been included in the supplementary information.

3.6. Performance of CMOS switch

Previous studies performed on intrinsic MS sample reveals its potential for broadband and wavelength selective optical sensing as a function of number of layers.[6] The coupling strength of the isolated MS and WS layers governs the charge transfer and absorption of incident light in the HS sample. The time response photocurrent plots shown in Figure 7a-c for MS, WS and the HS under white light irradiance indicate that the well-defined ON-OFF switching behavior is retained for multiple cycles. The current ramps to a high value when light is turned ON and drops back to a low value when light is turned OFF, as seen from the corresponding figures. The sensitivity (S), a measure of the performance of a photodetector, calculated using the formula $S = (I_L – I_D)/ I_D$, where I_L is the photocurrent (in light) and I_D is the dark current, is 1.32, 0.117 and 0.77 for MS, WS and the HS device, respectively. Due to the well balanced ambipolar properties of the WS and the HS device, electron and hole conduction can be modulated by tuning the gate voltage from positive to negative bias. Combining this property with the optical sensing capacity of the devices, HS device can be effectively used in CMOS photodetector circuits where a single material can detect light with gate tunable switching. Transistor devices with ambipolar behavior have a high potential for applications in next-generation nanoscale electronics such as logic circuits. We present a prototype CMOS inverter switch with high (±1) and low (0) operations governed by the gate tunable charge carriers as shown in the schematic of Figure 7d and the corresponding circuit diagram in Figure 7e. For an n-type operation, logic high and low can be realized with $V_G = +5$ V and $V_G = 0$ V in light ON and OFF, conditions. Similarly, for a p-type operation, logic high and low is realized with $V_G = -5$ V and $V_G = 0$ V in presence and absence of light. A -5 V input connects the p-type transistor to output, whereas, a +5 V input connects the n-type transistor to the output, thereby realizing an inversion operation.

A sharp increase in drain current is observed in Figure 7f when gate voltage is increased to 5V in both positive and negative polarity when light is turned On. In the light Off state, the drain current reduces to a negligibly small value at zero gate voltage. This result suggests that the easily processable, high quality heterostructures have properties suitable for device applications. Low dimensional material based devices having potential in CMOS technology are promising candidates for implementation in synaptic devices offering excellent bio-compatibility and electrical response with high flexibility owing to their optoelectronic and mechanical properties.[61]

4. CONCLUSIONS

In conclusion, we have systematically studied the electrical and opto-electronic behavior of back-gated FETs fabricated using single crystalline 2D flakes of TMDCs synthesized by chemical vapour deposition on SiO_2/ Si substrate. The understanding of interlayer interactions in vertical heterostructure was supported by a type-II band alignment between MoS_2 and WS_2, revealed by our systematic material characterization, including PL, KPFM and XPS studies. Successful operation of ambipolar and n-type conduction behaviors of the fabricated FET devices was achieved. A high ON/OFF ratio (~10^3) apart from a low subthreshold swing (668 mV/decade) of n-type MoS_2 FET, consistent with the previous findings, demonstrates its potential in high speed switching applications. The low threshold voltages for WS_2 and MoS_2 - WS_2 heterostructure devices along with high electron and hole mobilities suggest suitability for low power applications. Moreover, the low threshold voltages of WS_2 (-0.28 V) and MoS_2 - WS_2 heterostructure (-2.9 V) devices achieved at a positive drain voltage (V_D = +1 V) ensure that drawbacks associated with techniques used for threshold voltage engineering can be circumvented. The present work paves way for a precise modulation of electronic conduction behaviour between n-type and ambipolar transport, depending on chemically active species present during the synthesis. A successful

demonstration of a logic CMOS inverter switch fabricated utilizing the ambipolarity and high photoresponse of the heterostructure, capable of detecting light with gate tunability was achieved. The study hence, demonstrates the enormous potential of 2D semiconductor materials in future electronic devices.

ASSOCIATED CONTENT

Supporting Information

The following information is available free of charge.

Detailed information on the electrical connections between source – drain and gate – source with corresponding charge distribution for MS, WS and HS devices for n-channel and p-channel operation under different gate biases. The optimum ranges required for drain and gate biases and detailed mobility and threshold voltage calculations described. (PDF).

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FIGURES

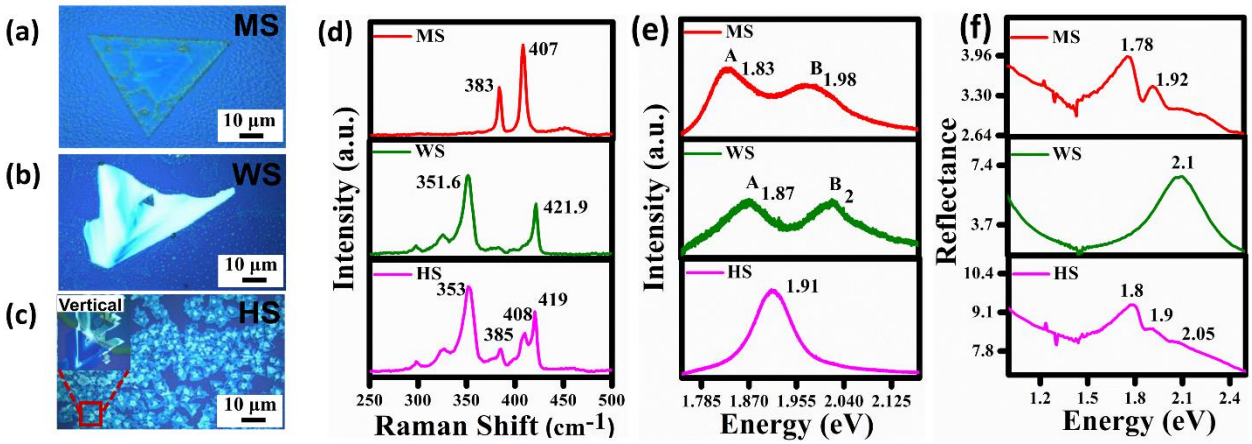


Figure 1. Optical micrographs for typical 3-4 layered MS (a), WS (b) and HS samples (c). The inset in (c) shows the vertical heterostructure within the HS sample. The Raman spectra for 3-4 L MS, WS and HS samples are shown in (d). Photoluminescence spectra for 3-4 L MS, WS and HS samples are as shown in (e). Reflectance spectra of a typical 3-4 layered sample showing a comparison between pristine material (MS & WS) and heterostructure (HS) is shown in (f).

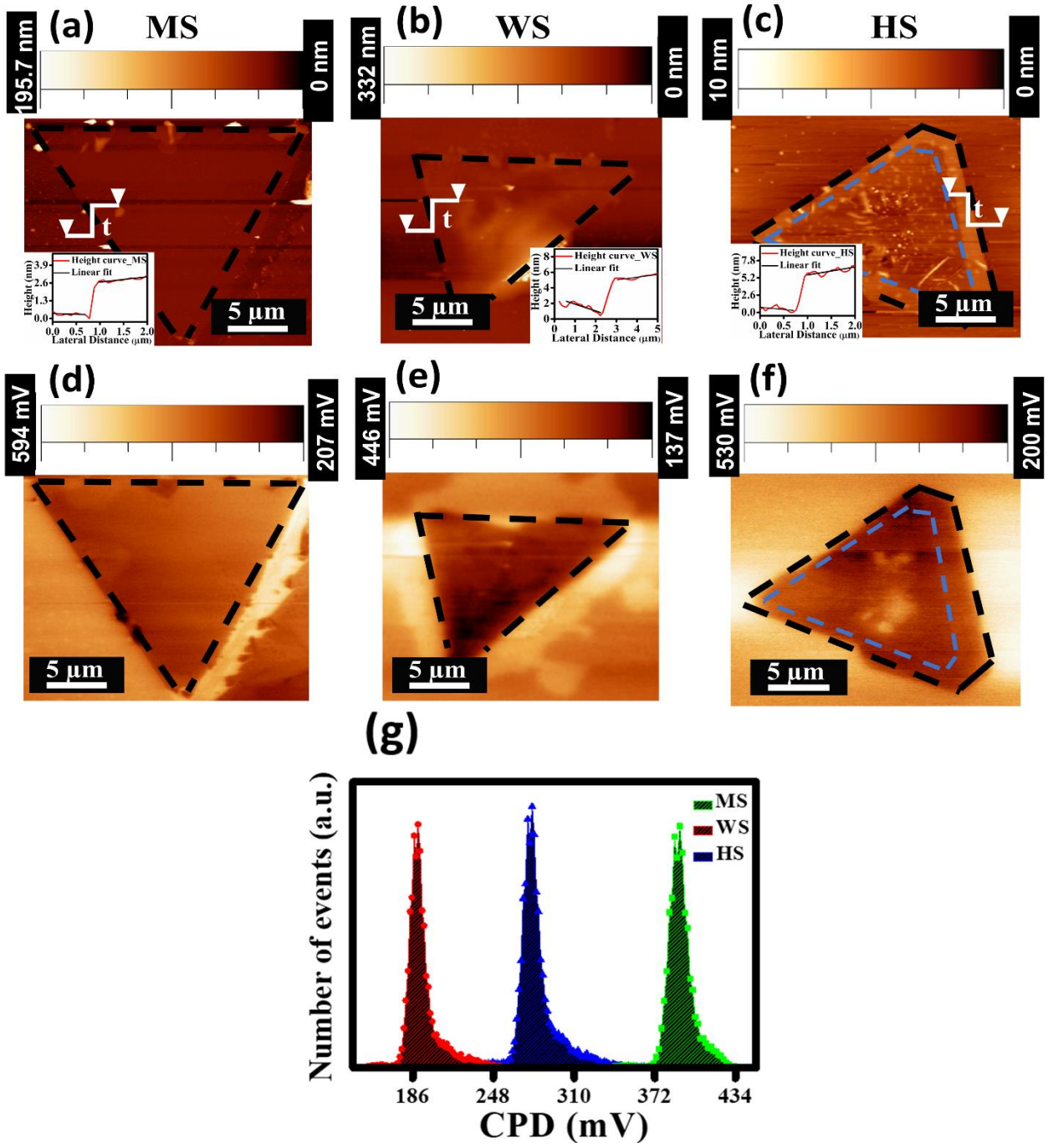


Figure 2. KPFM topography maps shown in (a) to (c) with the inset showing the corresponding height profiles and their corresponding surface potential images for MS (d), WS (e) and HS (f) for typical 3-4 layered sample. Histograms showing the contact potential difference in (g) for the three samples.

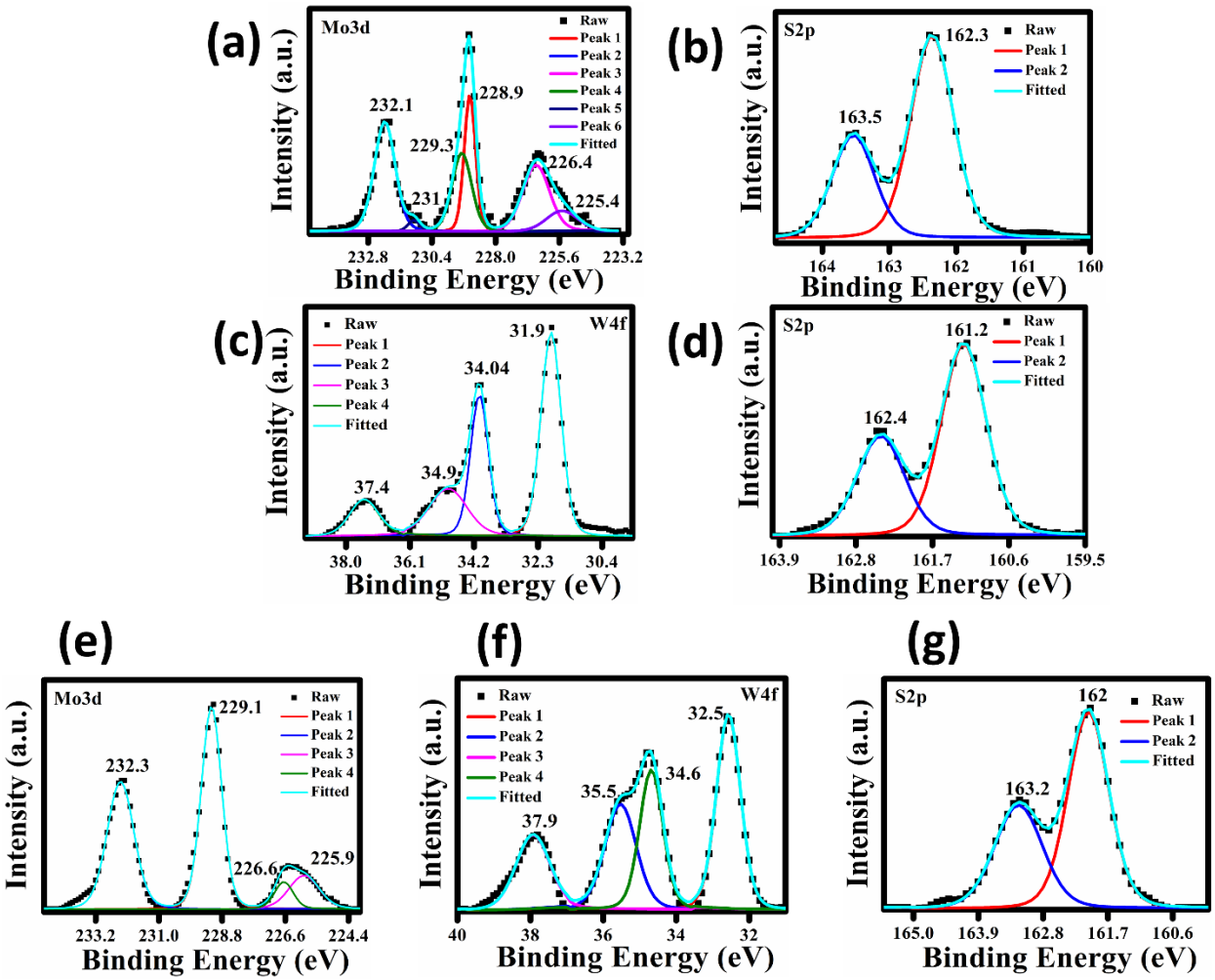


Figure 3. XPS spectra for MoS_2 (Mo 3d, S 2s and S 2p) in (a) & (b), WS_2 (W 4f, S 2p) in (c) & (d) and MoS_2 – WS_2 heterostructure in (e) to (g).

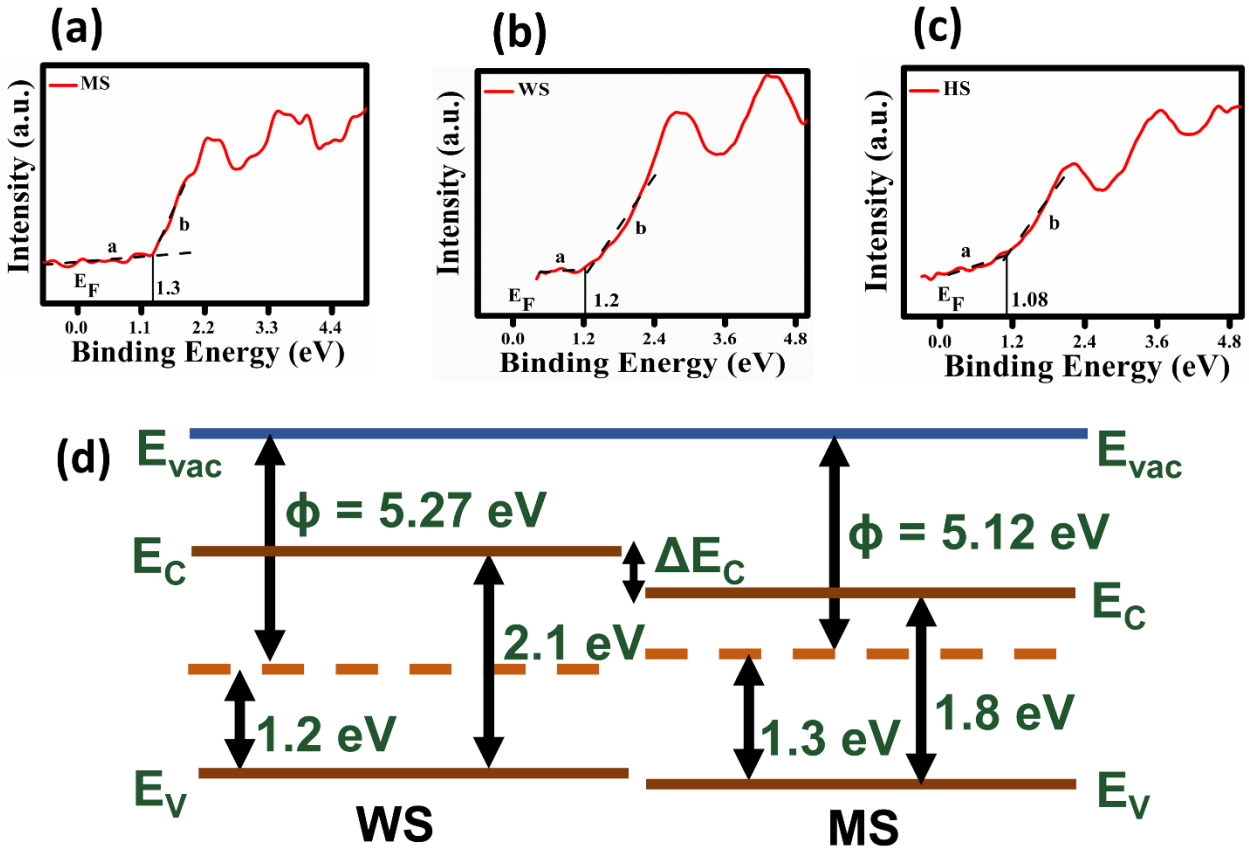


Figure 4. Valence band spectra for MoS_2 (MS) (a), WS_2 (WS) (b) and MoS_2 – WS_2 heterostructure (HS) (c) sample. Schematic energy band diagrams showing band bending for HS is shown in (d).

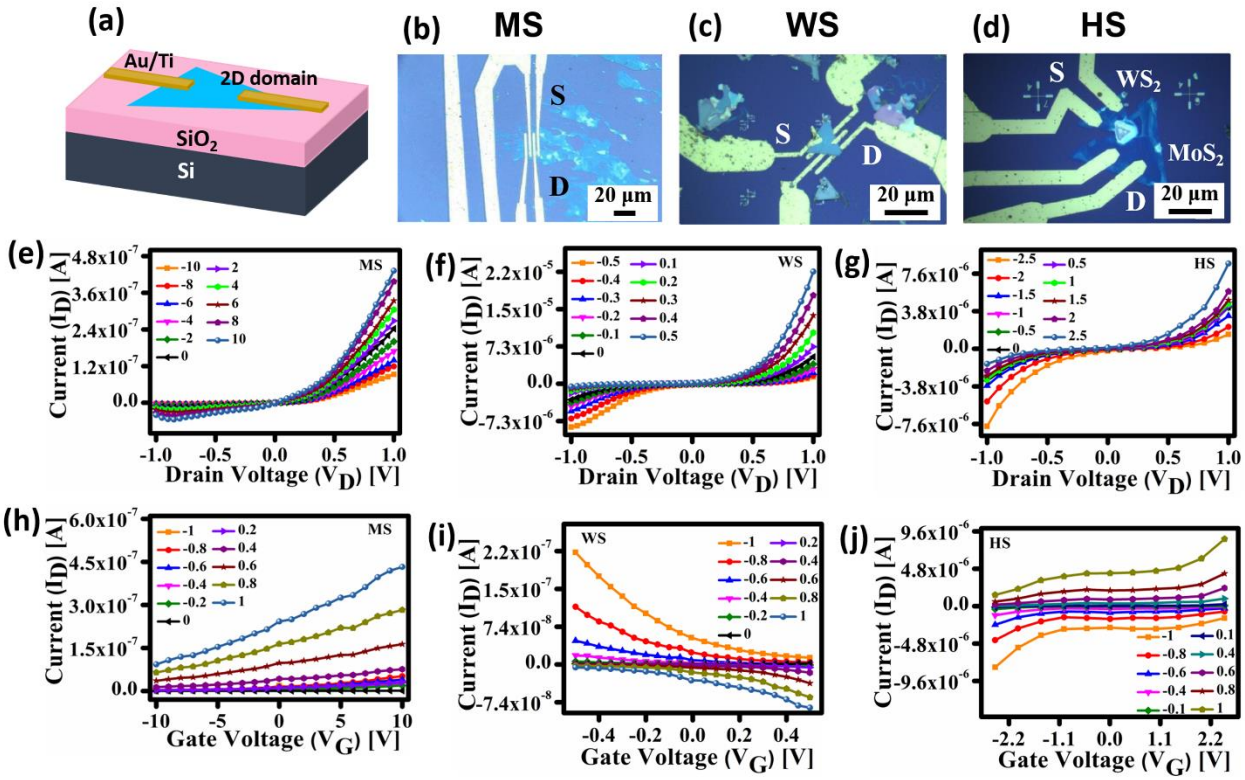


Figure 5. Schematic representation of a 2D FET with highly doped silicon as the back gate is shown in (a). Optical image of the integrated circuit constituting the fabricated metal contacts on MS (b), WS (c) and HS (d) samples, respectively. Device characteristics for MS, WS and HS FET devices. The drain characteristics describe the source – drain current (I_D) versus drain voltage (V_D) for varying gate voltages of the above-mentioned devices are shown for MS, WS and HS in (e), (f) and (g). The corresponding transfer characteristics shown as a variation of source – drain current (I_D) versus gate voltage (V_{GS}) at varying drain voltages in (h), (i) and (j).

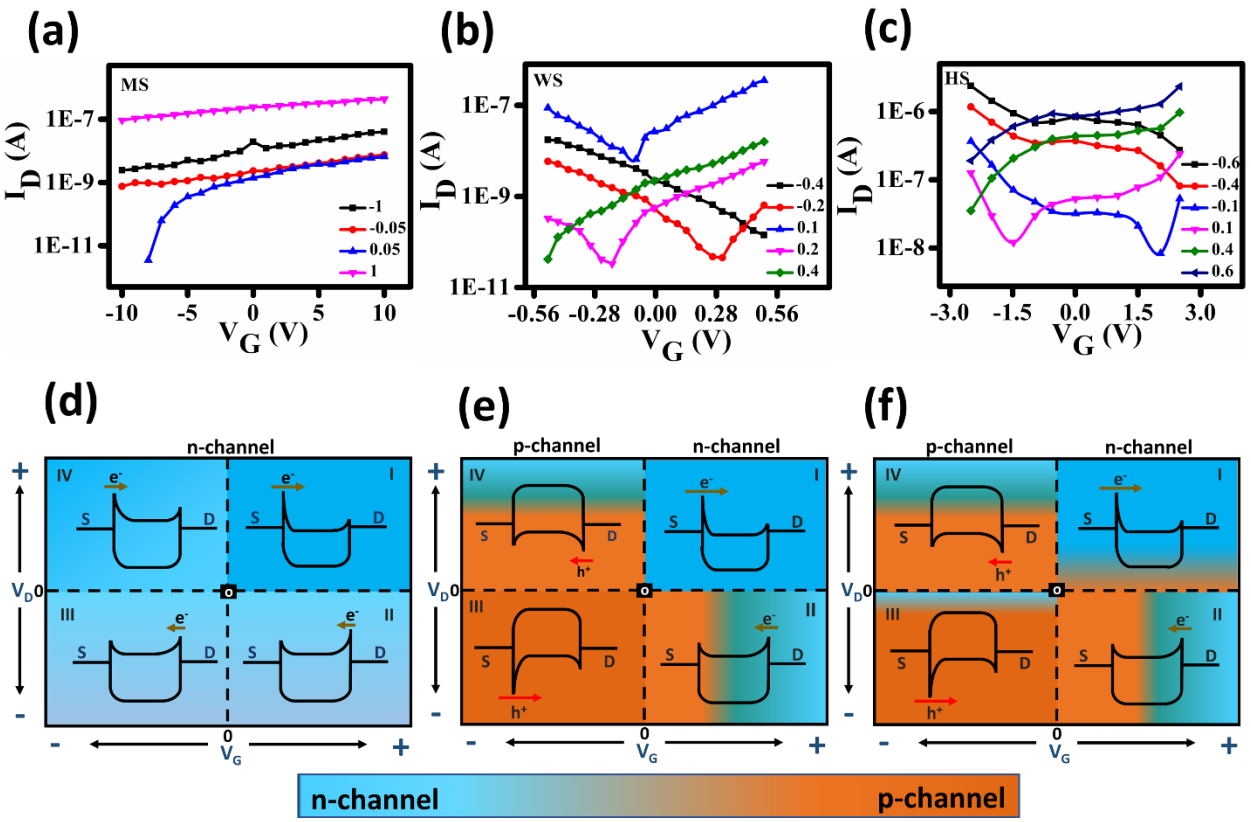


Figure 6. Semilog transfer characteristic graphs for MS (a), WS (b) and HS (c) FET devices. The band bending due to positive or negative gate voltage bias for varying drain to source voltages gives the n-type and p-type behavior dominant in the respective samples. Energy band diagrams for MS (d), WS (e) and the HS sample (f) under varying biases illustrating electron, hole injections for n-channel and ambipolar transport behavior. Color scale represents the transitioning gradient from n- to p-channel, respectively.

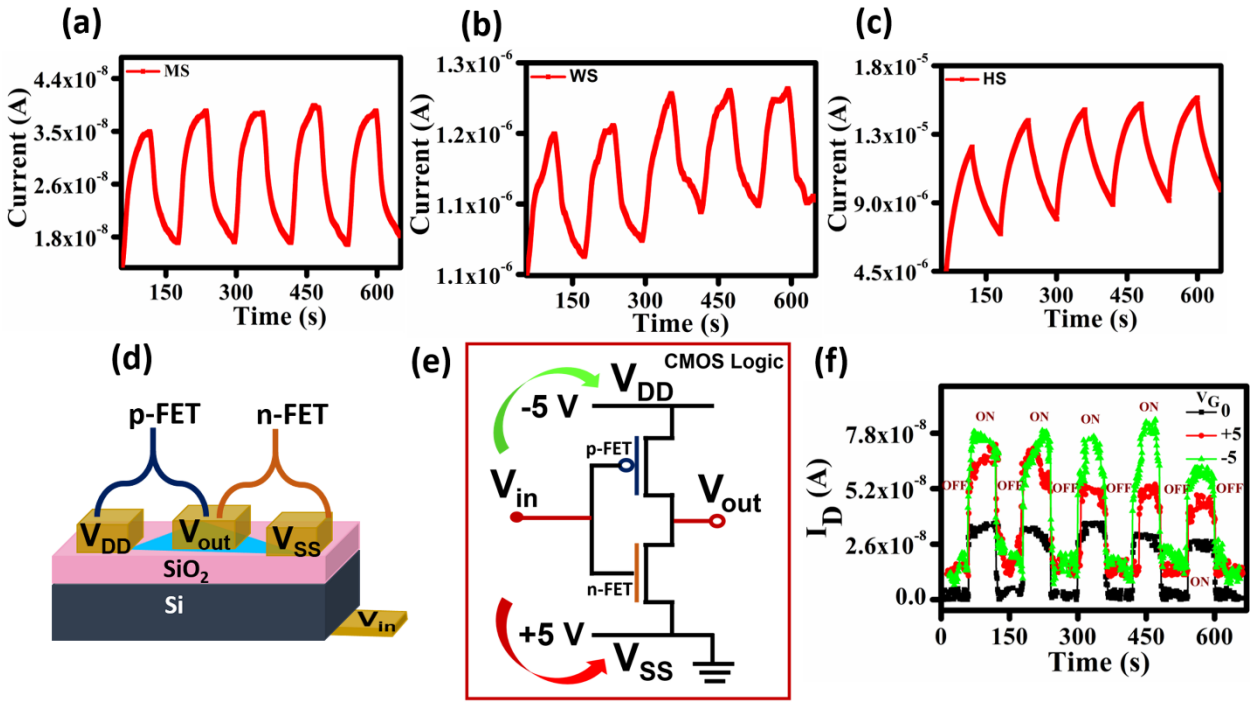


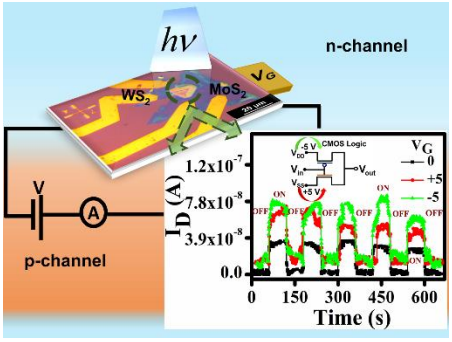
Figure 7. Photoresponse (white light) characteristics for MS (a), WS (b) and HS (c) FET devices are shown. The measurement is taken at V_{DS} = 1 V, V_G = 0 V. The schematic of a prototype CMOS like inverter switch with p- and n-type ambipolar heterostructure FET is shown in (d) with the corresponding circuit diagram in (e). The I-t characteristics with varying gate voltages is shown in (f).

TABLES

Table 1. Mobility and threshold voltage values of MS, WS and HS devices at $V_D = \pm 1$ V.

	Mobility (V_D = +1 V)	Mobility (V_D = -1 V)	Threshold Voltage (V_D = +1 V)	Threshold Voltage (V_D = -1 V)
MS	**1.23 cm^2/V.s**	**---**	**- 12.2 V**	**---**
WS	**3.32 cm^2/V.s**	**3.64 cm^2/V.s**	**-0.28 V**	**+0.27 V**
HS	**19 cm^2/V.s**	**20 cm^2/V.s**	**-2.9 V**	**+3.14 V**

TOC Graphic


hν
n-channel
WS2
MoS2
VG
V
A
p-channel
CMOS Logic
-5 V
+5 V
Vout
VG
0
+5
-5
ON
OFF
1.2x10-7
7.8x10-8
3.9x10-8
0.0
ID (A)
0
150
300
450
600
Time (s)