A Virtual Synchronous Machine-based Control for Eliminating DC-side Power Oscillations of Three-Phase VSCs under Unbalanced Grid Voltages

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***Abstract*—This paper presents a Virtual Synchronous Machine (VSM)-based control method for avoiding dc-side power oscillations in grid connected voltage source converters (VSCs) when operating under under unbalanced conditions. The proposed implementation is based on a Current Controlled VSM (CCVSM) where the positive sequence current references are determined by a virtual impedance and the emulated swing equation. Thus, the VSM-based control is synchronized to the positive sequence grid voltage, while the elimination of double frequency power oscillations due to the unbalanced voltage is obtained by controlling the negative sequence currents. The negative sequence current reference calculation is based on the modulation signals of the converter instead of the ac voltage measurements as in previous approaches. This prevents double frequency oscillations in the power flow and in the dc side voltage due to the unbalanced currents flowing in the filter inductors. The performance of the proposed method is demonstrated by time-domain simulations and compared to a VSM-based control where voltage measurements are utilized to eliminate power oscillations at the grid-side of the filter inductors.**

Keywords— Grid connected Voltage Source Converters, Negative Sequence Current Control, Unbalanced Grid Voltage Conditions, Virtual Synchronous Machines

I. INTRODUCTION

Increasing shares of non-synchronous generation is leading to growing concerns on the declining equivalent inertia in power systems [1]-[3]. To address this issue, extensive research on control methods for providing virtual inertia from power electronic converters has been conducted during the last two decades [4]-[6]. Thus, various control schemes including functionality for inertia emulation have been proposed for power converters in a wide range of applications. As a specific category of control methods for providing virtual inertia, the concept of Virtual Synchronous Machines (VSMs) based on explicit emulation of the electromechanical swing equation of synchronous generators has been extensively studied [6]-[9]. The VSM concept also has the advantage of providing inherent "grid-forming" functionality. Thus, VSM-based control strategies can be especially suitable for operation in weak or isolated grid conditions [6], [7].

The design, analysis and operation of different implementations of VSM-based control has until now been mainly studied under balanced operating conditions. However, the challenges of operation during unbalanced conditions has also recently attracted attention. Indeed, operation with unbalanced voltages when connected to a strong grid as well as operation with unbalanced load in smaller islanded grid configurations have been studied in [10]-[18]. From these studies, it is clear that objectives for the power flow control and the challenges of ensuring intended operation will differ between grid-connected and islanded conditions [18].

For designing VSM-based control strategies capable of grid connected operation under unbalanced voltage conditions, the most common approach until now has been to control the negative sequence current components to shape the power flow characteristics [12]-[16], [18]. Thus, an inner current control loop is typically applied together with a strategy for calculating the negative sequence current references, while the positive sequence current references are generated by the emulation of the SM characteristics. The most common control objectives for calculating the negative sequence current references are then to obtain i) balanced three phase currents, ii) elimination of active power oscillations or iii) elimination of reactive power oscillations. Especially, the possibility of utilizing the control of the negative sequence currents to eliminate double frequency oscillations in the power flow can be attractive in several common applications of Voltage Source Converters (VSCs). Indeed, elimination of double frequency power oscillations can enable operation with reduced dc-side capacitance, although this will limit the power transfer capability during unbalanced conditions [19]. Elimination of double frequency oscillations in the dc voltage can also be important for avoding uncontrolled propagation of double frequency power oscillations in VSC-based dc grids [20].

The VSM-based control methods presented in [12]-[16], -[18] include the option of eliminating the power oscillations at the point where the grid voltages are measured, which for a VSC is typically at the grid-side of the filter inductors. However, the introduction of negative sequence currents that will eliminate the double frequency power oscillations at the grid side of the filter inductors will not necessarily eliminate

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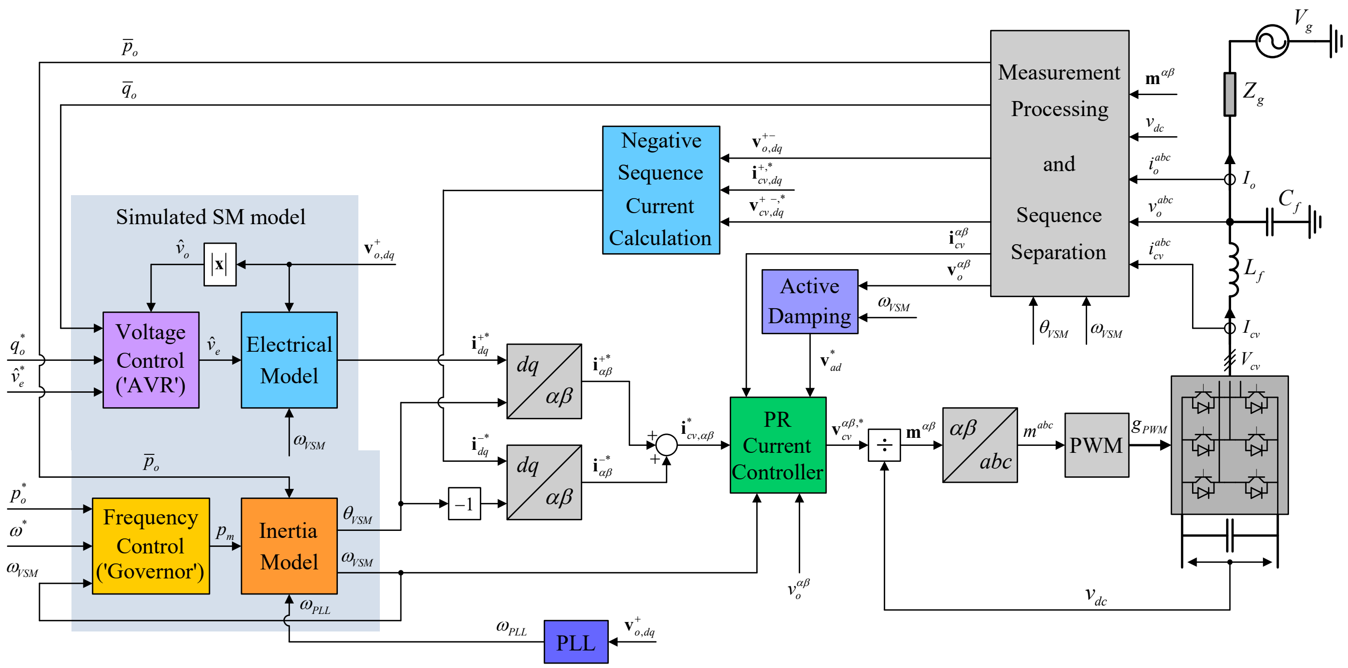


Fig. 1 Overview of the CCVSM-based control strategy for unbalanced grid-connected and islanded operation

the power oscillations in the converter. Indeed, the unbalanced currents flowing in the filter inductor will cause a small remaining double frequency power oscillation that will be reflected in the dc voltage. Thus, to effectively eliminate dc-side voltage oscillations, the double frequency power oscillations flowing in the converer, and not the power oscillations at the filter terminals, should be eliminated.

In this paper, a method for eliminating double frequency oscillations in the power flow is proposed for a VSC operated as a VSM. The method is inspired by the control strategy proposed in [20], where the voltage references for operation of the VSC instead of the measured voltages at the filter capacitors are utilized for calculating the current references under unbalanced voltage conditions. Thus, the same approach is applied in this paper by utilizing the modulation signals for the converter to calculate the negative sequence current references of a VSM that will eliminate the double frequency oscillations in the power flow at the converter terminals during grid-connected operation with unbalanced voltages. The basic principles of the assumed VSM implementation and the derivation of the proposed approach for negative sequence current references calculation are adapted from [18] by applying the approach from [20]. Then the intended operation of the resulting control strategy is verified by time-domain simulations and compared to a VSM-based control strategy where the measured grid voltages are utilized for calculating the negative sequence current references.

II. OVERVIEW OF VSM-BASED CONTROL STRATEGY FOR OPERATION UNDER UNBALANCED CONDITIONS

The configuration analysed in the paper is shown in Fig. 1. A two-level VSC is assumed to operate as a Current Controlled VSC (CCVSM), based on the implementation presented in [18]. An LC filter is used as the interface between the VSC and the main grid, which is represented by a Thevenin equivalent. Since the equivalent grid impedance is assumed to be relatively small, the impact from the VSC operation on the local grid voltage is limited. In the following, lowercase letters are used to indicate per-unit quantities used in the control, while uppercase letters indicate physical quantities.

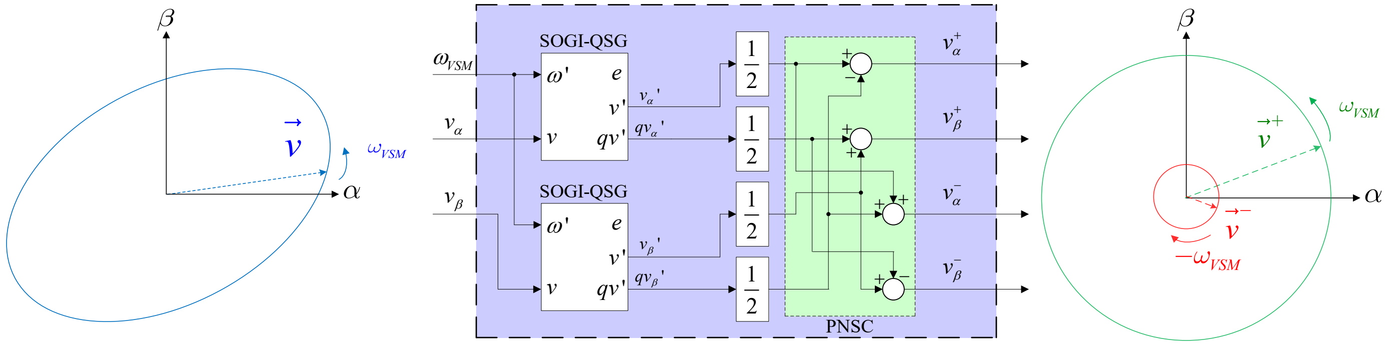
A. *CCVMS control structure*

The structure of the CCVSM implementation shown in Fig. 1 is directly adapted from the control system presented in [18]. Thus, the inner loop current control is based on a set of Proportional-Resonant (PR) controllers implemented in the stationary $\alpha\beta$ reference. These controllers ensure the capability to control positive and negative sequence currents by operating directly on the $\alpha\beta$-components of the converter currents $\mathbf{i}_{cv}$. Furthermore, active damping of LC filter oscillations is implemented for each current component by utilizing a frequency-adaptive band-pass filter based on a second order generalized integrator (SOGI) configured as a quadrature signal generator (QSG) [18], [21].

B. *Power control under unbalanced conditions*

In order to control the VSC under unbalanced working conditions, it is necessary to obtain the positive and negative sequence components of the grid voltages and currents. This is achieved according to [21] by a dual set of SOGI-QSGs.

Using the voltage as an example, Fig. 3 shows how the unbalanced voltage given by the blue trajectory in Fig. 3 (a) is processed by the sequence separation according to the block diagram in Fig. 3 (b). Thus, the DSOGI-QSGs structure generates the in-phase and in-quadrature components required for positive and negative sequence calculation (PNSC). Differently from [21], the frequency adaptivity of the DSOGI-QSG is directly obtained by using the VSM speed without relying on frequency estimation of the measured grid voltage. The outputs of the block diagram are the positive and negative sequence voltage components, as shown in Fig. 3 (c) by the



(a) (b) (c)

Fig. 3 Sequence separation of voltage measurements by DSOGI-QSG with frequency adaptivity provided by the VSM speed

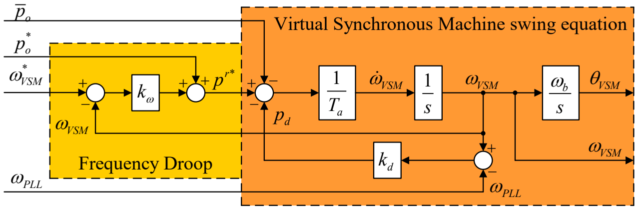


Fig. 2 Virtual synchronous machine swing equation operated with an ideal frequency droop as a 'governor' function

green and red trajectories of the corresponding voltage vectors rotating with speed ω_{VSM} and $-\omega_{VSM}$, respectively.

Active and reactive power feedbacks are necessary to implement the voltage and frequency controls respectively, as indicated in Fig. 1. The dc-componetns of these quantities can be estimated using the positive and negative components of the acquired voltages and currents as:

$$\begin{aligned}\bar{p}_o &= v^+_{o,\alpha}\cdot i^+_{o,\alpha} + v^+_{o,\beta}\cdot i^+_{o,\beta} + v^-_{o,\alpha}\cdot i^-_{o,\alpha} + v^-_{o,\beta}\cdot i^-_{o,\beta} \\ \bar{q}_o &= -v^+_{o,\alpha}\cdot i^+_{o,\beta} + v^+_{o,\beta}\cdot i^+_{o,\alpha} - v^-_{o,\alpha}\cdot i^-_{o,\beta} + v^-_{o,\beta}\cdot i^-_{o,\alpha}\end{aligned} \tag{1}$$

The inertia emulation and the power control are implemented according to the strategy presented in [18], [22]. Thus, the 'governor' function of Fig. 1 is implemented as an ideal frequency droop generating the reference power for the VSM as sum of the external power reference setpoint p_0^* and a term proportional to the frequency error. By applying a swing equation according to [22] as the inertia model, the VSM speed is defined by:

$$T_a \frac{d\omega_{VSM}}{dt} = p^* + k_\omega\left(\omega^*_{VSM} - \omega_{VSM}\right) - \bar{p}_o + k_d\left(\omega_{VSM} - \omega_{PLL}\right) \tag{2}$$

The scheme of the VSM and the frequency droop control is reported in Fig. 2, where k_ω is the droop gain, ω^*_{VSM} is the frequency reference, ω_{VSM} is the emulated VSM speed, and k_d is the damping coefficient. A phase locked loop algorithm (PLL), acting on the positive sequence of the grid voltage, $\mathbf{v}_o^+$, is used to estimate the grid frequency ω_{PLL}. The output of the PLL is only used to implement the inertial damping according to the scheme of Fig. 2, while grid synchronitazion is determined by the virtual swing equation. In order to avoid impact from double frequency power oscillations during unbalanced conditions, the VSM swing equation in (2) is implemented by using the average power $\bar{p}_o$ instead of the instantaneous three-phase power p_o as traditionally applied in VSM-based control [6], [13], [22].

The VSM also relies on a quasi-stationary electrical model of a synchronous machine according to [23]. An internal positive sequence voltage, $\hat{v}_e$, is used in series with a virtual ohmic-inductive impedance to represent the behaviour of the machine. The amplitude of the emulated internal voltage is obtained by a reactive power droop as:

$$\hat{v}_e = \hat{v}_e^* + k_q\left(q^* - \bar{q}_o\right) \tag{3}$$

where q^* is the reactive power reference, k_q is the droop coefficient and $\hat{v}_e^*$ is the reference of the internal voltage. In order to limit the reactive power flow during voltage sags, $\hat{v}_e$ is limited to be within ± 0.05 pu of the measured positive sequence voltage, so that $0.95|\mathbf{v}_o^+| < \hat{v}_e < 1.05|\mathbf{v}_o^+|$.

The positive sequence current reference component can then be calculated by the quasi-stationary model of the SM as:

$$\mathbf{i}_o^+ = \frac{\hat{v}_e - \mathbf{v}_o^+}{r_v^+ + j\omega_{VSM} l_v^+} \tag{4}$$

where r_v^+, l_v^+ are the corresponding positive sequence per unit virtual resistance and inductance.

C. *Control of the negative sequence currents*

In a Synchronous Machine (SM) the negative sequence currents will result from the voltage unbalance and the equivalent negative sequence impedance. However, for a VSM it could be convenient to apply the inertia SM emulation only for the positive sequence components. It is then possible to control the negative sequence currents to achieve an additional objective. In this paper, the negative sequence currents are controlled to avoid power oscillations in the converter.

The motivation for the approach presented in the following is that any active power oscillations of a converter during unbalanced conditions will propagate to its dc-side. Thus, the power oscillations will give rise to voltage fluctuations on the dc-side, depending on the the dc capacitance of the VSC. To mitigate the impact of dc voltage oscillations or to allow for operation with small dc-side capacitor, it will be necessary to suppress the double frequency oscillations of the active power flow to zero by injecting proper negative sequence currents.

In order to eliminate the active power oscillations in the ac-side grid interfact of the converter, it is possible to calculate the negative sequence current references as a function of the voltages and the positive sequence currents resulting from (4). As reported in [18], the negative sequence current references to achieve a constant active power flow (CAP) are:

$$\mathbf{i}_{CAP}^{-*}=\begin{bmatrix} i_{cv,d}^{-,*} \\ i_{cv,q}^{-,*} \end{bmatrix}=\frac{-1}{\left(v_{o,d}^{+}\right)^{2}+\left(v_{o,q}^{+}\right)^{2}}\cdot \begin{bmatrix} v_{o,d}^{+}v_{o,d}^{-}-v_{o,q}^{+}v_{o,q}^{-} & v_{o,q}^{+}v_{o,d}^{-}+v_{o,d}^{+}v_{o,q}^{-} \\ v_{o,q}^{+}v_{o,d}^{-}+v_{o,d}^{+}v_{o,q}^{-} & v_{o,q}^{+}v_{o,q}^{-}-v_{o,d}^{+}v_{o,d}^{-} \end{bmatrix}\cdot\begin{bmatrix} i_{cv,d}^{+,*} \\ i_{cv,q}^{+.*} \end{bmatrix} \qquad (5)$$

Controlling the currents according to (5) will eliminate the power oscillations at the node where $\boldsymbol{v}_o$ is measured, which in in Fig. 1 is at the filter capacitors C_f. As a consequence, the CAP algorithm from [18], as well as the methods from [12]-[16], will suppress the double frequency power oscillations at the grid-side of the filter inductor.

In order to eliminate the voltage fluctuations on the dc-side of the converter, the voltages and currents used for calculating the negative sequence current references must be obtained at the converter terminals (i.e. before the inductive filter). While the current is easily available, the switched output voltage cannot be easily obtained by measurements. For this reason, it is proposed in this paper to use the modulation signal $\boldsymbol{m}$, as generated by the PR current controller (see Fig. 1), and the the measured dc voltage to estimate the converter output voltage (i.e. $\check{\mathbf{v}}_{\mathrm{cv}} = \mathbf{m}\cdot v_{dc}$). This estimated voltage can then be used for calculating the negative sequence current references. However, the positive and negative sequence components of the estimated converter output voltage $\check{\mathbf{v}}_{\mathrm{cv}}$ must first be obtained by the DSOGI-QSG-based sequence separation. Introducing this approach into (5) provides a simple way of eliminating power oscillations flowing through the converter and thereby to avoid double frequency oscillations in the dc voltage. This proposed approach is the main contribution of the paper and is referred to in the following as Constant dc Power (CDCP) control.

III. SIMULATION RESULTS

The parameters of the system studied by simulations in Matlab/Simulink are summarized in TABLE I. In order to verify both the steady state and the dynamic performances of the proposed algorithm, an unbalanced voltage sag is applied at time t = 0.02 s while the converter is at steady state, injecting 30 kW active power to the grid. The unbalanced voltage sag is simulated by reducing the positive sequence voltage to 0.8 pu while applying a negative sequence component of 0.2 pu.

TABLE I. PARAMETERS OF THE STUDIED SYSTEM CONFIGURATION

Parameter	**Value**	**Parameter**	**Value**
AC Voltage $V_{ll,g,n}$	400 V	Rated current	72 A
Rated angular frequency ω_n	2π·50 Hz	Primary filter inductance l_f , r_{lf}	0.1pu, 0.008pu
DC voltage V_{dcn}	686 V	Filter capacitance c_f	0.079 pu
Active damping k_{SOGI}, k_{AD}	√2 0.5 pu	Grid-side filter inductance l_g, r_g	0.2pu, 0.01pu
Current controller gains, kpc,kic	1.2 0.8	DSOGI-QSGs for sequence separation k_{SOGI}	√2
VSM Positive Seq. I mpedance, r_v^+, l_v^+	0.01 pu 0.2 pu	PLL PI controller, $k_{p,PLL}$, $k_{i,PLL}$	2, 70
Virtual inertia Ta	10 s	VSM damping k_d	200 pu
Frequency droop k_ω	20 pu	Reactive power droop k_q	0 pu

A. *Response of the system to unbalanced voltage sag*

The steady state response of the system to the unbalanced voltage sag is shown in Fig. 4. The results in the left column refers to operation with Balanced Positive Sequence Currents (BPSC) [18], while the results in the center and right columns refer to the CAP and CDCP algorithms respectively. In the first row the unbalanced voltages are depicted and they are the same for the three cases. In the second row, the currents injected into the grid are shown. As expected, the BPSC algorithm injects symmetric currents even under unbalanced grid voltages. On the contrary, the other two strategies inject unbalanced currents to avoid active power oscillations by injecting higher current in the phase with lower voltage and vice versa. In the third row, the active powers are represented. In particular, three powers are shown for each case: i) the power P_{out} exchanged with the grid, which depends on the measured voltage $\boldsymbol{v}_o$ and the grid-side current $\boldsymbol{i}_o$, ii) the power flowing out of the filter inductor, P_L, depending on the measured voltage $\boldsymbol{v}_o$ at the filter capacitors and the inductor current $\boldsymbol{i}_{cv}$, and iii) the power P_{DC} flowing from the dc side of the converter.

The BPSC strategy implies very similar oscillations in the three powers. This is the direct consequence of injecting symmetrical currents when unbalanced voltages are applied. The CAP strategy, as expected, reduces almost to zero the power oscillations P_L at the grid-side of the filter inductor. As a consequence, also the oscillations of the other two powers are quite reduced, but the power at the dc side still presents an undesired oscillation. This is mainly due to the power oscillations caused by unbalanced currents flowing in the filter inductor, which are not considered by the CAP algorithm.

Finally, the CDCP algorithm reduces almost to zero the power oscillation at the dc-side of the VSC. This implies a larger oscillation in the power at the grid side of the filter inductor, but this does not imply any disadvantage in normal installations. It is worth noting that the oscillation of the power exchanged with the grid using the CDCP is actually lower than what results form the CAP strategy. This can be explained by considering that the power oscillations in the filter inductors will be almost in opposite phase with respect to the power oscillations in the filter capacitors, which leads to a partial compensation of the oscillations in the output power. This could be an additional advantage achieved by the proposed control algorithm. Indeed, the proposed control strategy (i.e. the CDCP) is capable of reducing the dc side power oscillation and, at the same time, reduces the output power oscillation if compared with the traditional CAP strategy. From an implementation point of view, the CDPC does not need any additional measurement and is not more complex than the CAP strategy. For this reason, the obtained advantages are achieved without any adverse effect.

B. *Dynamic response of the system*

When an unbalanced voltage sag occurs, a transient response of the VSM-based control system implies a transient in the power exchanged with the grid. The dc-side power obtained with the CAP and the CDCP strategies are reported in Fig. 5. Looking at the figure, it is clear that the dynamic behaviour of the VSM obtained with the proposed CDCP strategy is the same as obtained by the traditional CAP.

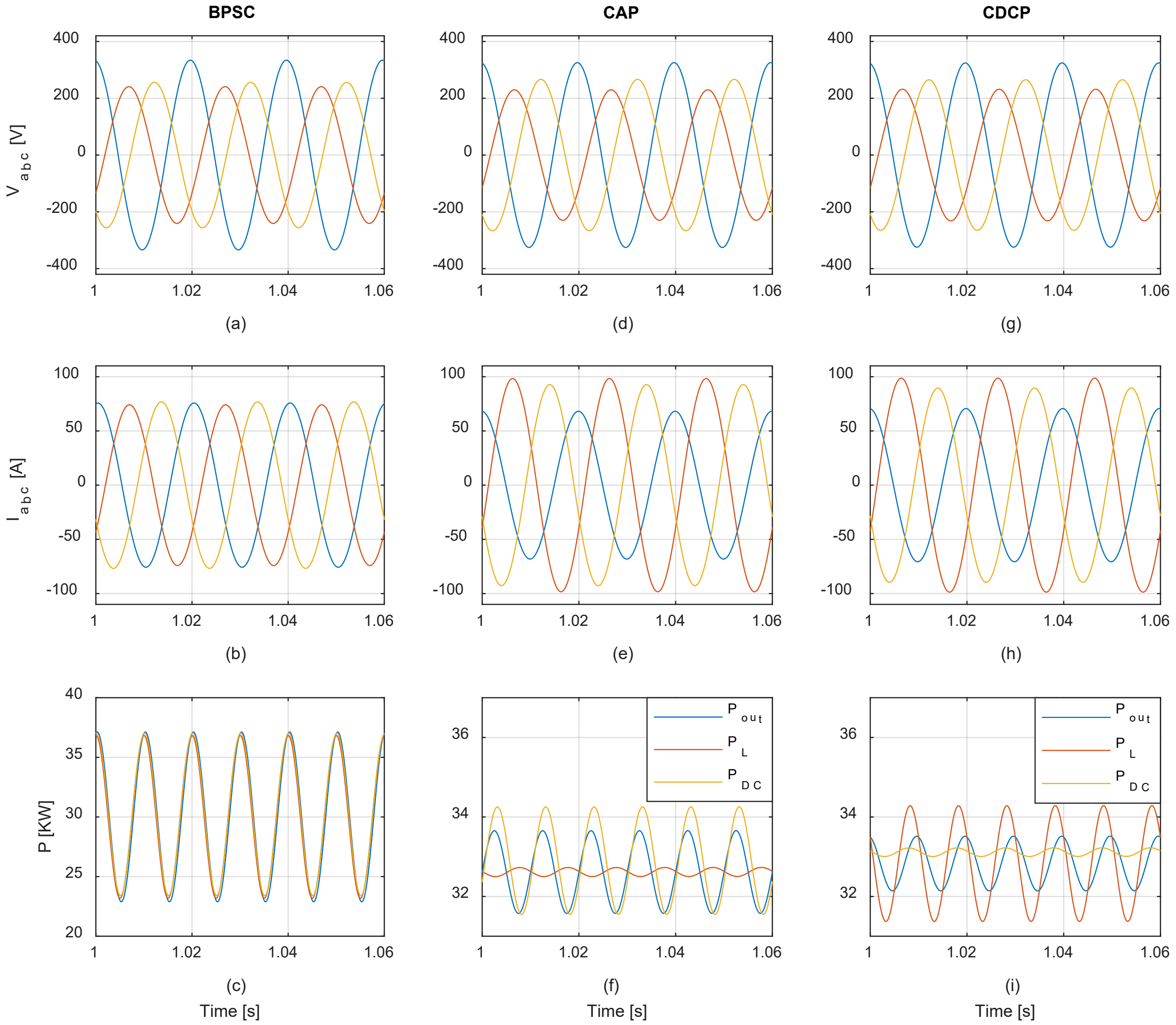


Fig. 4 Simulation results in grid-connected mode showing the steady state response to an unbalanced voltage sag occurring at t=0.02, resulting in a grid voltage with 25% unbalance ($|V^-|/|V^+| = 0.2/0.8=0.25$).

Nevertheless, elimination of the power oscillations on the dc side is achieved also during the transient. In order to better verify that the proposed control strategy does not affect the dynamic behaviour of the VSM, an additional simulation is performed by applying a step in the active power reference at time t = 0.05 s. The average generated power and the virtual speed of the VSM obtained with the two algoritms are reported in Fig. 6. From the comparison shown in the figure, it is highlighted that the two control strategies dynamically perform in the same way in the emulation of the SM inertial dynamics. Therefore, the advantages achieved at steady state do not imply any drawback during the transient response.

IV. Conclusions

Virtual synchronous machines (VSM) can provide virtual inertia to power systems and inherently introduces grid forming capabilities by mimicking the behaviour of synchronous machines. This behaviour can be preserved also in case of unbalanced ac grid voltage conditions, but unbalanced operation can result in double frequency oscillations in the power flow and in the dc-side capacitor voltage. Such voltage oscillations could be undesirable in several applications. In this paper, a VSM implementation specifically designed for avoiding dc-side voltage oscillations during operation in unbalanced grid voltage conditions is presented. The positive sequence current references are determined by a virtual impedance and the emulated swing equation, as in common VSM implementaitons for balanced conditions. However, the negative sequence currents are controlled to eliminate the double frequency power oscillations due to the unbalanced voltage. Specifically, the calculation of the negative sequence current references is based on the modulation signals of the converter rather than on ac voltage measurements as in previous VSM-based control schemes for unbalanced conditions. This ensures elimination of double frequency oscillations in the power flow through the converter by inherently avoiding remaining power oscillations resulting from the unbalanced currents flowing in the filter inductors. The intended operation of the proposed control system implementation and the improved performance compared to schemes based on voltage measurements at the filter capacitors has been demonstrated by time-domain simulations.

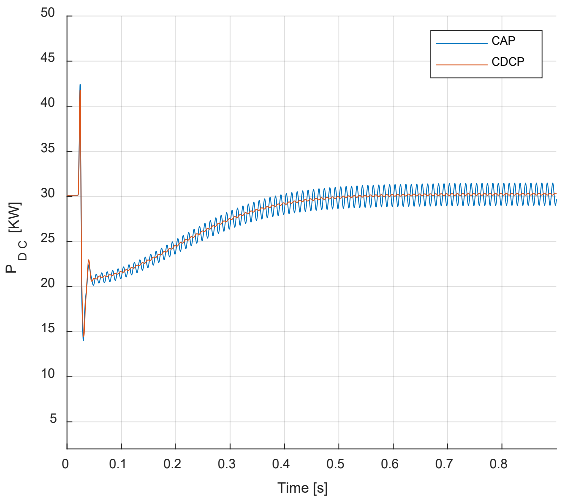


Fig. 5 Comparison of the control strategies effect on the dc power under unbalanced ac voltage conditions

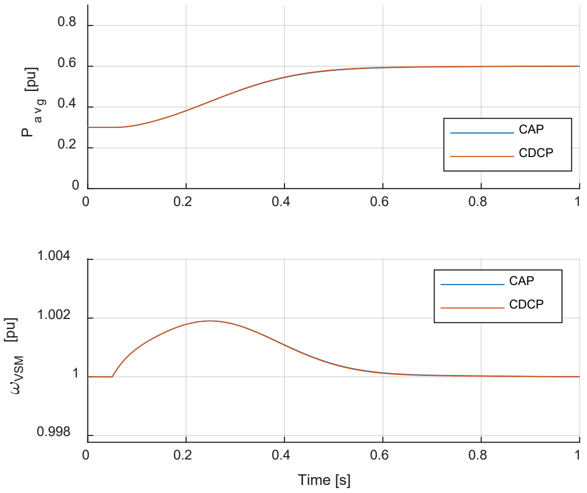


Fig. 6 Comparison of the inertial response with a step in the active power reference at time t=0.05

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