Windowed PWM: A Configurable Modulation Scheme for Modular Multilevel Converter-Based Traction Drives

Davide De Simone, Luigi Piegari, *Senior Member, IEEE*, Pietro Tricoli, *Member, IEEE*, and Salvatore D'Arco

***Abstract*—This article introduces a modulation technique for modular multilevel converter (MMC) in variable speed traction drives for electrical transportation referred as windowed pulsewidth modulation (W-PWM). The windowed PWM (W-PWM) is derived by blending the principles of operation of conventional modulation schemes for MMC based on the nearest level control (NLC) and on PWM with the aim of combining their inherent strengths and offering a higher degree of flexibility. This can reduce switching losses compared to classical PWM schemes and lower the current harmonic distortion compared to NLC schemes. The window in which the PWM is applied can be seen as an additional degree of freedom that allows a dynamic optimization of the performance of the traction drive depending on its operating characteristics. The performance of the W-PWM technique is assessed in this article for several operating conditions and compared with conventional schemes based on NLC and on the phase opposition disposition PWM with both numerical simulation and experimental verification on a small-scale prototype. Results demonstrate the flexibility of the W-PWM and its potential for applications in electrical traction drives.**

***Index Terms*—AC motor drives, traction motor drives, power converter, road vehicle electric propulsion, pulsewidth-modulated power converters.**

I. Introduction

IN THE last few decades, private transport has become one of the main source of pollutants and it is now clear that the technical improvements on conventional internal combustion engines (ICE) will not be sufficient to reduce the global CO2 emissions. Battery electric vehicles (BEVs) are a valid alternative to ICE vehicles and although the sales are now accelerating, battery electric vehicles (BEVs) still represent only 1% of the consumer market. Main factors slowing the penetration of BEV are arguably the perceived limitations of the technology as the limited vehicle range and the long battery recharge time [1].

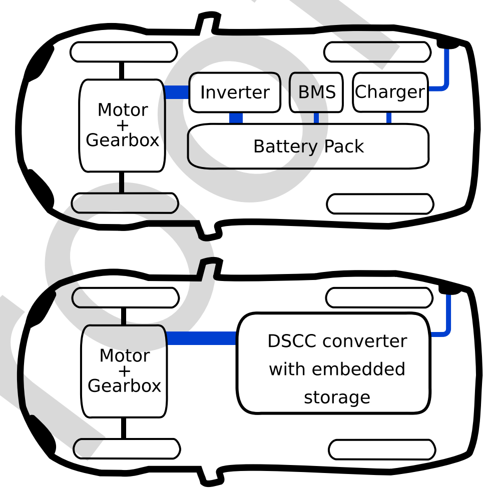

Fig. 1. Typical BEV powertrain.

A typical power train of a BEV includes several power converters, as represented in Fig. 1. The battery pack is composed by connecting in series a large number of low voltage cells [2]. Due to unavoidable differences between the cells, a battery management system is required to ensure that each individual cell remains within its voltage limits [3]. The traction inverter is responsible to supply and control the motor, while a separate on-board battery charger could be added to charge the battery pack from the utility grid. In many vehicles, the on-board battery charger has a low power rating, typically up to 7 kW, leading to long charging times when an external dc rapid charger is not available.

In [4], D'Arco *et al.* proposed a configuration for BEVs based on a double star chopper cell (DSCC) converter, belonging to the family of modular multilevel converter (MMC). This DSCC-based configuration embeds in a single converter the functions of the traction inverter [5], the battery management system (BMS) [6], [7], and the battery charger [8]. Multilevel topologies as the cascaded H-bridge (CHB), the single-star bridge-cell (SSBC), and the single-delta bridge-cell (SDBC) topologies also can control the power supplied by the individual battery modules, thereby allowing the integration of both traction drive and BMS functionalities. However, the DSCC offers more flexibility than

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CHB, SSBC, and SDBC configurations, as the direct, inverse, and zero sequence of the circulating currents can be used for cell balancing. Additionally, the DSCC can be connected to an external dc source for charging the batteries as an alternative to ac charging. For this reason, in this article, the DSCC will be addressed.

Using the same converter for different tasks leads to a higher global efficiency in comparison with standard two-level inverters [9] with consequent more range of the BEV. This is also supported by the fact that balancing is achieved using the load current rather than transferring energy between the cells. The single converter does not influence negatively the reliability of the system since, as demonstrated in [10], the proposed topology presents a high redundancy. As DSCCs can handle the rated power also for charging operations, rapid charging is allowed without the need of extra hardware on-board.

The efficiency of motor drives with DSCCs could be further increased by adopting new modulation strategies with lower switching losses. However, any modulation strategy has to consider the impact on the total harmonic distortion (THD) of the current, as harmonics increase the losses of the motor and generate torque ripples that lead to mechanical vibrations and faster wear of the transmission. In the automotive industry, the drive system efficiency and the injected THD are a major concern since it might affect the lifespan of insulation systems [11] and the general driving performance. As harmonics depend on load parameters and, hence, are not constant for all the operating conditions, the comparison between different modulation techniques is usually based on the voltage weighted total harmonic distortion (WTHD).

Two main families of MMC modulation techniques can be identified in the technical literature: modulation schemes based on nearest level control (NLC) [12], [13] and schemes based on pulsewidth modulation (PWM) [14]–[16]. NLC techniques present the lowest switching losses but relatively high WTHD of the phase voltage and motor losses, whereas PWM has opposite characteristics. In this article, the authors propose a modulation technique called windowed-PWM (W-PWM) that applies PWM only at specific angular intervals of the reference waveform to achieve the optimal compromise between power losses and WTHD. Therefore, the angles in which PWM is applied can be controlled dynamically and continuously and adapted to the different operating conditions of the traction drive. Even if not explicitly addressed in this article, the proposed technique can be also easily extended to any electrical drives with multilevel converters and especially medium voltage drives for which switching losses are particularly critical.

The article is organized as follows. Section II summarizes the application of the DSCC topology for traction drives. Section III reviews the state of the art of modulation techniques and control strategies for multilevel inverters. The W-PWM and its main characteristics are described in Section IV. A detailed description of the simulation and test rig is given in Section V. Section VI shows the main numerical and experimental results. Section VIII summarizes the main outcomes and draws the conclusion of this article.

II. Reference System Configuration

The reference system configuration assumed for this article is a traction drive composed by an induction machine connected to

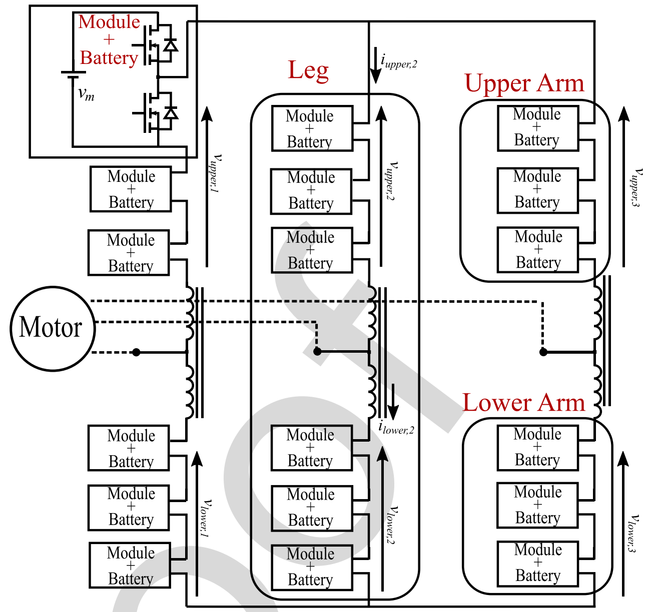

Fig. 2. Double star chopped cell converter topology.

a DSCC converter embedding an energy storage cell with voltage v_m in each module as represented in Fig. 2. As in standard MMCs, the arm inductors can be mutually coupled to reduce the weight of the converter and to reduce the output voltage drop. To generate the output phase voltage, the following voltage references are sent to the upper and lower arm of each phase

$$\begin{cases} v_{\text{lower},k} = \frac{v_{\text{dc,bus}}}{2} + v_{\text{phase},k} + v_{k,\text{circ}} \\ v_{\text{upper},k} = \frac{v_{\text{dc,bus}}}{2} - v_{\text{phase},k} + v_{k,\text{circ}} \end{cases} \tag{1}$$

where $v_{\text{dc,bus}}$ is the dc bus voltage, $v_{\text{phase},k}$ is the phase voltage reference of a generic converter leg "k" [17], and $v_{k,\text{circ}}$ is the cell balancing control voltage referred to the same converter leg [4], [18]. From upper and lower arm voltages (1), the expression of the output phase voltage $v_{\text{phase},k}$ is obtained as

$$v_{\text{phase},k} = \frac{1}{2}\left[v_{\text{lower},k} - v_{\text{upper},k}\right]. \tag{2}$$

If the per unit impedance of the leg inductors is low and/or if the output frequency is low, $v_{\text{upper},k}$ and $v_{\text{lower},k}$ must be generated so that the total number of inserted modules is equal across the three converter legs. If this condition is not met, the difference between the instantaneous voltage of the legs give rise to circulating currents.

DSCCs can use circulating currents between legs acting on $v_{k,\text{circ}}$ of (1) to exchange energy between battery cells, acting effectively as a BMS. The energy stored in a battery can be quantified by the state of charge (SOC), which is the ratio between the available energy and the total battery capacity. Since the estimation of the SOC is not the main focus of this article, a simple Coulomb-counting method was considered for sake of simplicity [10]

$$\text{SOC}_h(t) = \text{SOC}_h(t_0) - \frac{1}{3600 \cdot Q_{\max}}\left(\int_{t_0}^{t} i_h(t)dt\right) \tag{3}$$

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with $\mathrm{SOC}_h(t_0)$ the hth cell SOC at initial time, and $Q_{\max}$ the total module battery capacity in Ah. Moreover, $i_h(t)$ is the battery current, which was estimated knowing the current flowing in the arm in which the module is installed and the conduction state (ON or OFF) of the module itself. A positive current discharges the battery reducing its SOC.

The balancing process is achieved through three control loops [19], namely leg balancing, arm balancing, and module balancing. The leg balancing algorithm operates on the dc voltage reference of each leg to impose a dc circulating current. This current transfers energy between the phases of the converter so that the average SOC is the same for all the phases. The arm balancing algorithm balances the average SOCs of the upper and lower arms of each phase. The exchange of energy within the arms of the same leg is achieved by imposing a negative and positive sequence current synchronized with the output phase voltage [18]. The circulating currents cannot be accurately controlled with an NLC modulation technique in converters with a limited number of modules or at low frequency. This could lead to high circulating currents and risks of damaging the converter. Therefore, if cells belonging to different legs and phases are strongly unbalanced, a PWM modulation technique is necessary. Once the balancing is completed, NLC or W-PWM modulation techniques can be applied.

The module balance algorithm equalizes the SOC of all the cells included in each arm. This is achieved by controlling the modules to activate using a sorting algorithm: if the current charges the cells of the arm, the modules with the lowest SOC are turned ON first; if, instead, the current discharges the cells, the modules with the higher SOC are used first.

When used as battery chargers, DSCC converters can be connected to either single-phase, three-phase, and dc power sources with no modification of the hardware and, therefore, they are a versatile choice for automotive applications. As DSCCs have typically a high number of voltage levels, they can be connected to the power source with no or very small filters, reducing the curb weight of the BEVs on which they are installed.

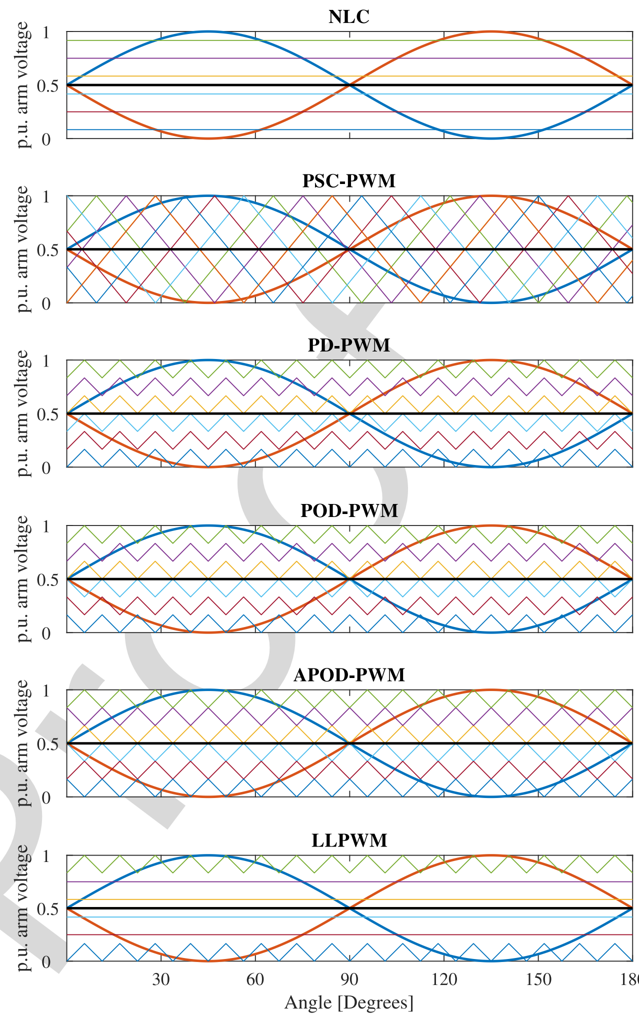

Fig. 3. Carrier and arm references of different modulation techniques.

III. DSCCs Modulation Techniques

This section reviews the most widely used modulation techniques for DSCCs [10], [14], i.e., the NLC, the carrier phase shifted PWM, the phase disposition PWM (PD-PWM), the phase opposition disposition PWM (POD-PWM), the alternate phase opposition disposition PWM (APOD-PWM) and the last level PWM (LLPWM), which are shown in a qualitative way in Fig. 3 in the case of four modules per arm converter.

A. Nearest Level Control

In the NLC modulation technique, the modules are activated or deactivated to minimize the error $e_v = v^*_{\mathrm{phase},k} - v_{\mathrm{phase},k}$, where $v^*_{\mathrm{phase},k}$ represents the reference of the phase k output voltage, and $v_{\mathrm{phase},k}$ represents the actual phase k voltage. When the error is above a specified threshold, the related module is activated [12]. In accordance with [13], the NLC algorithm has been implemented considering the mean voltage of the modules

$$v_{th}(n) = (n-1)\cdot \overline{V}_m + \frac{1}{2}\overline{V}_m \tag{4}$$

where $v_{th}(n)$ is the threshold voltage of the nth module and $\overline{V}_m$ is the module mean voltage.

B. Phase Shifted Carrier Pulsewidth Modulation

This modulation technique is the extension of the traditional sinusoidal PWM strategy to multilevel converters [20], [15], [21], [22]. If the converter has N modules per arm, the output voltage is generated by comparing $2\cdot N$ equally shifted triangle carrier signals with the arms modulation signals. With this modulation technique, all the modules are switched in each carrier period, removing the need of the inner arms balancing algorithm (see Section II) and, hence, simplifying the control of the converter. The generated output phase voltages are characterized by $N+1$ levels. In this modulation, the carrier frequency applied to the modules f_{carrier} is N times smaller than the desired output switching frequency f_{sw}: $f_{\mathrm{carrier}} = \frac{f_{\mathrm{sw}}}{N}$. Thus, each module is subjected to lower frequency harmonics.

C. Phase Disposition Pulsewidth Modulation

In this modulation technique, an individual carrier signal with amplitude equal to the module voltage is assigned to each

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module [20], [23], [21]. The offset given by (4) is added to each carrier. The carrier signals are shifted by the module sorting algorithm. For example, if the current is charging, the modules with the lower SOC are shifted at the bottom to keep them turned ON for the maximum possible time. The total number of active modules for each leg differs by ± 1 module. This leads to $2 \cdot N + 1$ levels on the output phase voltage, but also introduces additional voltage ripple across the arm inductors with consequent increase of the circulating currents.

D. Phase Opposition Disposition Pulsewidth Modulation

This modulation technique is based upon the same principles of PD-PWM, with the difference that the carriers of the upper arm are delayed by half a period of those of the lower arm [20], [21], [23]. With this modification, the total number of active modules per leg is always the same, independently on the modulation index, thus, the internal circulating currents are minimized. The output phase voltage is obtained changing the distribution of active modules between the upper and the lower arms within a converter leg. This modulation strategy generates an output phase voltage with $N + 1$ levels.

E. Alternate Phase Opposition Disposition Pulsewidth Modulation

The APOD-PWM is based upon the same principle of POD-PWM, but the carrier signals of odd modules have a $180°$ shift in respect to the even modules [21], [23]. In the POD-PWM, this modulation technique generates $N + 1$ levels and presents no theoretical voltage ripples across the dc bus.

F. Last Level Pulsewidth Modulation

LLPWM is a hybrid NLC-PWM modulation strategy proposed in [24]. LLPWM generally activates the components of the converter using NLC. At each module activation, the controller checks the peak value of the reference, if the module in activation will be the last one (top and bottom point of the reference) PWM will be applied on that particular module.

IV. Windowed Pulsewidth Modulation

The W-PWM applies PWM around the peak value of the sinusoidal reference signals to reduce the harmonic distortion of the generated voltages. For operations with variable voltage amplitude and frequency like EV applications, it is necessary to identify the correct position of the peak values, as the signals are not strictly sinusoidal. To do so, the modulation is switched between NLC and POD-PWM in relation of the phase angle of the reference space vector. By choosing appropriate space vector phase intervals, NLC can be applied to the steepest areas of the output waveforms while PWM can be applied where the derivative of the reference is relatively small. W-PWM carrier signals are generated following (5), $x(t)$ represents a triangle wave with average value of zero and peak values of ± 1, u represents the control variable that turns ON and OFF the PWM signal and V_i is the nth module voltage

$$v_{th}(n,t) = \sum_{i=1}^{n-1} V_i + (1 + u \cdot x(t)) \cdot \frac{1}{2} V_n. \quad (5)$$

TABLE I
W-PWM Activation Angles as Function of ϕ = Window, θ = Space Vector Angle

Phase		
A	$-\frac{\phi}{2} \leq \theta \leq \frac{\phi}{2}$	$\pi + \frac{\phi}{2} \leq \theta \leq \pi - \frac{\phi}{2}$
B	$\frac{2}{3}\pi + \frac{\phi}{2} \leq \theta \leq \frac{2}{3}\pi - \frac{\phi}{2}$	$\frac{5}{3}\pi + \frac{\phi}{2} \leq \theta \leq \frac{5}{3}\pi - \frac{\phi}{2}$
C	$\frac{4}{3}\pi + \frac{\phi}{2} \leq \theta \leq \frac{4}{3}\pi - \frac{\phi}{2}$	$\frac{\pi}{3} + \frac{\phi}{2} \leq \theta \leq \frac{\pi}{3} - \frac{\phi}{2}$

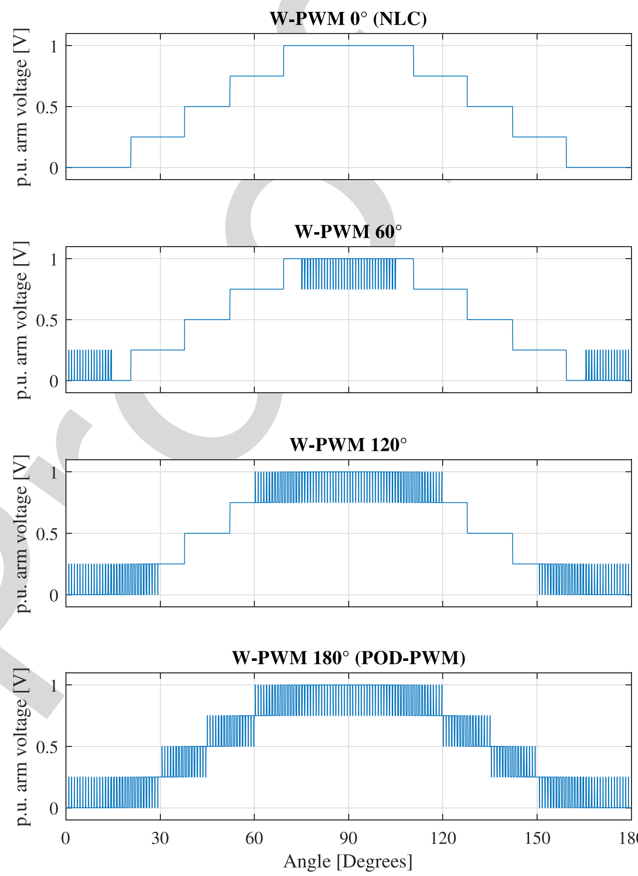

Fig. 4. Qualitative W-PWM arm voltages at NLC, W-PWM 60°, 120° and POD-PWM.

Starting from a three-phase voltage reference, the related space vector is calculated according to

$$\overline{v^*} = \frac{2}{3}\left[v_a^*(t) + v_b^*(t) \cdot e^{j\frac{2}{3}\pi} + v_c^*(t) \cdot e^{j\frac{4}{3}\pi}\right] \quad (6)$$

where $v_a^*(t)$, $v_b^*(t)$, and $v_c^*(t)$ are the three-phase output voltage references. The phase of the space vector is, then, compared with the intervals of Table I. In each period of the waveform, there are two PWM intervals, around the positive and the negative peaks, respectively. If the phase does not fall within one of the two intervals, the control variable u is set to zero, thus the carrier signal is replaced by its average value and the W-PWM reduces to the NLC modulation. On the contrary, if the phase of the space vector falls in one of the two intervals, u is set to one enabling the PWM.

Fig. 4 shows the output converter arm voltages with different W-PWM windows sizes.

The W-PWM enables a precise control of the PWM window and the length of this window is effectively a new degree of

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TABLE II
TESTED MMC MAIN PARAMETERS

Parameter	Value
Modules per arm	4
Module Battery	PL-9759156-5C
Mosfet Switches	IRF1324S-7PPbF
Arm Inductance	22 μH
Arm resistance	30 $m\Omega$

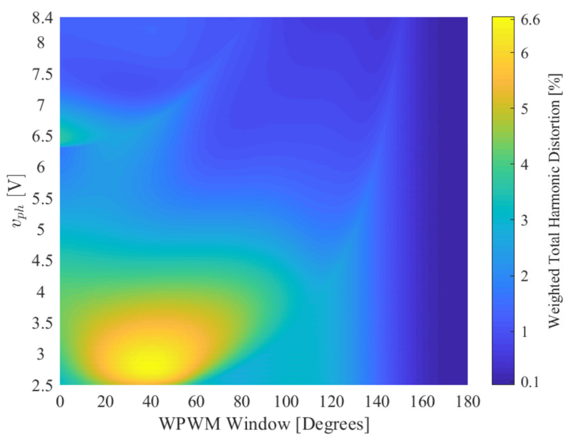

Fig. 5. WTHD as a function of output voltage and W-PWM window of a generic four modules per arm MMC.

freedom for the control system. It is worth noting that for certain values of ϕ that depends on the number of modules of the converter and on the magnitude of the voltage reference, W-PWM reduces to LLPWM modulation [24].

V. Simulation and Experimental Set-Up

To study the W-PWM characteristics, a Simulink model has been developed to obtain a relation between the harmonic distortion, quantified with the WTHD of the output voltage, the amplitude of the output voltage, the output frequency, and the PWM window size. The WTHD has been calculated in accordance with [25] as

$$\mathrm{WTHD} = \frac{1}{V_1}\left[\sum_{n=2,3..}^{\infty}\left(\frac{V_n}{n}\right)^2\right]^{1/2} \tag{7}$$

where V_1 is the amplitude of the first harmonic, V_n is the amplitude of the *n*th harmonic, and *n* is the harmonic order.

A switching model with the same characteristics of the small scale prototype whose main components are summarized in Table II has been used. Conduction losses were considered using the Simscape library blocks and matching switches and inductances parameters with the ones of the prototype. To estimate switching losses, the current and the voltages across each solid state switch were measured. Every time a change in the control signal is experienced, the procedures described in [26] were used to calculate the switching losses.

In Fig. 5, the variation of the output voltage WTHD as a function of the reference voltage amplitude and the PWM window angle is illustrated. The results have been obtained by means of several simulations using a V/Hz constant control law with base speed reached at 50 Hz and 8.4 V. It is worth noting that, when the output voltage reference is below 0.25 p.u. (2.1 V), NLC does not generate any signal and, hence, the WTHD of the waveform cannot be calculated. Moreover, the WTHD for NLC changes from 12.8% to 3.34% when the reference voltage increases from 2.2 to 2.5 V. However, for a clearer data representation, the v_{ph} axis of Fig. 5 starts from 2.5 V since the color mapping would become too flat in the zone of more interest if the minimum voltage is set to lower values (e.g., 2.1 V).

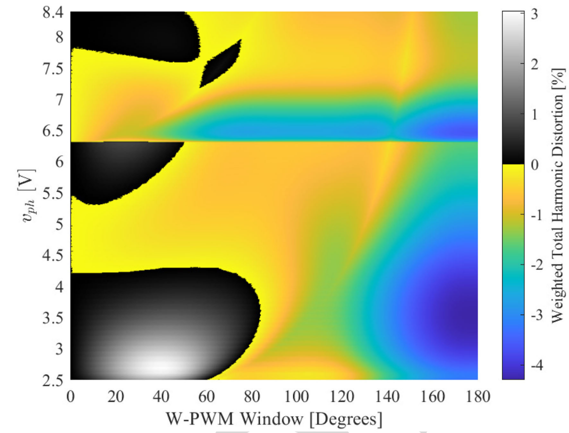

Fig. 6. Difference between the $\mathrm{WTHD_{w\text{-}pwm}}$ and the $\mathrm{WTHD_{NLC}}$ for a four modules per arm MMC.

In order to better visualize which PWM windows improve the WTHD with respect to the NLC at each output voltage/frequency, the difference between the WTHD for the W-PWM and the NLC is shown in Fig. 6. All the negative results are represented with a color gradient where the lowest values are blue and the highest values are yellow. The more negative is the differential WTHD, the more the selected window is improving the WTHD with respect to NLC. All the positive differences instead are represented with a gray scale; those values imply that the introduction of W-PWM with the corresponding window leads to a worse WTHD.

From the analysis of Fig. 6, it is possible to determine that 84° is the smallest window ensuring a WTHD lower than NLC for every value of the desired output voltage. Since the results obtained by simulation (Figs. 5 and 6) could not be obtained experimentally with the same detail level, the aim of the comparison between simulation and experimental results is to validate the simulation results measuring the converter performance in a reduced set of operating regions.

The experimental tests have been carried out on a DSCC prototype with four modules per arm, each one including a 4.2 V 10 Ah LiPo battery, as shown in Fig. 7. The main converter parameters are summarized in Table II. The controller has been implemented on a NI CompactRio FPGA system. From (2), it is possible to state that the maximum phase voltage is one half of the maximum arm voltage, thus, the maximum output voltage is 8.4 V with this configuration. The converter is connected to a variable load consisting of a 12–400 V step-up transformer, a variac, and a resistive load, as reported in Fig. 8. In the laboratory configuration, low voltage battery cells and a transformer have been used both due hardware availability and safety reasons even though higher voltage battery modules would be preferable in a real application. With this set-up, it is possible to regulate the

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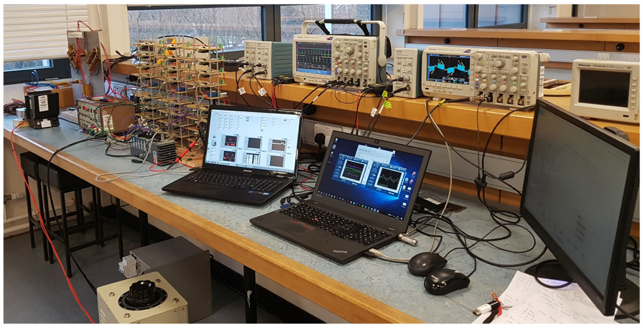

Fig. 7. Experimental set-up.

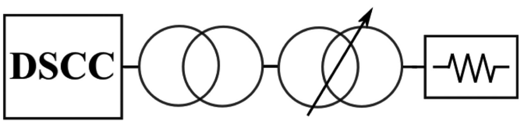

Fig. 8. Schematic overview of the test setup.

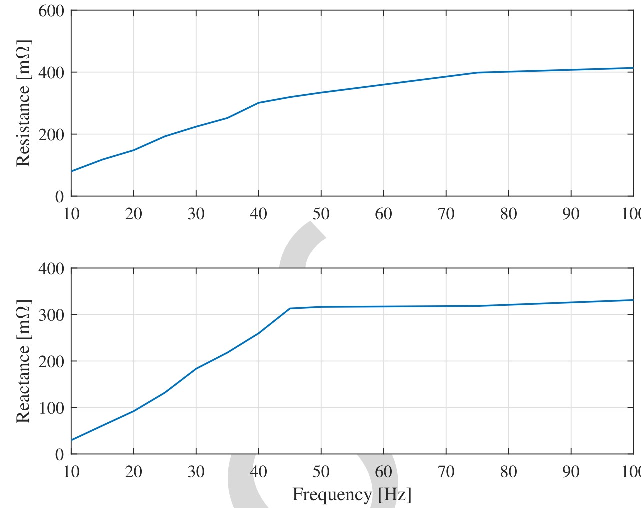

Fig. 9. Load resistance (top) and reactance (bottom) measured with POD-PWM.

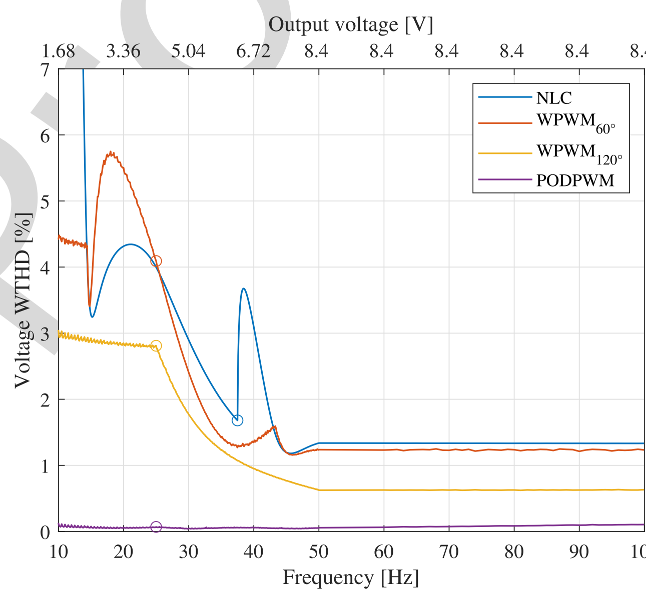

Fig. 10. Simulated output voltage WTHD when controlled with a V/Hz constant strategy. Circles identifies points in which a new module is added to generate the output.

output current while changing the converter output voltage and frequency.

The efficiency of the converter has been estimated by extrapolating the measurement from a single module, as the average power losses are the same if the cells are well balanced.

VI. Numerical and Experimental Results on a Down-Scaled System

The proposed W-PWM has been compared with NLC and POD-PWM in terms of output harmonic distortion and converter efficiency. The simulation and experimental tests have been undertaken with a load drawing 10 A rms and using a V/Hz constant law in the range 0 to–Hz (0 to 8.4 V) and a constant voltage over 50 Hz. The Simulink model used to perform the simulations reported in this chapter is a detailed reproduction of the converter described in Section V.

Simulation results are, then, compared with experimental data to ensure that the detailed behavior in terms of WTHD reported in Fig. 6. In theory, the test rig in Fig. 7 should change only the equivalent resistance seen by the converter. In practice, also the load inductance is affected by the nonlinearity of the two transformers. Therefore, the equivalent load parameters were estimated from the experimental data and, then, used in the detailed simulation. The estimation of the load parameters was obtained starting from the first harmonics phasors of the measured voltage and current waveforms. The measured load parameters were independent from the modulation technique, the resultant load parameters obtained from this analysis are summarized in Fig. 9.

A. WTHD Evaluation

The voltage WTHDs are measured for different output voltages. For what concerns W-PWM, window angles multiple of 60° are tested. Fig. 10 compares the voltage WTHD produced by the different W-PWM windows, whereby the values of 0° and 180° are equivalent to NLC and POD-PWM, respectively. As a general rule, the wider the PWM window, the lower the WTHD. For specific values of W-PWM windows, output voltage and output frequency, the harmonic distortion obtained by W-PWM becomes higher than the NLC.

The NLC and the PWM follow a different approach for activating additional cells. The PWM-based techniques activate new modules when reaching a voltage equivalent to an integer number of voltage cells while the NLC activates new modules when passing values in the middle of the voltage cell. This means that a diagram of the number of levels will jump from 1 to 2 at 6.3 V for the NLC while the same happens at 4.2 V for the PWM. As a V per Hz constant control algorithm has been applied, the voltage levels are proportional to the fundamental frequency of the output. Additionally, as the carriers are all the same, the type of PWM technique will not affect where there is the change of number of levels. Changes in the number of active levels are highlighted in Fig. 10 with circles.

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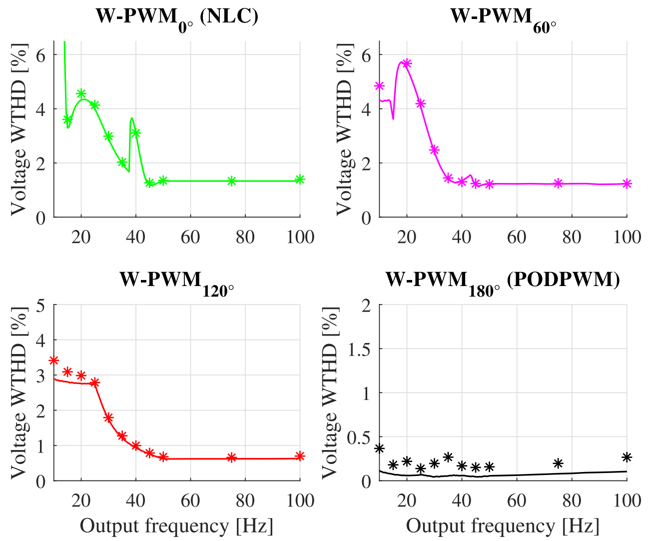

Fig. 11. Simulated (continuous line) versus measured (markers) converter WTHDs when controlled with a V/Hz constant strategy.

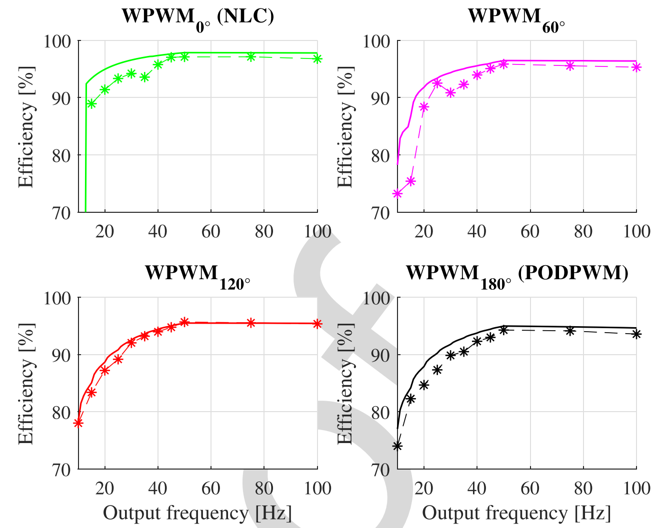

Fig. 13. Simulated (continuous line) versus measured (markers) converter efficiency when controlled with a V/Hz constant strategy.

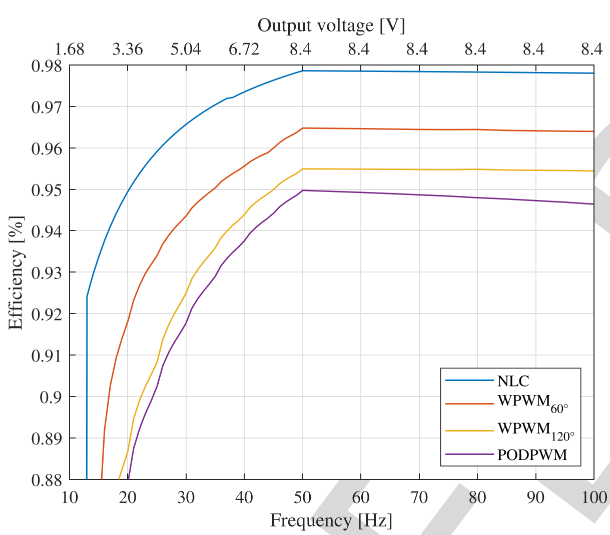

Fig. 12. Simulated converter efficiency when controlled with a V/Hz constant strategy.

The experimental data on the test rig are compared with the simulations in Fig. 11: the peaks of the NLC voltage WTHD due to the activation of a new module can be clearly seen also from the measurements. For the W-PWM at 120° and for the POD-PWM, this is not visible because the angle of PWM is sufficiently large to include the instant when an extra module is activated. Since the converter has four modules per arm, just two modules are triggered over the whole output voltage range. At 20 Hz, 3.36 V (on the first NLC WTHD peak), it is clear that W-PWM windows larger than 60° improve significantly the output WTHD. When a 60° window is considered, a poor performance is experienced, as predicted by the preliminary analysis shown in Fig. 6. At higher frequencies (at converter nominal voltage), W-PWM with 60° gives a very limited WTHD improvement with respect to NLC. W-PWM reduces the output voltage WTHD in a good agreement with the theoretical analysis.

B. Efficiency Evaluation

In the simulations, the converter efficiency was calculated as the ratio between the load power and the total battery injected power over a predefined time period. In the experiments, the efficiency was measured as the ratio of the output and input energy of one module of the converter. To ensure that the data extrapolated from one module represent accurately the global converter efficiency, it is extremely important that each module remained perfectly balanced with the others. Under this condition, all the modules have the same voltage and contribute equally to the generated power. Moreover, if the gate signals are all synchronized, when the cells are balanced there is no net power exchange between the three phases. To ensure this assumption was met, before each test, all the cells were charged an average of 30 min to restore a 100% SOC. Additionally, it is important that the module selected for the measurement was used as much as the others during the observation. To meet this condition, the sorting algorithm that balances the module SOCs [18], [19] was replaced with a function that sets the module priority with a fixed periodic pattern with period 1 s. The logging time interval of the instruments was set accordingly to 1 s.

In V/Hz constant tests, 11 points between the frequency range 10–100 Hz were taken for each investigated W-PWM window. The load current was kept constant at 10 A below 50 Hz. For NLC and some W-PWM windows, 10 A load current was not reachable at low voltage references. In these conditions, the maximum achievable current was set. Due to the approximations introduced to measure the efficiency, the longer are the tests, the higher is the unbalance level between the modules introduced by unavoidable differences among the storage system, leading to less reliable results. From the analysis of Fig. 13 in which experimental and theoretical data are reported on the same diagram, it is reasonable to state that there is a good matching between theoretical and experimental results.

Looking at the NLC curve reported in Fig. 12, the global efficiency is higher than all the other modulation schemes. An efficiency drop can be seen when the second module is turned ON. The phenomenon is related to the increase of the

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TABLE III
INDUCTION MOTOR PARAMETERS

Parameter	Value
Nominal voltage	156 V
Nominal frequency	50 Hz
Number of pole pairs	2
Stator resistance	10 $m\Omega$
Rotor resistance	10 $m\Omega$
Stator leakage inductance	0.2 mH
Rotor leakage inductance	0.2 mH
Magnetizing inductance	5 mH

TABLE IV
FULL-SCALE MMC PARAMETERS

Parameter	Value
Modules per arm	14
Module Voltage	22.2 V
Mosfet Switches	MMIX1T550N055T2
Arm Inductance	22 μH
Arm resistance	3 $m\Omega$

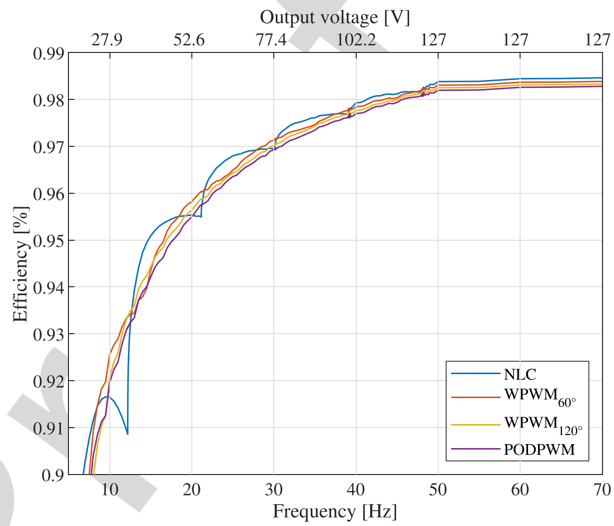

Fig. 14. Simulated full-scale converter efficiency.

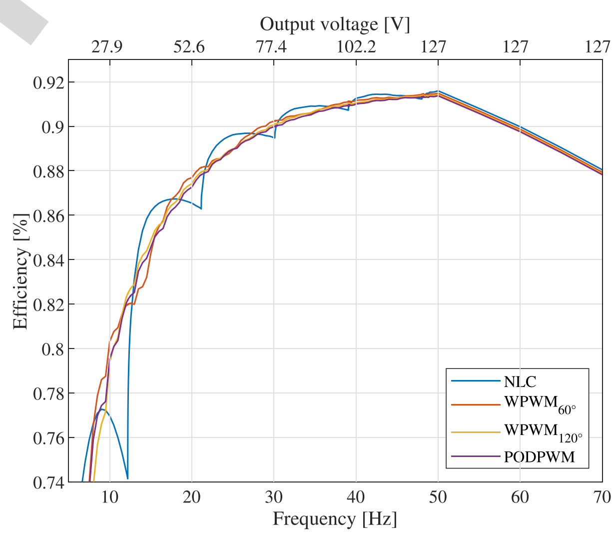

Fig. 15. Simulated full-scale converter and motor efficiency.

harmonic distortion of the load that reduces the active power transferred, and to the short duration of module on-time that increases switching losses without increasing significantly the load active power. The efficiency of the W-PWM is always between the NLC and the POD-PWM. In general, the longer the PWM window, the higher the switching losses and, hence, the lower the efficiency. As expected, the POD-PWM has the lowest efficiency for the highest number of device commutations per period.

It is worth noting that the NLC seems to be always preferable when looking only at the converter efficiency. However, the NLC increases the WTHD resulting in higher harmonics of the motor current and, thus, lower motor efficiency. Therefore, the global efficiency of the drive system is optimized with a combination of NLC and PWM. Moreover, increasing the WTHD could imply additional problems like accelerated ageing of insulation materials [27] and increase of torque ripple that could be not acceptable for several applications [28]. Finally, for EVs where a variable output voltage is required, NLC cannot be used at low voltage (i.e., at low speed) for the issues in controlling the circulating currents. This article demonstrates that by regulating the window length of the modulation, it is possible to smoothly increase the motor efficiency by reducing the WTHD, although at the expenses of a lower converter efficiency. This degree of freedom can be used to find a global maximum for a cost function accounting for overall efficiency and optimal operating conditions of the drive. However, this is beyond the scope of the article and is left for further analyses.

VII. NUMERICAL RESULTS ON A FULL-SCALE MODEL

In this section, the performance of the proposed modulation technique has been simulated numerically for further validation on a more realistic scale scenario. A full-scale simulation model has been developed to calculate the converter WTHD and efficiency when driving an automotive induction motor following a V/Hz constant algorithm. Motor parameters, taken from [29], are summarized in Table III. The converter has been sized in order to comply with the motor specifications with parameters summarized in Table IV. The simulations have been performed from 5 to 70 Hz with a constant load torque equal to half of the rated below the rated frequency, and a constant power equal to half of the rated over the rated frequency.

Simulation results for the WTHD of the converter are reported in Fig. 16. As expected, the WTHD of the NLC is the highest for almost all the frequencies. Moreover, every time a new module is activated, a discontinuity in the derivative of the WTHD is visible (marked with circles in the figure); this discontinuity is due to the change in the shape of the output voltages.

The efficiency has been calculated for the converter only and for the whole system (converter and induction motor) in order to include in the analysis the effect of losses due to current harmonics with results displayed in Figs. 14 and 15, respectively. In this full scale model, similarly to what was observed in the down-scaled model, at high frequency (speed), the greater is the

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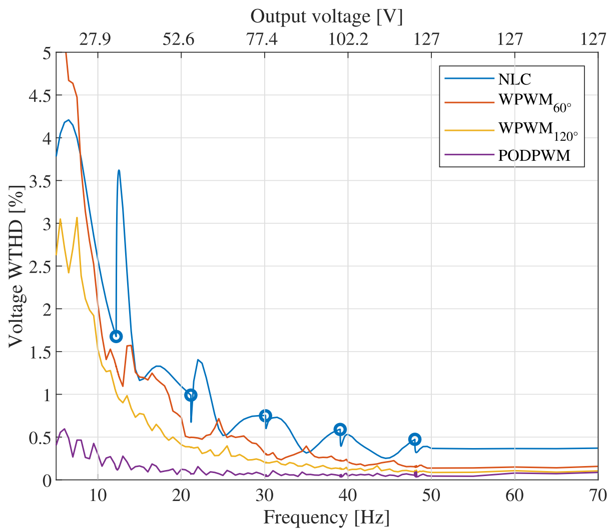

Fig. 16. Simulated full-scale converter WTHD.

PWM window, the lower the efficiency tends to be since conduction losses are equal for all the modulations and switching losses increase with the PWM window. Current harmonics are more relevant at low frequency (speed) since they are not strongly filtered by the induction motor. Thus, conduction losses of NLC become more relevant and the NLC efficiency is the lowest for several frequencies. This phenomenon is not evidenced in the down-scale prototype for the low number of modules making the switching losses more relevant with respect to the conduction losses.

In an electrical drive, even more relevant than the converter efficiency is the global efficiency in the conversion of stored energy to mechanical power. The efficiency of the traction drive (motor plus converter) is reported in Fig. 15. From the figure, it is clear that the NLC modulation at low speed is almost always the least efficient due to the increased current harmonics implying additional conduction losses. In the flux weakening zone (i.e., for frequencies higher than 50 Hz), the efficiency decreases for the more relevant effect of the viscous friction, accentuated by the reduction of the load torque.

VIII. Conclusion

This article proposes the windowed PWM as a modulation technique for double star chopped cells converters operated as variable frequency motor drives. The proposed modulation technique is compared with the NLC and the phase opposition disposition PWM. In comparison to the NLC, the windowed PWM reduces the current harmonic distortion while limiting the average switching frequency of the semiconductor devices. As predicted by simulations on a model of the converter, experimental data show that the W-PWM presents an efficiency higher that POD-PWM and, hence, it would increase the range of battery electric vehicles.

The introduced modulation technique adds a new degree of freedom, which allows a dynamic control of the output harmonic distortion and converter efficiency, leaving to the final user the flexibility to choose that is the most important factor to be optimized in the design. The possibility of changing the window angle allows variable speed drives to adapt the modulation technique dynamically with the speed at which the motor is rotating. Although this article is proposed for BEVs, the principle on which it is based can be applied also to a generic electrical drive.

Numerical and experimental WTHD analysis (Figs. 10 and 11) shows that the best window that ensures an output voltage WTHD reduction is dependent on the reference voltage and on the selected frequency. Due to these factors, a field implementation of that modulation technique should modify W-PWM window dynamically with the working condition. Although efficiency measurements in this article are affected by the uncertainties of the parameters of the test rig, the experimental results show that the efficiency achieved by the windowed PWM falls between the values of the NLC and POD-PWM as predicted by the numerical models. The increase in angle of the window of the W-PWM reduces both the output WTHD and the converter efficiency.

Depending on the specific application requirements, the proposed modulation technique can be used to achieve the optimal balance between efficiency and WTHD. In future works, an adaptive algorithm, changing the window length as function of the vehicle speed and torque, will be studied.

References

[1] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[2] J. O. Estima and A. J. M. Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Trans. Veh. Technol.*, vol. 61, no. 3, pp. 1021–1031, Mar. 2012.

[3] S. W. Moore and P. J. Schneider, "A review of cell equalization methods for lithium ion and lithium polymer battery systems," *SAE 2001 World Congress*, Apr. 2019. Q4

[4] S. D'Arco, L. Piegari, and P. Tricoli, "A modular converter with embedded battery cell balancing for electric vehicles," in *Proc. Electr. Syst. Aircraft, Railway Ship Propulsion*, Oct. 2012, pp. 1–6.

[5] L. M. Tolbert and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan. 1999.

[6] L. M. Tolbert, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[7] S. D'Arco, M. Quraan, P. Tricoli, and L. Piegari, "Low frequency operation of modular multilevel converters with embedded battery cells for traction drives," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, Jun. 2016, pp. 1375–1382.

[8] S. D'Arco, L. Piegari, M. S. Quraan, and P. Tricoli, "Battery charging for electric vehicles with modular multilevel traction drives," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drives*, Apr. 2014, pp. 1–6.

[9] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2041–2051, Mar. 2017.

[10] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 507–517, Jan. 2016.

[11] D. Fabiani and G. C. Montanari, "The effect of voltage distortion on ageing acceleration of insulation systems under partial discharge activity," *IEEE Electr. Insul. Mag.*, vol. 17, no. 3, pp. 24–33, May 2001.

[12] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Implementation of nearest level modulation for modular multilevel converter," in *Proc. IEEE 6th Int. Symp. Power Electron. Distrib. Gener. Syst.*, Jun. 2015, pp. 1–5.

[13] M. Guan, Z. Xu, and H. Chen, "Control and modulation strategies for modular multilevel converter based HVDC system," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2011, pp. 849–854.

[14] A. Marquez, J. I. Leon, S. Vazquez, L. G. Franquelo, and M. Perez, "A comprehensive comparison of modulation methods for MMC converters," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2017, pp. 4459–4464.

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[15] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, Jan. 2015.

[16] M. S. Rajan and R. Seyezhai, "Comparative study of multicarrier pwm techniques for a modular multilevel inverter," *Int. J. Eng. Technol.*, vol. 5, no. 6, pp. 4850–4865, Jan. 2014.

[17] A. D. Pizzo, M. Coppola, and I. Spina, "Current waveforms distribution among electrochemical cells of modular multilevel converters in battery electric vehicles," in *Proc. IEEE Int. Conf. Elect. Syst. Aircr., Railway, Ship Propulsion Road Vehicles Int. Transp. Electrific. Conf.*, Nov. 2018, pp. 1–4.

[18] G. Brando, A. Dannier, I. Spina, and P. Tricoli, "Integrated BMS-MMC balancing technique highlighted by a novel space-vector based approach for BEVs application," *Energies*, vol. 10, Oct. 2017, Art. no. 1628.

[19] S. D'Arco, L. Piegari, and P. Tricoli, "Power and balancing control considerations on modular multilevel converters for battery electric vehicles," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–9.

[20] G. B. Diaz, M. Boyra, and J. Vivas, "Novel control strategies for modular multilevel converters (MMC) - an evaluation and comparison of control and modulation schemes," in *Proc. Cigre Int. Symp. "Electric Power Syst. Future*," Sep. 2011.

[21] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[22] Y. Liang and C. O. Nwankpa, "A new type of statcom based on cascading voltage source inverters with phase-shifted unipolar spwm," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 33d IAS Annu. Meeting*, Oct. 1998, vol. 2, pp. 1447–1453.

[23] I. Ourdani, A. Bennani Ben Abdelghani, I. Slama Belkhodja, and D. Montesinos Miracle, "Phase opposition disposition PWM strategy and capacitor voltage control for modular multilevel converters," in *Proc. Int. Conf. Recent Adv. Electr. Syst.*, 2016, pp. 208–213.

[24] D. De Simone, L. Piegari, and S. D'Arco, "Comparative analysis of modulation techniques for modular multilevel converters in traction drives," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, Jun. 2018, pp. 593–600.

[25] J. Li and H. Hong, "Wthd optimization for single phase multilevel converters with step modulation," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2011, pp. 4463–4468.

[26] D. Graovac, M. Pürschel, and A. Kiep, "Mosfet power losses calculation using the data-sheet parameters," Infineon Tecnologies AG, pp. 1–22, Jul. 2006.

[27] F. Bertoldi, M. Pathmanathan, R. S. Kanchan, K. Spiliotis, and J. Driesen, "Quasi-two-level converter for overvoltage mitigation in medium voltage drives," in *Proc. Int. Power Electron. Conf.*, May 2018, pp. 488–494.

[28] B. Diong, H. Sepahvand, and K. A. Corzine, "Harmonic distortion optimization of cascaded h-bridge inverters considering device voltage drops and noninteger DC voltage ratios," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3106–3114, Aug. 2013.

[29] R. T.-Asl and J. Bauman, "Efficiency analysis of induction motor control strategies using a system-level EV model," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, Jun. 2019, pp. 1–6.

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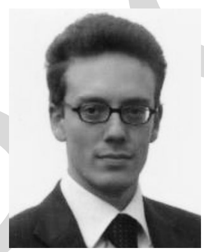

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Windowed PWM: A Configurable Modulation Scheme for Modular Multilevel Converter-Based Traction Drives

Davide De Simone, Luigi Piegari, *Senior Member, IEEE*, Pietro Tricoli, *Member, IEEE*, and Salvatore D'Arco

***Abstract*—This article introduces a modulation technique for modular multilevel converter (MMC) in variable speed traction drives for electrical transportation referred as windowed pulsewidth modulation (W-PWM). The windowed PWM (W-PWM) is derived by blending the principles of operation of conventional modulation schemes for MMC based on the nearest level control (NLC) and on PWM with the aim of combining their inherent strengths and offering a higher degree of flexibility. This can reduce switching losses compared to classical PWM schemes and lower the current harmonic distortion compared to NLC schemes. The window in which the PWM is applied can be seen as an additional degree of freedom that allows a dynamic optimization of the performance of the traction drive depending on its operating characteristics. The performance of the W-PWM technique is assessed in this article for several operating conditions and compared with conventional schemes based on NLC and on the phase opposition disposition PWM with both numerical simulation and experimental verification on a small-scale prototype. Results demonstrate the flexibility of the W-PWM and its potential for applications in electrical traction drives.**

***Index Terms*—AC motor drives, traction motor drives, power converter, road vehicle electric propulsion, pulsewidth-modulated power converters.**

I. Introduction

IN THE last few decades, private transport has become one of the main source of pollutants and it is now clear that the technical improvements on conventional internal combustion engines (ICE) will not be sufficient to reduce the global CO2 emissions. Battery electric vehicles (BEVs) are a valid alternative to ICE vehicles and although the sales are now accelerating, battery electric vehicles (BEVs) still represent only 1% of the consumer market. Main factors slowing the penetration of BEV are arguably the perceived limitations of the technology as the limited vehicle range and the long battery recharge time [1].

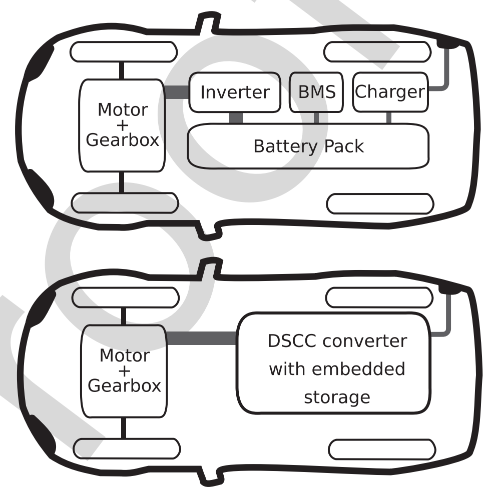

Fig. 1. Typical BEV powertrain.

A typical power train of a BEV includes several power converters, as represented in Fig. 1. The battery pack is composed by connecting in series a large number of low voltage cells [2]. Due to unavoidable differences between the cells, a battery management system is required to ensure that each individual cell remains within its voltage limits [3]. The traction inverter is responsible to supply and control the motor, while a separate on-board battery charger could be added to charge the battery pack from the utility grid. In many vehicles, the on-board battery charger has a low power rating, typically up to 7 kW, leading to long charging times when an external dc rapid charger is not available.

In [4], D'Arco *et al.* proposed a configuration for BEVs based on a double star chopper cell (DSCC) converter, belonging to the family of modular multilevel converter (MMC). This DSCC-based configuration embeds in a single converter the functions of the traction inverter [5], the battery management system (BMS) [6], [7], and the battery charger [8]. Multilevel topologies as the cascaded H-bridge (CHB), the single-star bridge-cell (SSBC), and the single-delta bridge-cell (SDBC) topologies also can control the power supplied by the individual battery modules, thereby allowing the integration of both traction drive and BMS functionalities. However, the DSCC offers more flexibility than

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CHB, SSBC, and SDBC configurations, as the direct, inverse, and zero sequence of the circulating currents can be used for cell balancing. Additionally, the DSCC can be connected to an external dc source for charging the batteries as an alternative to ac charging. For this reason, in this article, the DSCC will be addressed.

Using the same converter for different tasks leads to a higher global efficiency in comparison with standard two-level inverters [9] with consequent more range of the BEV. This is also supported by the fact that balancing is achieved using the load current rather than transferring energy between the cells. The single converter does not influence negatively the reliability of the system since, as demonstrated in [10], the proposed topology presents a high redundancy. As DSCCs can handle the rated power also for charging operations, rapid charging is allowed without the need of extra hardware on-board.

The efficiency of motor drives with DSCCs could be further increased by adopting new modulation strategies with lower switching losses. However, any modulation strategy has to consider the impact on the total harmonic distortion (THD) of the current, as harmonics increase the losses of the motor and generate torque ripples that lead to mechanical vibrations and faster wear of the transmission. In the automotive industry, the drive system efficiency and the injected THD are a major concern since it might affect the lifespan of insulation systems [11] and the general driving performance. As harmonics depend on load parameters and, hence, are not constant for all the operating conditions, the comparison between different modulation techniques is usually based on the voltage weighted total harmonic distortion (WTHD).

Two main families of MMC modulation techniques can be identified in the technical literature: modulation schemes based on nearest level control (NLC) [12], [13] and schemes based on pulsewidth modulation (PWM) [14]–[16]. NLC techniques present the lowest switching losses but relatively high WTHD of the phase voltage and motor losses, whereas PWM has opposite characteristics. In this article, the authors propose a modulation technique called windowed-PWM (W-PWM) that applies PWM only at specific angular intervals of the reference waveform to achieve the optimal compromise between power losses and WTHD. Therefore, the angles in which PWM is applied can be controlled dynamically and continuously and adapted to the different operating conditions of the traction drive. Even if not explicitly addressed in this article, the proposed technique can be also easily extended to any electrical drives with multilevel converters and especially medium voltage drives for which switching losses are particularly critical.

The article is organized as follows. Section II summarizes the application of the DSCC topology for traction drives. Section III reviews the state of the art of modulation techniques and control strategies for multilevel inverters. The W-PWM and its main characteristics are described in Section IV. A detailed description of the simulation and test rig is given in Section V. Section VI shows the main numerical and experimental results. Section VIII summarizes the main outcomes and draws the conclusion of this article.

II. Reference System Configuration

The reference system configuration assumed for this article is a traction drive composed by an induction machine connected to a DSCC converter embedding an energy storage cell with voltage v_m in each module as represented in Fig. 2. As in standard MMCs, the arm inductors can be mutually coupled to reduce the weight of the converter and to reduce the output voltage drop. To generate the output phase voltage, the following voltage references are sent to the upper and lower arm of each phase

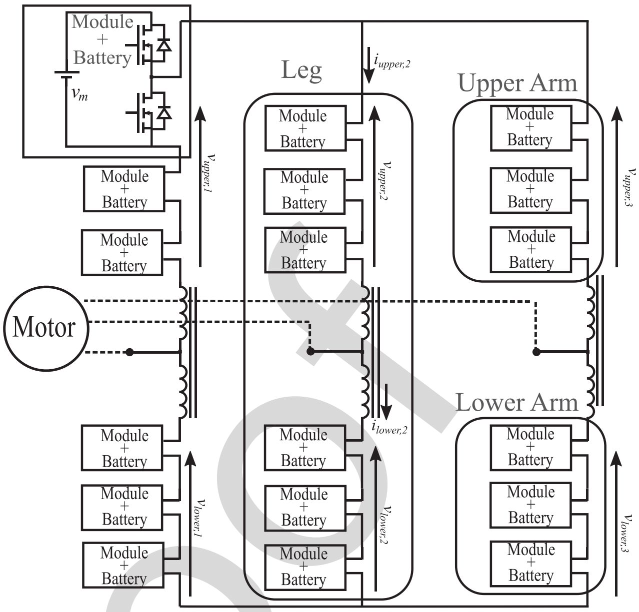

Fig. 2. Double star chopped cell converter topology.

$$\begin{cases} v_{\text{lower},k} = \frac{v_{\text{dc,bus}}}{2} + v_{\text{phase},k} + v_{k,\text{circ}} \\ v_{\text{upper},k} = \frac{v_{\text{dc,bus}}}{2} - v_{\text{phase},k} + v_{k,\text{circ}} \end{cases} \tag{1}$$

where $v_{\text{dc,bus}}$ is the dc bus voltage, $v_{\text{phase},k}$ is the phase voltage reference of a generic converter leg "k" [17], and $v_{k,\text{circ}}$ is the cell balancing control voltage referred to the same converter leg [4], [18]. From upper and lower arm voltages (1), the expression of the output phase voltage $v_{\text{phase},k}$ is obtained as

$$v_{\text{phase},k} = \frac{1}{2}\left[v_{\text{lower},k} - v_{\text{upper},k}\right]. \tag{2}$$

If the per unit impedance of the leg inductors is low and/or if the output frequency is low, $v_{\text{upper},k}$ and $v_{\text{lower},k}$ must be generated so that the total number of inserted modules is equal across the three converter legs. If this condition is not met, the difference between the instantaneous voltage of the legs give rise to circulating currents.

DSCCs can use circulating currents between legs acting on $v_{k,\text{circ}}$ of (1) to exchange energy between battery cells, acting effectively as a BMS. The energy stored in a battery can be quantified by the state of charge (SOC), which is the ratio between the available energy and the total battery capacity. Since the estimation of the SOC is not the main focus of this article, a simple Coulomb-counting method was considered for sake of simplicity [10]

$$\text{SOC}_h(t) = \text{SOC}_h(t_0) - \frac{1}{3600 \cdot Q_{\max}} \left(\int_{t_0}^{t} i_h(t)dt \right) \tag{3}$$

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with $\mathrm{SOC}_h(t_0)$ the hth cell SOC at initial time, and $Q_{\max}$ the total module battery capacity in Ah. Moreover, $i_h(t)$ is the battery current, which was estimated knowing the current flowing in the arm in which the module is installed and the conduction state (ON or OFF) of the module itself. A positive current discharges the battery reducing its SOC.

The balancing process is achieved through three control loops [19], namely leg balancing, arm balancing, and module balancing. The leg balancing algorithm operates on the dc voltage reference of each leg to impose a dc circulating current. This current transfers energy between the phases of the converter so that the average SOC is the same for all the phases. The arm balancing algorithm balances the average SOCs of the upper and lower arms of each phase. The exchange of energy within the arms of the same leg is achieved by imposing a negative and positive sequence current synchronized with the output phase voltage [18]. The circulating currents cannot be accurately controlled with an NLC modulation technique in converters with a limited number of modules or at low frequency. This could lead to high circulating currents and risks of damaging the converter. Therefore, if cells belonging to different legs and phases are strongly unbalanced, a PWM modulation technique is necessary. Once the balancing is completed, NLC or W-PWM modulation techniques can be applied.

The module balance algorithm equalizes the SOC of all the cells included in each arm. This is achieved by controlling the modules to activate using a sorting algorithm: if the current charges the cells of the arm, the modules with the lowest SOC are turned ON first; if, instead, the current discharges the cells, the modules with the higher SOC are used first.

When used as battery chargers, DSCC converters can be connected to either single-phase, three-phase, and dc power sources with no modification of the hardware and, therefore, they are a versatile choice for automotive applications. As DSCCs have typically a high number of voltage levels, they can be connected to the power source with no or very small filters, reducing the curb weight of the BEVs on which they are installed.

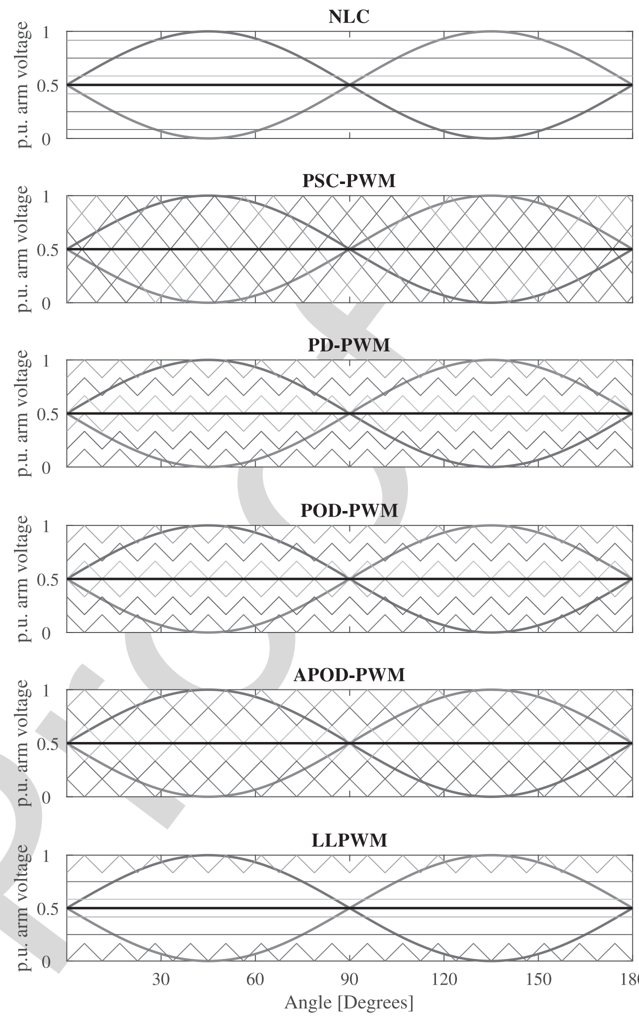

Fig. 3. Carrier and arm references of different modulation techniques.

III. DSCCs Modulation Techniques

This section reviews the most widely used modulation techniques for DSCCs [10], [14], i.e., the NLC, the carrier phase shifted PWM, the phase disposition PWM (PD-PWM), the phase opposition disposition PWM (POD-PWM), the alternate phase opposition disposition PWM (APOD-PWM) and the last level PWM (LLPWM), which are shown in a qualitative way in Fig. 3 in the case of four modules per arm converter.

A. Nearest Level Control

In the NLC modulation technique, the modules are activated or deactivated to minimize the error $e_v = v^*_{\mathrm{phase},k} - v_{\mathrm{phase},k}$, where $v^*_{\mathrm{phase},k}$ represents the reference of the phase k output voltage, and $v_{\mathrm{phase},k}$ represents the actual phase k voltage. When the error is above a specified threshold, the related module is activated [12]. In accordance with [13], the NLC algorithm has been implemented considering the mean voltage of the modules

$$v_{th}(n) = (n-1)\cdot \overline{V}_m + \frac{1}{2}\overline{V}_m \tag{4}$$

where $v_{th}(n)$ is the threshold voltage of the nth module and $\overline{V}_m$ is the module mean voltage.

B. Phase Shifted Carrier Pulsewidth Modulation

This modulation technique is the extension of the traditional sinusoidal PWM strategy to multilevel converters [20], [15], [21], [22]. If the converter has N modules per arm, the output voltage is generated by comparing $2 \cdot N$ equally shifted triangle carrier signals with the arms modulation signals. With this modulation technique, all the modules are switched in each carrier period, removing the need of the inner arms balancing algorithm (see Section II) and, hence, simplifying the control of the converter. The generated output phase voltages are characterized by $N+1$ levels. In this modulation, the carrier frequency applied to the modules f_{carrier} is N times smaller than the desired output switching frequency f_{sw}: $f_{\mathrm{carrier}} = \frac{f_{\mathrm{sw}}}{N}$. Thus, each module is subjected to lower frequency harmonics.

C. Phase Disposition Pulsewidth Modulation

In this modulation technique, an individual carrier signal with amplitude equal to the module voltage is assigned to each

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module [20], [23], [21]. The offset given by (4) is added to each carrier. The carrier signals are shifted by the module sorting algorithm. For example, if the current is charging, the modules with the lower SOC are shifted at the bottom to keep them turned ON for the maximum possible time. The total number of active modules for each leg differs by ± 1 module. This leads to $2 \cdot N + 1$ levels on the output phase voltage, but also introduces additional voltage ripple across the arm inductors with consequent increase of the circulating currents.

D. Phase Opposition Disposition Pulsewidth Modulation

This modulation technique is based upon the same principles of PD-PWM, with the difference that the carriers of the upper arm are delayed by half a period of those of the lower arm [20], [21], [23]. With this modification, the total number of active modules per leg is always the same, independently on the modulation index, thus, the internal circulating currents are minimized. The output phase voltage is obtained changing the distribution of active modules between the upper and the lower arms within a converter leg. This modulation strategy generates an output phase voltage with $N + 1$ levels.

E. Alternate Phase Opposition Disposition Pulsewidth Modulation

The APOD-PWM is based upon the same principle of POD-PWM, but the carrier signals of odd modules have a 180° shift in respect to the even modules [21], [23]. In the POD-PWM, this modulation technique generates $N + 1$ levels and presents no theoretical voltage ripples across the dc bus.

F. Last Level Pulsewidth Modulation

LLPWM is a hybrid NLC-PWM modulation strategy proposed in [24]. LLPWM generally activates the components of the converter using NLC. At each module activation, the controller checks the peak value of the reference, if the module in activation will be the last one (top and bottom point of the reference) PWM will be applied on that particular module.

IV. Windowed Pulsewidth Modulation

The W-PWM applies PWM around the peak value of the sinusoidal reference signals to reduce the harmonic distortion of the generated voltages. For operations with variable voltage amplitude and frequency like EV applications, it is necessary to identify the correct position of the peak values, as the signals are not strictly sinusoidal. To do so, the modulation is switched between NLC and POD-PWM in relation of the phase angle of the reference space vector. By choosing appropriate space vector phase intervals, NLC can be applied to the steepest areas of the output waveforms while PWM can be applied where the derivative of the reference is relatively small. W-PWM carrier signals are generated following (5), $x(t)$ represents a triangle wave with average value of zero and peak values of ± 1, u represents the control variable that turns ON and OFF the PWM signal and V_i is the nth module voltage

$$v_{th}(n,t) = \sum_{i=1}^{n-1} V_i + (1 + u \cdot x(t))) \cdot \frac{1}{2} V_n. \qquad (5)$$

TABLE I
W-PWM Activation Angles as Function of ϕ = Window, θ = Space Vector Angle

Phase		
A	$-\frac{\phi}{2} \le \theta \le \frac{\phi}{2}$	$\pi + \frac{\phi}{2} \le \theta \le \pi - \frac{\phi}{2}$
B	$\frac{2}{3}\pi + \frac{\phi}{2} \le \theta \le \frac{2}{3}\pi - \frac{\phi}{2}$	$\frac{5}{3}\pi + \frac{\phi}{2} \le \theta \le \frac{5}{3}\pi - \frac{\phi}{2}$
C	$\frac{4}{3}\pi + \frac{\phi}{2} \le \theta \le \frac{4}{3}\pi - \frac{\phi}{2}$	$\frac{\pi}{3} + \frac{\phi}{2} \le \theta \le \frac{\pi}{3} - \frac{\phi}{2}$

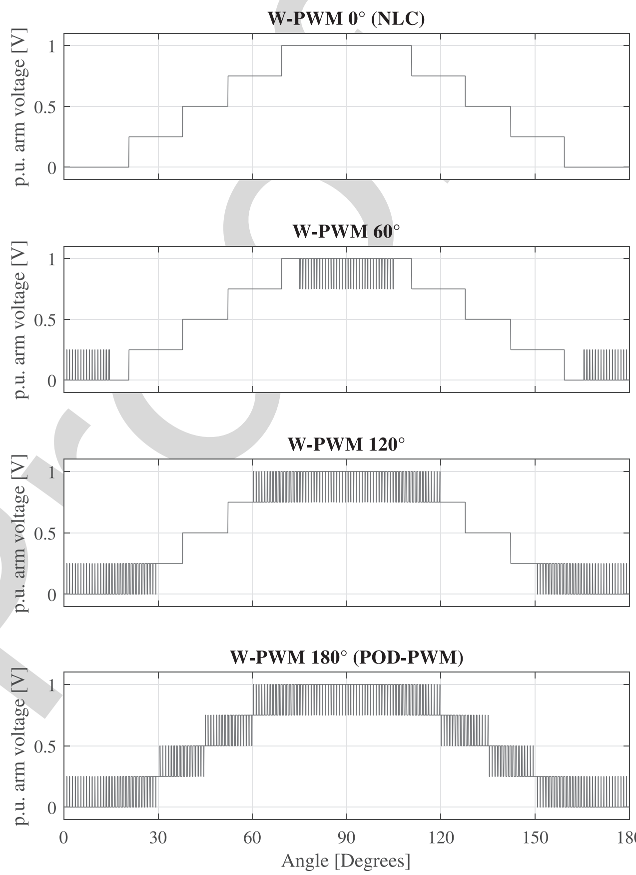

Fig. 4. Qualitative W-PWM arm voltages at NLC, W-PWM 60°, 120° and POD-PWM.

Starting from a three-phase voltage reference, the related space vector is calculated according to

$$\overline{v^*} = \frac{2}{3}\left[v_a^*(t) + v_b^*(t) \cdot e^{j\frac{2}{3}\pi} + v_c^*(t) \cdot e^{j\frac{4}{3}\pi}\right] \qquad (6)$$

where $v_a^*(t)$, $v_b^*(t)$, and $v_c^*(t)$ are the three-phase output voltage references. The phase of the space vector is, then, compared with the intervals of Table I. In each period of the waveform, there are two PWM intervals, around the positive and the negative peaks, respectively. If the phase does not fall within one of the two intervals, the control variable u is set to zero, thus the carrier signal is replaced by its average value and the W-PWM reduces to the NLC modulation. On the contrary, if the phase of the space vector falls in one of the two intervals, u is set to one enabling the PWM.

Fig. 4 shows the output converter arm voltages with different W-PWM windows sizes.

The W-PWM enables a precise control of the PWM window and the length of this window is effectively a new degree of

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TABLE II
TESTED MMC MAIN PARAMETERS

Parameter	Value
Modules per arm	4
Module Battery	PL-9759156-5C
Mosfet Switches	IRF1324S-7PPbF
Arm Inductance	22 μH
Arm resistance	30 $m\Omega$

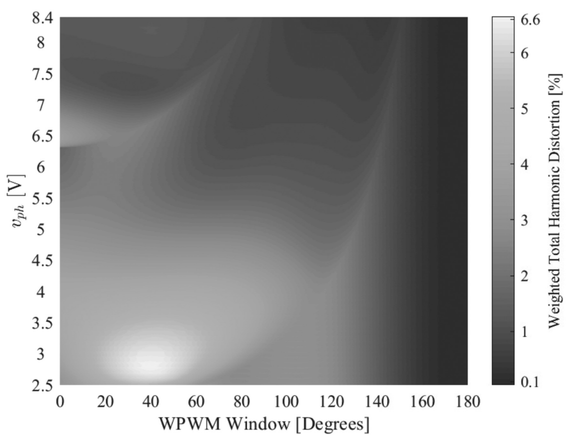

Fig. 5. WTHD as a function of output voltage and W-PWM window of a generic four modules per arm MMC.

freedom for the control system. It is worth noting that for certain values of ϕ that depends on the number of modules of the converter and on the magnitude of the voltage reference, W-PWM reduces to LLPWM modulation [24].

V. Simulation and Experimental Set-Up

To study the W-PWM characteristics, a Simulink model has been developed to obtain a relation between the harmonic distortion, quantified with the WTHD of the output voltage, the amplitude of the output voltage, the output frequency, and the PWM window size. The WTHD has been calculated in accordance with [25] as

$$\mathrm{WTHD} = \frac{1}{V_1}\left[\sum_{n=2,3..}^{\infty}\left(\frac{V_n}{n}\right)^2\right]^{1/2} \tag{7}$$

where V_1 is the amplitude of the first harmonic, V_n is the amplitude of the *n*th harmonic, and *n* is the harmonic order.

A switching model with the same characteristics of the small scale prototype whose main components are summarized in Table II has been used. Conduction losses were considered using the Simscape library blocks and matching switches and inductances parameters with the ones of the prototype. To estimate switching losses, the current and the voltages across each solid state switch were measured. Every time a change in the control signal is experienced, the procedures described in [26] were used to calculate the switching losses.

In Fig. 5, the variation of the output voltage WTHD as a function of the reference voltage amplitude and the PWM window angle is illustrated. The results have been obtained by means of several simulations using a V/Hz constant control law with base speed reached at 50 Hz and 8.4 V. It is worth noting that, when the output voltage reference is below 0.25 p.u. (2.1 V), NLC does not generate any signal and, hence, the WTHD of the waveform cannot be calculated. Moreover, the WTHD for NLC changes from 12.8% to 3.34% when the reference voltage increases from 2.2 to 2.5 V. However, for a clearer data representation, the v_{ph} axis of Fig. 5 starts from 2.5 V since the color mapping would become too flat in the zone of more interest if the minimum voltage is set to lower values (e.g., 2.1 V).

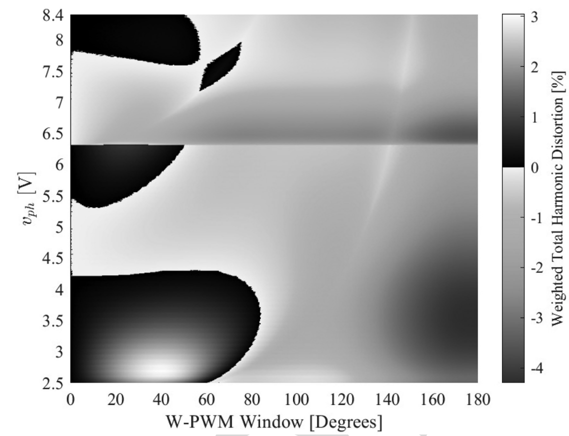

Fig. 6. Difference between the $\mathrm{WTHD}_{\text{w-pwm}}$ and the $\mathrm{WTHD}_{\text{NLC}}$ for a four modules per arm MMC.

In order to better visualize which PWM windows improve the WTHD with respect to the NLC at each output voltage/frequency, the difference between the WTHD for the W-PWM and the NLC is shown in Fig. 6. All the negative results are represented with a color gradient where the lowest values are blue and the highest values are yellow. The more negative is the differential WTHD, the more the selected window is improving the WTHD with respect to NLC. All the positive differences instead are represented with a gray scale; those values imply that the introduction of W-PWM with the corresponding window leads to a worse WTHD.

From the analysis of Fig. 6, it is possible to determine that 84° is the smallest window ensuring a WTHD lower than NLC for every value of the desired output voltage. Since the results obtained by simulation (Figs. 5 and 6) could not be obtained experimentally with the same detail level, the aim of the comparison between simulation and experimental results is to validate the simulation results measuring the converter performance in a reduced set of operating regions.

The experimental tests have been carried out on a DSCC prototype with four modules per arm, each one including a 4.2 V 10 Ah LiPo battery, as shown in Fig. 7. The main converter parameters are summarized in Table II. The controller has been implemented on a NI CompactRio FPGA system. From (2), it is possible to state that the maximum phase voltage is one half of the maximum arm voltage, thus, the maximum output voltage is 8.4 V with this configuration. The converter is connected to a variable load consisting of a 12–400 V step-up transformer, a variac, and a resistive load, as reported in Fig. 8. In the laboratory configuration, low voltage battery cells and a transformer have been used both due hardware availability and safety reasons even though higher voltage battery modules would be preferable in a real application. With this set-up, it is possible to regulate the

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Fig. 7. Experimental set-up.

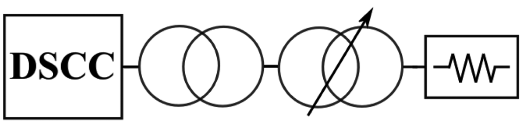

Fig. 8. Schematic overview of the test setup.

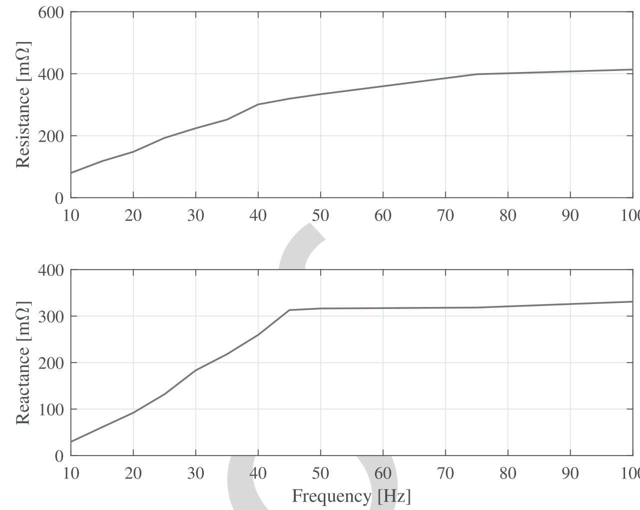

Fig. 9. Load resistance (top) and reactance (bottom) measured with POD-PWM.

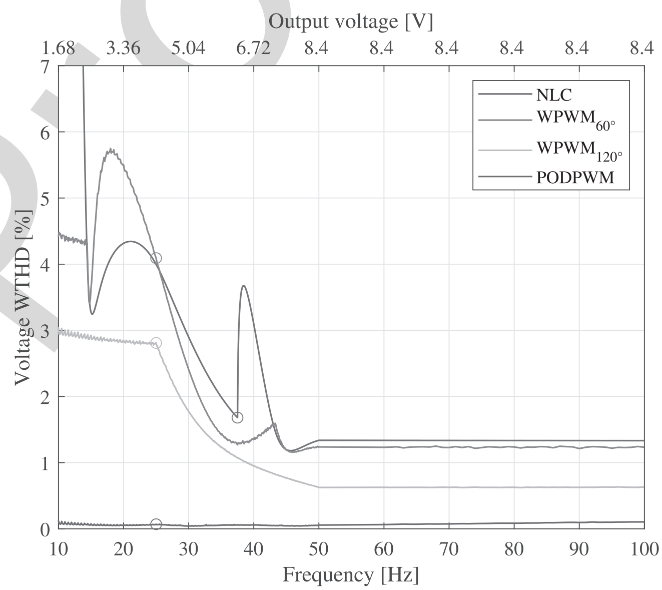

Fig. 10. Simulated output voltage WTHD when controlled with a V/Hz constant strategy. Circles identifies points in which a new module is added to generate the output.

output current while changing the converter output voltage and frequency.

The efficiency of the converter has been estimated by extrapolating the measurement from a single module, as the average power losses are the same if the cells are well balanced.

VI. Numerical and Experimental Results on a Down-Scaled System

The proposed W-PWM has been compared with NLC and POD-PWM in terms of output harmonic distortion and converter efficiency. The simulation and experimental tests have been undertaken with a load drawing 10 A rms and using a V/Hz Q3 constant law in the range 0 to–Hz (0 to 8.4 V) and a constant voltage over 50 Hz. The Simulink model used to perform the simulations reported in this chapter is a detailed reproduction of the converter described in Section V.

Simulation results are, then, compared with experimental data to ensure that the detailed behavior in terms of WTHD reported in Fig. 6. In theory, the test rig in Fig. 7 should change only the equivalent resistance seen by the converter. In practice, also the load inductance is affected by the nonlinearity of the two transformers. Therefore, the equivalent load parameters were estimated from the experimental data and, then, used in the detailed simulation. The estimation of the load parameters was obtained starting from the first harmonics phasors of the measured voltage and current waveforms. The measured load parameters were independent from the modulation technique, the resultant load parameters obtained from this analysis are summarized in Fig. 9.

A. *WTHD Evaluation*

The voltage WTHDs are measured for different output voltages. For what concerns W-PWM, window angles multiple of 60° are tested. Fig. 10 compares the voltage WTHD produced by the different W-PWM windows, whereby the values of 0° and 180° are equivalent to NLC and POD-PWM, respectively. As a general rule, the wider the PWM window, the lower the WTHD. For specific values of W-PWM windows, output voltage and output frequency, the harmonic distortion obtained by W-PWM becomes higher than the NLC.

The NLC and the PWM follow a different approach for activating additional cells. The PWM-based techniques activate new modules when reaching a voltage equivalent to an integer number of voltage cells while the NLC activates new modules when passing values in the middle of the voltage cell. This means that a diagram of the number of levels will jump from 1 to 2 at 6.3 V for the NLC while the same happens at 4.2 V for the PWM. As a V per Hz constant control algorithm has been applied, the voltage levels are proportional to the fundamental frequency of the output. Additionally, as the carriers are all the same, the type of PWM technique will not affect where there is the change of number of levels. Changes in the number of active levels are highlighted in Fig. 10 with circles.

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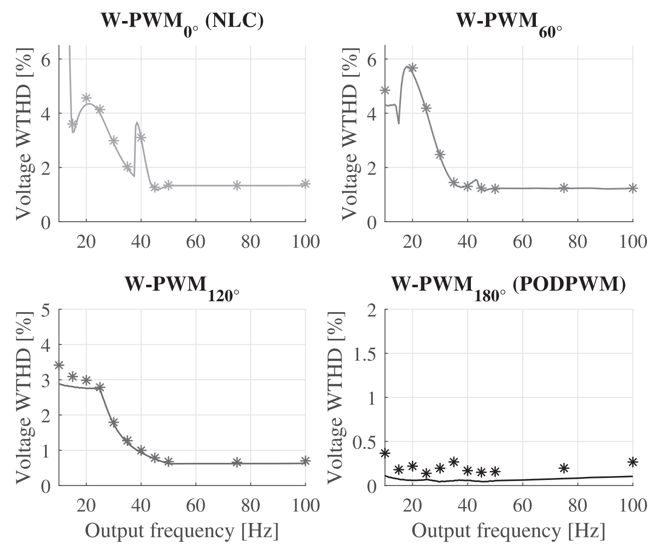

Fig. 11. Simulated (continuous line) versus measured (markers) converter WTHDs when controlled with a V/Hz constant strategy.

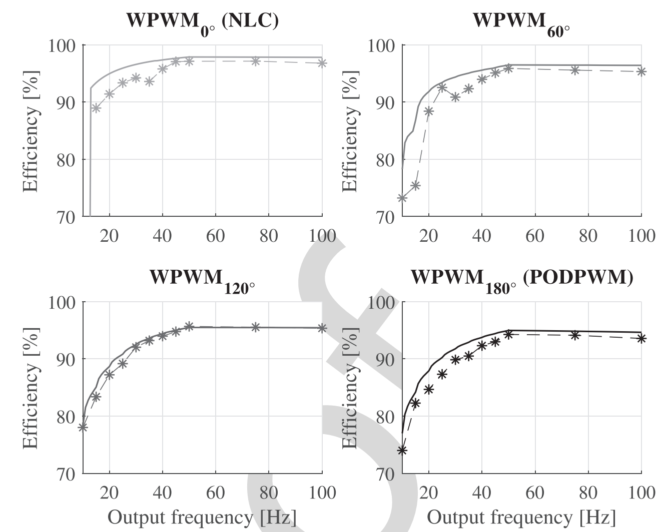

Fig. 13. Simulated (continuous line) versus measured (markers) converter efficiency when controlled with a V/Hz constant strategy.

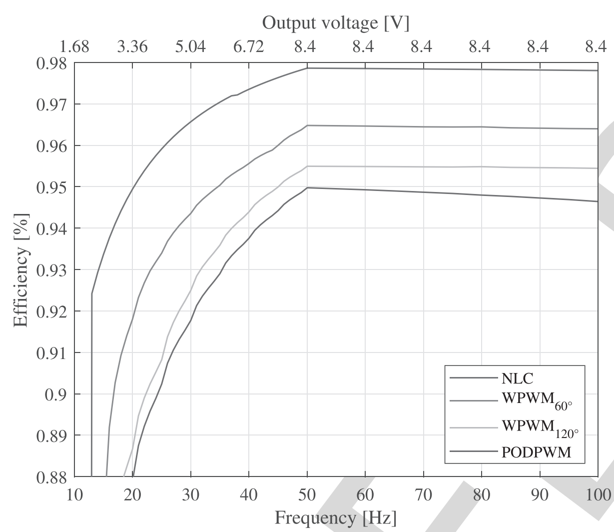

Fig. 12. Simulated converter efficiency when controlled with a V/Hz constant strategy.

The experimental data on the test rig are compared with the simulations in Fig. 11: the peaks of the NLC voltage WTHD due to the activation of a new module can be clearly seen also from the measurements. For the W-PWM at 120° and for the POD-PWM, this is not visible because the angle of PWM is sufficiently large to include the instant when an extra module is activated. Since the converter has four modules per arm, just two modules are triggered over the whole output voltage range. At 20 Hz, 3.36 V (on the first NLC WTHD peak), it is clear that W-PWM windows larger than 60° improve significantly the output WTHD. When a 60° window is considered, a poor performance is experienced, as predicted by the preliminary analysis shown in Fig. 6. At higher frequencies (at converter nominal voltage), W-PWM with 60° gives a very limited WTHD improvement with respect to NLC. W-PWM reduces the output voltage WTHD in a good agreement with the theoretical analysis.

B. *Efficiency Evaluation*

In the simulations, the converter efficiency was calculated as the ratio between the load power and the total battery injected power over a predefined time period. In the experiments, the efficiency was measured as the ratio of the output and input energy of one module of the converter. To ensure that the data extrapolated from one module represent accurately the global converter efficiency, it is extremely important that each module remained perfectly balanced with the others. Under this condition, all the modules have the same voltage and contribute equally to the generated power. Moreover, if the gate signals are all synchronized, when the cells are balanced there is no net power exchange between the three phases. To ensure this assumption was met, before each test, all the cells were charged an average of 30 min to restore a 100% SOC. Additionally, it is important that the module selected for the measurement was used as much as the others during the observation. To meet this condition, the sorting algorithm that balances the module SOCs [18], [19] was replaced with a function that sets the module priority with a fixed periodic pattern with period 1 s. The logging time interval of the instruments was set accordingly to 1 s.

In V/Hz constant tests, 11 points between the frequency range 10–100 Hz were taken for each investigated W-PWM window. The load current was kept constant at 10 A below 50 Hz. For NLC and some W-PWM windows, 10 A load current was not reachable at low voltage references. In these conditions, the maximum achievable current was set. Due to the approximations introduced to measure the efficiency, the longer are the tests, the higher is the unbalance level between the modules introduced by unavoidable differences among the storage system, leading to less reliable results. From the analysis of Fig. 13 in which experimental and theoretical data are reported on the same diagram, it is reasonable to state that there is a good matching between theoretical and experimental results.

Looking at the NLC curve reported in Fig. 12, the global efficiency is higher than all the other modulation schemes. An efficiency drop can be seen when the second module is turned ON. The phenomenon is related to the increase of the

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TABLE III
INDUCTION MOTOR PARAMETERS

Parameter	Value
Nominal voltage	$156\ V$
Nominal frequency	$50\ Hz$
Number of pole pairs	2
Stator resistance	$10\ m\Omega$
Rotor resistance	$10\ m\Omega$
Stator leakage inductance	$0.2\ mH$
Rotor leakage inductance	$0.2\ mH$
Magnetizing inductance	$5\ mH$

harmonic distortion of the load that reduces the active power transferred, and to the short duration of module on-time that increases switching losses without increasing significantly the load active power. The efficiency of the W-PWM is always between the NLC and the POD-PWM. In general, the longer the PWM window, the higher the switching losses and, hence, the lower the efficiency. As expected, the POD-PWM has the lowest efficiency for the highest number of device commutations per period.

It is worth noting that the NLC seems to be always preferable when looking only at the converter efficiency. However, the NLC increases the WTHD resulting in higher harmonics of the motor current and, thus, lower motor efficiency. Therefore, the global efficiency of the drive system is optimized with a combination of NLC and PWM. Moreover, increasing the WTHD could imply additional problems like accelerated ageing of insulation materials [27] and increase of torque ripple that could be not acceptable for several applications [28]. Finally, for EVs where a variable output voltage is required, NLC cannot be used at low voltage (i.e., at low speed) for the issues in controlling the circulating currents. This article demonstrates that by regulating the window length of the modulation, it is possible to smoothly increase the motor efficiency by reducing the WTHD, although at the expenses of a lower converter efficiency. This degree of freedom can be used to find a global maximum for a cost function accounting for overall efficiency and optimal operating conditions of the drive. However, this is beyond the scope of the article and is left for further analyses.

VII. NUMERICAL RESULTS ON A FULL-SCALE MODEL

In this section, the performance of the proposed modulation technique has been simulated numerically for further validation on a more realistic scale scenario. A full-scale simulation model has been developed to calculate the converter WTHD and efficiency when driving an automotive induction motor following a V/Hz constant algorithm. Motor parameters, taken from [29], are summarized in Table III. The converter has been sized in order to comply with the motor specifications with parameters summarized in Table IV. The simulations have been performed from 5 to 70 Hz with a constant load torque equal to half of the rated below the rated frequency, and a constant power equal to half of the rated over the rated frequency.

Simulation results for the WTHD of the converter are reported in Fig. 16. As expected, the WTHD of the NLC is the highest for almost all the frequencies. Moreover, every time a new module is activated, a discontinuity in the derivative of the WTHD is visible (marked with circles in the figure); this discontinuity is due to the change in the shape of the output voltages.

The efficiency has been calculated for the converter only and for the whole system (converter and induction motor) in order to include in the analysis the effect of losses due to current harmonics with results displayed in Figs. 14 and 15, respectively. In this full scale model, similarly to what was observed in the down-scaled model, at high frequency (speed), the greater is the

TABLE IV
FULL-SCALE MMC PARAMETERS

Parameter	Value
Modules per arm	14
Module Voltage	$22.2\ V$
Mosfet Switches	MMIX1T550N055T2
Arm Inductance	$22\ \mu H$
Arm resistance	$3\ m\Omega$

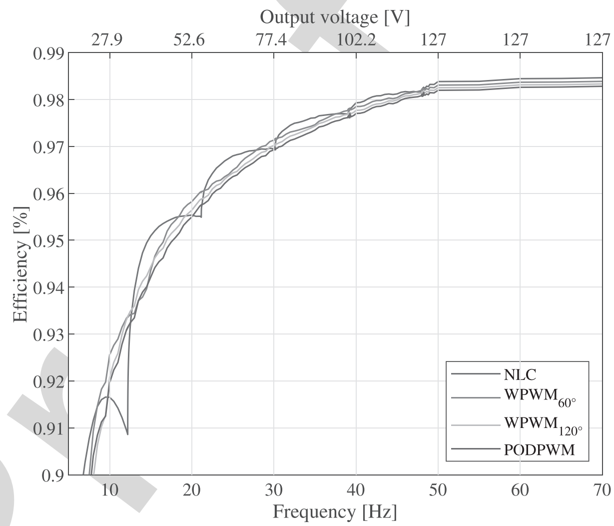

Fig. 14. Simulated full-scale converter efficiency.

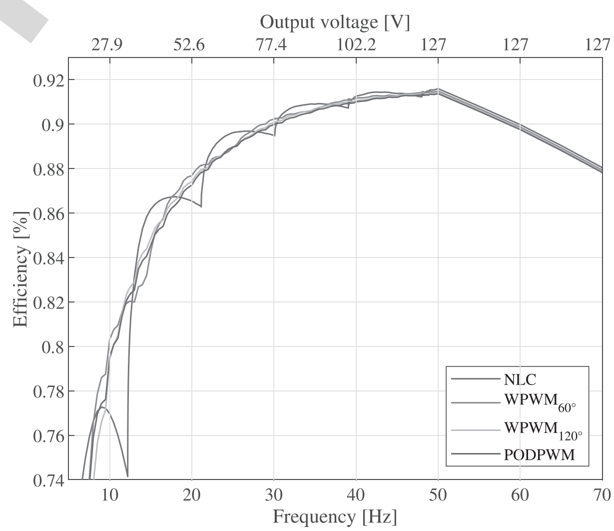

Fig. 15. Simulated full-scale converter and motor efficiency.

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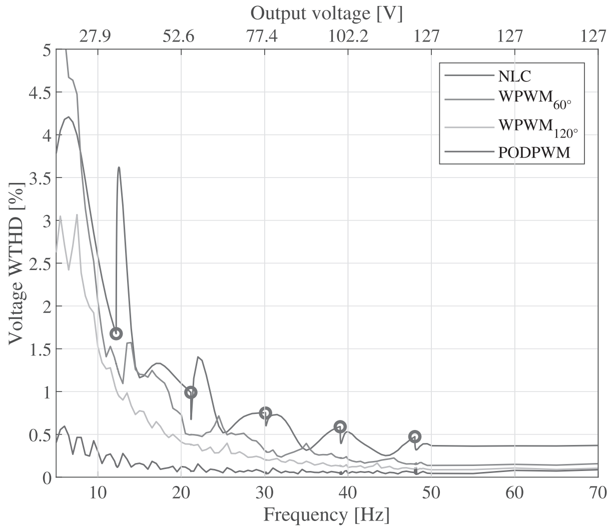

Fig. 16. Simulated full-scale converter WTHD.

PWM window, the lower the efficiency tends to be since conduction losses are equal for all the modulations and switching losses increase with the PWM window. Current harmonics are more relevant at low frequency (speed) since they are not strongly filtered by the induction motor. Thus, conduction losses of NLC become more relevant and the NLC efficiency is the lowest for several frequencies. This phenomenon is not evidenced in the down-scale prototype for the low number of modules making the switching losses more relevant with respect to the conduction losses.

In an electrical drive, even more relevant than the converter efficiency is the global efficiency in the conversion of stored energy to mechanical power. The efficiency of the traction drive (motor plus converter) is reported in Fig. 15. From the figure, it is clear that the NLC modulation at low speed is almost always the least efficient due to the increased current harmonics implying additional conduction losses. In the flux weakening zone (i.e., for frequencies higher than 50 Hz), the efficiency decreases for the more relevant effect of the viscous friction, accentuated by the reduction of the load torque.

VIII. Conclusion

This article proposes the windowed PWM as a modulation technique for double star chopped cells converters operated as variable frequency motor drives. The proposed modulation technique is compared with the NLC and the phase opposition disposition PWM. In comparison to the NLC, the windowed PWM reduces the current harmonic distortion while limiting the average switching frequency of the semiconductor devices. As predicted by simulations on a model of the converter, experimental data show that the W-PWM presents an efficiency higher that POD-PWM and, hence, it would increase the range of battery electric vehicles.

The introduced modulation technique adds a new degree of freedom, which allows a dynamic control of the output harmonic distortion and converter efficiency, leaving to the final user the flexibility to choose that is the most important factor to be optimized in the design. The possibility of changing the window angle allows variable speed drives to adapt the modulation technique dynamically with the speed at which the motor is rotating. Although this article is proposed for BEVs, the principle on which it is based can be applied also to a generic electrical drive.

Numerical and experimental WTHD analysis (Figs. 10 and 11) shows that the best window that ensures an output voltage WTHD reduction is dependent on the reference voltage and on the selected frequency. Due to these factors, a field implementation of that modulation technique should modify W-PWM window dynamically with the working condition. Although efficiency measurements in this article are affected by the uncertainties of the parameters of the test rig, the experimental results show that the efficiency achieved by the windowed PWM falls between the values of the NLC and POD-PWM as predicted by the numerical models. The increase in angle of the window of the W-PWM reduces both the output WTHD and the converter efficiency.

Depending on the specific application requirements, the proposed modulation technique can be used to achieve the optimal balance between efficiency and WTHD. In future works, an adaptive algorithm, changing the window length as function of the vehicle speed and torque, will be studied.

References

[1] M. Yilmaz and P. T. Krein, "Review of battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.

[2] J. O. Estima and A. J. M. Cardoso, "Efficiency analysis of drive train topologies applied to electric/hybrid vehicles," *IEEE Trans. Veh. Technol.*, vol. 61, no. 3, pp. 1021–1031, Mar. 2012.

[3] S. W. Moore and P. J. Schneider, "A review of cell equalization methods for lithium ion and lithium polymer battery systems," *SAE 2001 World Congress*, Apr. 2019. Q4

[4] S. D'Arco, L. Piegari, and P. Tricoli, "A modular converter with embedded battery cell balancing for electric vehicles," in *Proc. Electr. Syst. Aircraft, Railway Ship Propulsion*, Oct. 2012, pp. 1–6.

[5] L. M. Tolbert and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, Jan. 1999.

[6] L. M. Tolbert, T. Cunnyngham, and J. N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[7] S. D'Arco, M. Quraan, P. Tricoli, and L. Piegari, "Low frequency operation of modular multilevel converters with embedded battery cells for traction drives," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, Jun. 2016, pp. 1375–1382.

[8] S. D'Arco, L. Piegari, M. S. Quraan, and P. Tricoli, "Battery charging for electric vehicles with modular multilevel traction drives," in *Proc. 7th IET Int. Conf. Power Electron., Mach. Drives*, Apr. 2014, pp. 1–6.

[9] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2041–2051, Mar. 2017.

[10] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 507–517, Jan. 2016.

[11] D. Fabiani and G. C. Montanari, "The effect of voltage distortion on ageing acceleration of insulation systems under partial discharge activity," *IEEE Electr. Insul. Mag.*, vol. 17, no. 3, pp. 24–33, May 2001.

[12] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Implementation of nearest level modulation for modular multilevel converter," in *Proc. IEEE 6th Int. Symp. Power Electron. Distrib. Gener. Syst.*, Jun. 2015, pp. 1–5.

[13] M. Guan, Z. Xu, and H. Chen, "Control and modulation strategies for modular multilevel converter based HVDC system," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2011, pp. 849–854.

[14] A. Marquez, J. I. Leon, S. Vazquez, L. G. Franquelo, and M. Perez, "A comprehensive comparison of modulation methods for MMC converters," in *Proc. 43rd Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2017, pp. 4459–4464.

This is the accepted version of an article published in IEEE transactions on power electronics
http://dx.doi.org/10.1109/TPEL.2020.2969375

[15] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 297–310, Jan. 2015.

[16] M. S. Rajan and R. Seyezhai, "Comparative study of multicarrier pwm techniques for a modular multilevel inverter," *Int. J. Eng. Technol.*, vol. 5, no. 6, pp. 4850–4865, Jan. 2014.

[17] A. D. Pizzo, M. Coppola, and I. Spina, "Current waveforms distribution among electrochemical cells of modular multilevel converters in battery electric vehicles," in *Proc. IEEE Int. Conf. Elect. Syst. Aircr., Railway, Ship Propulsion Road Vehicles Int. Transp. Electrific. Conf.*, Nov. 2018, pp. 1–4.

[18] G. Brando, A. Dannier, I. Spina, and P. Tricoli, "Integrated BMS-MMC balancing technique highlighted by a novel space-vector based approach for BEVs application," *Energies*, vol. 10, Oct. 2017, Art. no. 1628.

[19] S. D'Arco, L. Piegari, and P. Tricoli, "Power and balancing control considerations on modular multilevel converters for battery electric vehicles," in *Proc. 15th Eur. Conf. Power Electron. Appl.*, Sep. 2013, pp. 1–9.

[20] G. B. Diaz, M. Boyra, and J. Vivas, "Novel control strategies for modular multilevel converters (MMC) - an evaluation and comparison of control and modulation schemes," in *Proc. Cigre Int. Symp. "Electric Power Syst. Future*," Sep. 2011.

[21] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[22] Y. Liang and C. O. Nwankpa, "A new type of statcom based on cascading voltage source inverters with phase-shifted unipolar spwm," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 33d IAS Annu. Meeting*, Oct. 1998, vol. 2, pp. 1447–1453.

[23] I. Ourdani, A. Bennani Ben Abdelghani, I. Slama Belkhodja, and D. Montesinos Miracle, "Phase opposition disposition PWM strategy and capacitor voltage control for modular multilevel converters," in *Proc. Int. Conf. Recent Adv. Electr. Syst.*, 2016, pp. 208–213.

[24] D. De Simone, L. Piegari, and S. D'Arco, "Comparative analysis of modulation techniques for modular multilevel converters in traction drives," in *Proc. Int. Symp. Power Electron., Elect. Drives, Autom. Motion*, Jun. 2018, pp. 593–600.

[25] J. Li and H. Hong, "Wthd optimization for single phase multilevel converters with step modulation," in *Proc. 37th Annu. Conf. IEEE Ind. Electron. Soc.*, Nov. 2011, pp. 4463–4468.

[26] D. Graovac, M. Pürschel, and A. Kiep, "Mosfet power losses calculation using the data-sheet parameters," Infineon Tecnologies AG, pp. 1–22, Jul. 2006.

[27] F. Bertoldi, M. Pathmanathan, R. S. Kanchan, K. Spiliotis, and J. Driesen, "Quasi-two-level converter for overvoltage mitigation in medium voltage drives," in *Proc. Int. Power Electron. Conf.*, May 2018, pp. 488–494.

[28] B. Diong, H. Sepahvand, and K. A. Corzine, "Harmonic distortion optimization of cascaded h-bridge inverters considering device voltage drops and noninteger DC voltage ratios," *IEEE Trans. Ind. Electron.*, vol. 60, no. 8, pp. 3106–3114, Aug. 2013.

[29] R. T.-Asl and J. Bauman, "Efficiency analysis of induction motor control strategies using a system-level EV model," in *Proc. IEEE Transp. Electrific. Conf. Expo.*, Jun. 2019, pp. 1–6.

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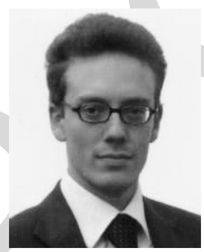

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