

Research Article

Silicon Powder-Based Wafers for Low-Cost Photovoltaics: Laser Treatments and Nanowire Etching

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In this study, laser-treated polycrystalline Si (pc-Si) wafers, fabricated by wire sawing of hot-pressed ingots sintered from Si powder, have been investigated. As-cut wafers and those with high-quality thin Si layers deposited on top of them by e-beam have been subjected to laser irradiation to clarify typical trends of structural modifications caused by laser treatments. Moreover, possibility to use laser-treated Si powder-based substrates for fabrication of advanced Si structures has been analysed. It is established that (i) Si powder-based wafers with thicknesses $\sim 180 \mu\text{m}$ can be fully (from the front to back side) or partly (subsurface region) remelted by a diode laser and grain sizes in laser-treated regions can be increased; (ii) a high-quality top layer can be fabricated by crystallization of an additional a-Si layer deposited by e-beam evaporation on top of the pc-Si; and (iii) silicon nanowires can be formed by metal-assisted wet chemical etching (MAWCE) of polished Si powder-based wafers and as-cut wafers irradiated with medium laser power, while a surface texturing on the as-cut pc-Si wafers occur, and no nanowires can form in the region subject to a liquid phase crystallization (LPC) caused by high-power laser treatments.

1. Introduction

Crystalline silicon (c-Si) wafer-based solar cells contribute to over 90% of commercial photovoltaic (PV) devices at present [1] and will be dominant in the foreseeable future due to the mature technology. Most of the silicon-based solar cells are made from single crystalline or multicrystalline wafers produced by Cz-growth and block casting from costly purified solar grade silicon. The ingots must be subsequently cut into wafers by wire sawing, and the damaged surface layer has to be removed by polishing.

As a result, around 50% of purified solar grade silicon will be lost due to the wafer sawing and subsequent processing [2], in the form of Si kerf (powders) in the sawing waste or in the slurry during the polishing of the wafers, that corresponds to approximately 200,000 tons out of the 400,000 tons of solar grade silicon consumed for solar cell production in 2016 [1, 3].

Therefore, several dicing-free approaches to overcome problems related to Si kerf losses have been proposed [4]. Among them, fabrication of silicon wafers by sintering of silicon powders using hot pressing [5] followed by zone melting recrystallization [6, 7], which is similar to earlier proposed direct growth of silicon sheets (SSP) from compacted silicon powders with a halogen heat source [8], can be considered as one of the promising approaches. However, the disadvantage of the above-mentioned Si powder-based concept is that sintered wafers are quite thick ($\sim 300\text{-}500 \mu\text{m}$), and as a result, consumption of Si is still quite high and comparable with that of conventional Si wafers fabricated by wire sawing of Si ingots. An alternative approach, which is based on ingots fabricated from sintering of Si powders, followed by slicing of wafers using a wire sawing process has been proposed recently [9] and provides a possibility to process Si powder-based wafers with thicknesses below $200 \mu\text{m}$. However, production of Si kerf, similar to that of a conventional Si

wafer-based approach, occurs in this case as well. Taking into account that purification of Si kerf allows to use purified material for a conventional block casting process [10, 11], it can be expected that Si powders processed from the purified Si kerf by milling can be used for the cost-effective fabrication of sintered Si powder-based wafers. Such approach can be considered as a cost-effective, circular economical solution for an advanced low-cost Si-based PV.

Moreover, another source of silicon feedstock, which can be used to produce high-quality Si powders by milling, comes from microelectronics, which discharge several thousand tons per annum (tpa) of silicon IC waste [12]. In addition, considering that already installed solar modules will reach their end-of-life stage in approximately 30 years after the installation, it is expected that silicon waste from the recycled solar modules is a continuously growing source of solar grade Si feedstock and will alone provide 88,000 and 207,000 tpa by 2040 and 2050, respectively [2]. Important to note that Si extracted from the end-of-life modules or broken solar cells has a doping level adjusted for the processing of good-quality solar cells. Although some efforts to extract such Si feedstock are still required, this process is feasible and can be realised in a cost-effective way [13].

It is therefore of huge economic and environmental advantages, if the above-mentioned Si feedstock from different sources of Si-based wastes can be used for the needs of an advanced Si-based PV after appropriate purification of such feedstock and its conversion into Si powders.

It can be concluded that Si powder-based concepts targeting on utilisation of solar grade Si powders, fabricated from different sources of Si feedstock, have strong background and reasons to be developed further, taking into account the above-mentioned arguments.

Si powder-based wafers can be used for the needs of an advanced Si-based PV by three main routes: (i) to produce Si powder-sintered wafer-based solar cells if the quality is sufficient; (ii) to serve as supporting substrates for solar cells either bonded on top of them [14, 15] or fabricated directly on such polycrystalline Si (pc-Si) wafers; and (iii) to fabricate Si-based structures in the frame of an advanced concept which allow to use low-grade (or defective) silicon wafers to process radial junction (core-shell) nanowire solar cells, in which the generated minority carriers have to be drifted to a very short path (tens of nm in the range of the radii of the nanowires) to be collected by the emitter. Moreover, the core is mostly depleted so that the defects are empty (no carriers are trapped at the defects), so that almost no Shockley-Read-Hall recombination takes place in the core even if it is very defective. As a result, very low-grade silicon materials can be used to produce solar cells [16–18].

It should be noted that apart from the compacting of Si powders, the common issue in the above-mentioned Si powder-based approaches (SSP and hot pressing) is a need for the recrystallization of such substrates. In the case of Si powder-based wafers processed by wire sawing of sintered ingots, such recrystallization is required as well, since the size of Si grains is defined by the size of initial Si powders (1–100 μm), and therefore, grains should be enlarged to get better quality of the final polycrystalline (pc) material.

In this study, following the above-mentioned three routes, we have demonstrated some progress towards fabrication of relevant advanced Si powder-based structures using laser treatments to modify their properties.

In particular, pc-Si wafers, fabricated by wire sawing of the hot-pressed ingots from Si powders, as well as Si powder-based structures processed by e-beam deposition of high-quality Si layers on top of such wafers, were subjected to laser irradiation to clarify typical trends of structural modifications of such structures. Moreover, possibility to use laser-treated Si powder-based substrates for fabrication of advanced Si structures has been analysed.

All the pc-Si powder-based wafers were produced from solar grade p-type silicon powders with a doping level of $\sim 10^{16} \text{ cm}^{-3}$ in this study, which have been prepared by ball milling of wafers and sieving techniques.

2. Experimental Results and Discussion

2.1. Laser Recrystallization to Improve the Material Quality.

The wire-sawn pc-Si wafer produced from silicon powders was fixed between two glass substrates by Ag paste, so that the to-be-treated area is free-standing bridging between the glass substrates as shown in Figure 1(a), and this setup is advantageous to minimize heat transfer onto the glass substrates. In this case, the glass keeps solid even if the temperature at the laser-treated area is above the melting point of silicon (1414°C). The thickness of the wafer is $170 \pm 10 \mu\text{m}$. In this work, we use a diode laser working at a wavelength of 808 nm, which is commonly used to crystallize Si thin films on glass [19]. It is possible to melt the whole piece of the pc-Si wafer fully from the front to the back side, and a substrate temperature of 600°C was used to reduce the thermal stress during the solidification. Figure 1(a) demonstrates pc-Si wafers treated with a laser power density of 15.0 (upper case) and 13.5 kW cm^{-2} (lower case) at a scan speed of 10 mm s^{-1} . A complete melt of the whole pc-wafer can be achieved at 15.0 kW cm^{-2} , and at some positions, the liquid Si even flows down on the sample stage as indicated by the arrow of the upper wafer piece. By lowering the laser power density to 13.5 kW cm^{-2} , a melt of the pc-Si wafer occurs while no downflow of the liquid Si takes place. The surface of pc-Si wafer pieces exhibits mirror-like properties at the irradiated regions as shown in Figure 1(a) while the nonirradiated regions appear greyish. A smoothing of the surface can also be seen in a tilted (70°) SEM image in Figure 1(b), which was taken at a cross section of a sample irradiated at a laser power density of 13.5 kW cm^{-2} . However, some microdefects such as grown-up protrusions and microvoids on the surface and in the volume have been detected by SEM measurements in Figures 1(c) and 1(d). Although some microvoids are found in the volume, they are not the same as observed on the surface. The recrystallization shows clear characteristic of liquid phase crystallization (LPC) [20] at the power density level of $13.5\text{--}15.0 \text{ kW cm}^{-2}$, which have been monitored by the optical reflection using a control laser measured at the scan front, where a highly reflecting surface is the characteristic for the materials above the melting temperature [20].

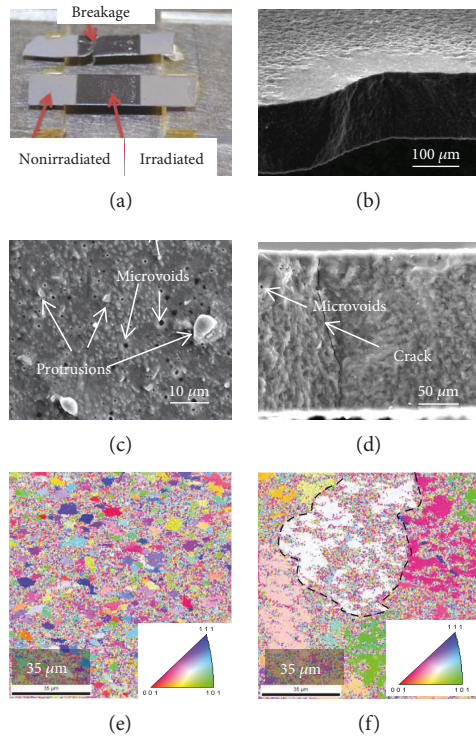


FIGURE 1: (a) Photograph of the samples irradiated by the laser at 15.0 (upper case) and 13.5 kW cm^{-2} (lower case) at a scan speed of 10 mm s^{-1} ; (b) SEM image (70° tiled) at the cross section with a rough surface of the nonirradiated region and the smooth laser-recrystallized region; (c) surface morphology of the laser-recrystallized region showing examples of protrusions and microvoids on the surface; (d) a crack induced by the laser recrystallization process and microvoid in the volume; (e) top-view EBSD image of the as-cut pc-Si sample; (f) top-view EBSD image of the laser-recrystallized (at a power density of 13.5 kW cm^{-2}) pc-Si sample.

Crack formation is an issue for the LPC process due to high stress originating from the high temperature gradient during the solidification [21]; it starts within the top layer and spreads to the volume of the pc-wafer as indicated by the arrow in Figure 1(d). Such crack formation sometimes leads to breakage of the wafers; therefore, a substrate temperature of 600°C was used to reduce the thermal stress.

A significant difference between the nonirradiated and laser-recrystallized (with a laser power density of 13.5 kW cm^{-2} at a scan speed of 10 mm s^{-1}) regions can be clearly detected by the top-view electron backscatter diffraction (EBSD) measurements. In particular, the nonirradiated pc-Si wafer shows few grains with a size of about $10 \mu\text{m}$ embedded in a large amount of small grains as shown in Figure 1(e), whereas the recrystallized region shows substantial growth of large grains up to $50 \mu\text{m}$ (Figure 1(f)). For the visualization, in Figure 1(f), an enlarged grain is circled by the dashed line (the dashed line is just a guide and not an accurate grain boundary). It can be seen that enlarged grains are in contact with each other and densely packed. The image noise within single enlarged grains may probably originate from the microdefects (protrusions and microvoids) on the surface.

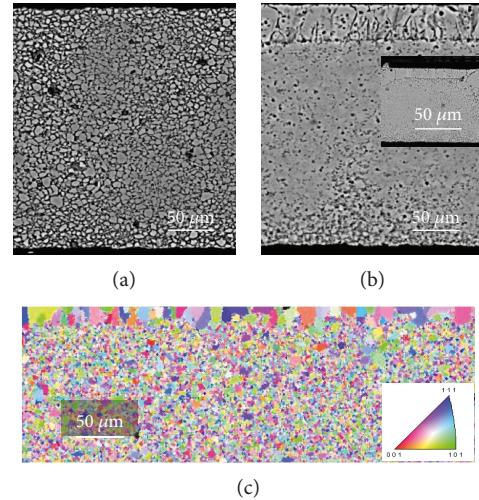


FIGURE 2: (a) SEM cross section image of the as-cut pc-Si sample subject to a polishing; (b) SEM cross section image of the laser-crystallized pc-Si sample (at a power density of 13.5 kW cm^{-2}) and the inset showing another region; (c) cross-sectional EBSD mapping of the laser-recrystallized pc-wafer (at a power density of 13.5 kW cm^{-2}).

A cross-sectional morphological study of the as-cut pc-Si sample as well as of another sample subjected to a laser scan at 13.5 kW cm^{-2} has been performed. Both samples were embedded in an epoxy resin and subsequently polished and ion-milled (in order to prevent charging of the epoxy) prior to the EBSD measurements. The cross-sectional SEM image of the as-cut pc-Si sample in Figure 2(a) shows similar crystal size distribution as indicated by the top-view EBSD image in Figure 1(e). However, the cross section of the laser-recrystallized pc-Si sample (in Figure 1(f)) clearly shows a top layer with larger grains with a thickness of $25\text{--}30 \mu\text{m}$, which extends up to $60 \mu\text{m}$ into the bulk in some positions (see the inset in Figure 2(b)). EBSD measurement has been performed at the cross section of the laser-recrystallized sample as shown in Figure 2(b), and large grains with sizes in the range of $20\text{--}30 \mu\text{m}$ can be clearly seen in the subsurface area of the laser-treated side (Figure 2(c)). This result is in a good agreement with the results of the cross-sectional SEM (Figure 2(b)) and the top-view EBSD (Figure 1(f)) measurements.

It is demonstrated that the wire-sawed pc-Si wafers produced from silicon powder can be recrystallized by a high-power diode laser scan, the grain size in the top layer can be significantly enlarged through the LPC mechanism, and the conductivity of the laser-treated pc-Si-based structures can be improved, which can be attributed to the growth of a larger grain as well as to an improved crystallinity.

2.2. Laser Crystallization of an Additional a-Si Layer Deposited on Top of the pc-Si Wafer. The second route, mentioned above, supposes to use low-cost pc-Si wafers as supporting substrates as well as a conductive back contact. In the frame of such approach, a high-quality Si layer (solar cell grade) has to be fabricated on top of the supporting pc-Si wafers. In this study, a high purity $10 \mu\text{m}$ a-Si layer was

deposited on top of the pc-Si wafers by the e-beam evaporation. An n -type doping of $\sim 6 \times 10^{16} \text{ cm}^{-3}$ of the a-Si layer was achieved by heating an effusion cell with a phosphorus source during the deposition, as determined by our previous systematic investigation at the same deposition condition.

In order to prevent the pc-Si wafers from breakage, the crystallization of the a-Si layer was performed at reduced power of 11.0 up to 12.0 kW cm^{-2} while keeping the scan speed of 10 mm s^{-1} and substrate temperature at 600°C . At these reduced power density levels, a crystallization of the top a-Si layer occurs through the solid phase crystallization (SPC) instead of the LPC mechanism, as confirmed by the optical reflection measurement through a control laser at the scan front [20], because the SPC does not show substantial change of the surface reflection during the crystallization. It is noted that laser crystallization at higher power densities between 13.5 and 15.0 kW cm^{-2} leads to immediate crack formation and breakage of the wafers, and this is much frequently happening than those laser recrystallization processes performed on the as-cut pc-Si wafers. This is probably because of the stress that was already induced by the additional a-Si layer.

The crystallized top layer got slightly smoothed, though, not like the one subject to laser recrystallization of the whole wafer. Figure 3(a) shows a SEM image (sample is 70° tilted) at the cross section. The corresponding higher magnification SEM image in Figure 3(b) shows the morphology of the surface after the laser-induced SPC process. No substantial protrusions have been detected on top of the crystallized a-Si layer. Figure 3(c) shows the boundary (step) between two regions—the region with deposited $10 \mu\text{m}$ a-Si (left side) and that without a-Si (right side) after laser treatment.

The EBSD image in Figure 3(d) shows that most of the grains have size around $10 \mu\text{m}$, in the range of the a-Si layer thickness, which is typical for the SPC process.

2.3. Nanowire Etching for Core-Shell Solar Cells. Nanowire core-shell solar cells, the so-called radial junction, have the advantages that allow to produce high-efficiency solar cells using low-grade silicon material [16, 22]. This is due to the fact that light absorption [23] will be significantly enhanced by light trapping of the densely packed nanowire array [24]. Additionally, the carrier recombination in the bulk will be greatly reduced because of the short collection path of the generated carriers [16, 22, 25], which is only in the range of the radii of the nanowires. Moreover, the core is mostly depleted so that the defects are empty (no carriers are trapped in the defects); therefore, almost no Shockley-Read-Hall recombination takes place in the core even if it is very defective. As a result, very low-grade silicon materials can be used to produce solar cells.

The core-shell nanowire solar cell concept fits very well with the low-cost pc-Si wafers produced from silicon powder, so the nanowire etching on these wafers is a prerequisite for this advanced concept.

In this study, one-step and two-step metal-assisted wet chemical etching (MAWCE) processes have been performed on the pc-Si wafers. All the wafers have been cleaned by

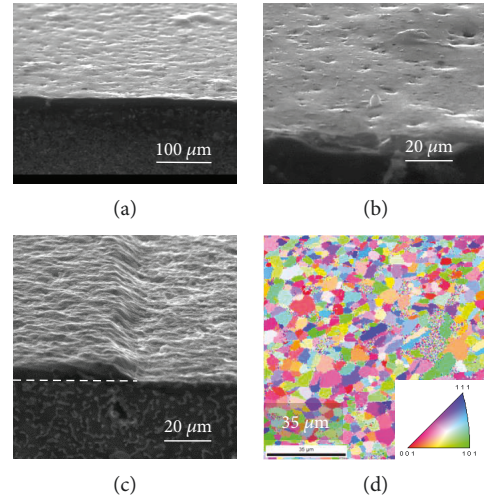


FIGURE 3: (a) SEM image (sample is 70° tilted) of the laser-crystallized thin e-beam-deposited Si layer at the cross section; (b) the corresponding higher magnification SEM image; (c) the boundary at the region deposited with $10 \mu\text{m}$ a-Si (left side) and that without a-Si (right side) after laser crystallization, the dashed line indicated the boundary between the additional layer and the pc-wafer; (d) EBSD image of the laser-crystallized thin e-beam-deposited Si layer on top of the pc-Si wafer.

acetone and subsequent isopropanol to remove surface contamination prior to the etching. All the etching has been done at room temperature. The cleaned wafers were etched in a AgNO_3 (0.02 M): HF (5 M) solution (one-step etching) for the etching of nanowires corresponding to an etching rate of about 30 nm min^{-1} . The two-step etching was done by immersion of the wafers in the AgNO_3 (0.02 M): HF (5 M) solution for 30 s to deposit Ag nanoparticles on the surface as the first step. Then the second step was performed in a HF (5 M): H_2O_2 (30%) solution [26, 27] with a volume ratio of 20:1. Here, the etching rate is much faster at about 300 nm min^{-1} and one order of magnitude higher than the one-step etching. In both cases, the Ag nanoparticles were etched away afterwards by concentrated HNO_3 (65%) for 10 min followed by deionized water rinsing.

The etching of nanowires on the as-cut pc-wafers using the above-described two methods has failed independently of the etching time. The etching produces rather a surface texturing as shown in the SEM image in Figure 4(a) and the corresponding higher magnification SEM image in Figure 4(b). Some nanofeatures can be seen between the textures as shown in the insets of Figure 4(b) (regions marked with red rectangles).

On polished pc-Si wafers, a very homogeneous nanowire array can be etched. The vertically densely packed nanowire array can be obtained despite the different crystal orientation. This result is comparable with the etching on high-quality pc-Si wafers and thin films. Figure 4(c) and the corresponding higher magnification SEM images show an example of nanowires etched on the polished pc-Si wafers by the two-step process. The duration of the second step was 5 min, and the length of the nanowires is about $1.5 \mu\text{m}$.

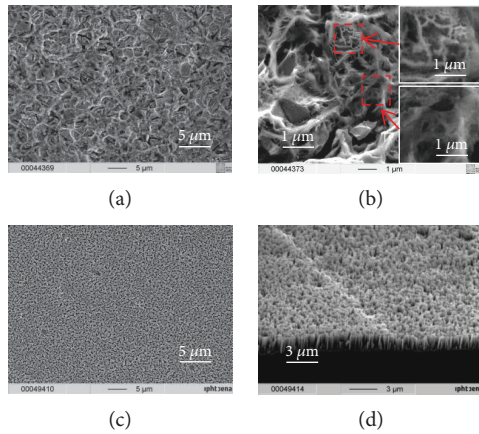


FIGURE 4: (a) Surface texturing of the as-cut pc-Si wafers subject to a MAWCE; (b) higher magnification SEM image of the surface texture showing nanofeatures (examples in the insets are shown in the regions marked with red rectangles); (c) densely packed nanowires formed after the two-step MAWCE on polished wafers; (d) vertically orientated silicon nanowires etched by the two-step MAWCE process.

Both nanowire etching processes have been applied on the pc-Si wafers after the laser recrystallization process. Here, it shows different behaviors in regions treated with different laser powers. pc-Si-based structures treated with different laser powers at 12.0 and 13.5 kW cm^{-2} have been tested for the nanowire fabrication process. Moreover, a reference pc-Si sample is placed on the heater along with the samples to be laser treated (the pc-Si samples were heated up to 600°C in about 2 hours, but no laser treatment has been performed on the reference). The two-step MAWCE was performed on the pc-Si samples, in which the duration of the first etching keeps unchanged at 30 s, and the second etching took 10 min.

It has been found that nanowires could not be etched as before for the reference sample without laser treatment. Instead, a surface texturing occurs as shown in the SEM image in Figure 5(a), (A) and in the corresponding higher magnification SEM image in Figure 5(a), (B). However, the textures are quite different with those generated on the as-cut pc-Si wafers shown in Figures 4(a) and 4(b). No nanofeatures and only grains with sharp edges can be seen in this case. This change in the structure compared to the as-cut pc-Si wafer may closely relate to the thermal process during the laser crystallization, indicating that some solid-state transformation has happened at the process temperature even without laser scanning.

It was established that Si nanowires can be etched on the region treated with medium laser power of 12.0 kW cm^{-2} , and this region appears greyish similar to the as-cut wafer, though, with a laser track, which underwent a SPC crystallization. The SEM image in Figure 5(b), (A) and the corresponding higher magnification SEM image in Figure 5(b), (B) show deep and dense nanowires prepared in this region by a two-step MAWCE, where the first step is kept 30 s and the second step for 10 min.

On the region treated with a higher laser power of 13.5 kW cm^{-2} , the surface is mirror smooth after the LPC process initiated by the laser scan, and no nanowire can be

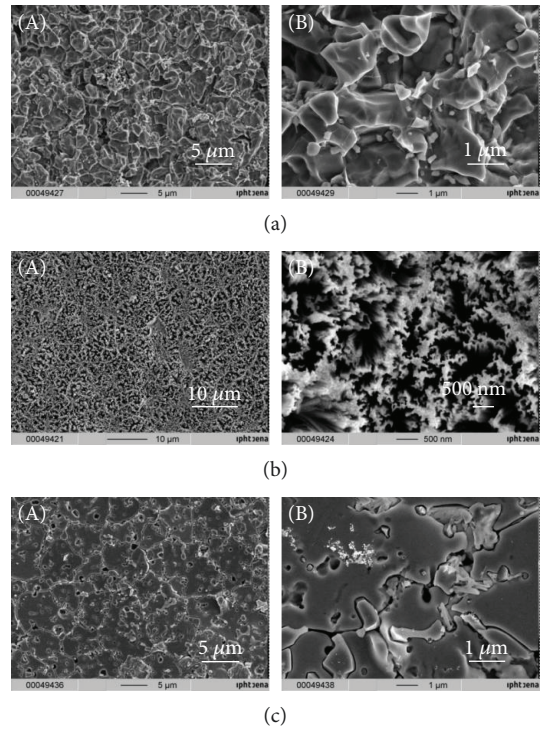


FIGURE 5: (a), (A) SEM image showing the surface textures of the nonirradiated pc-Si sample (only heat up to 600°C for about 2 h without laser treatment) subject to a MAWCE process and (a), (B) the corresponding higher resolution SEM image; (b), (A) nanowires formed by MAWCE in the region treated with medium laser power density of 12.0 kW cm^{-2} and (b), (B) the corresponding higher resolution SEM image; (c), (A) no nanowires being detected in the region treated with a laser power density of 13.5 kW cm^{-2} and (c), (B) the corresponding higher resolution SEM image.

etched by both methods. In this case, the surface looks visually untouched after the etching. The typical surface structure of the laser-recrystallized regions after the two-step etching (duration of second step is 5 min) is shown in Figure 5(c), (A) and the corresponding higher magnification SEM images in Figure 5(c), (B). It can be clearly seen that some small grains are embedded in large grains, and the “grain boundaries” were etched away completely, leaving behind hollow “boundaries” between neighboring grains. This behavior is quite different compared to previous results obtained for a multicrystalline Si (mc-Si) thin film deposited on glass, EFG-grown thin mc-Si wafers and low-cost mc-Si wafers [28], where the grain boundaries remain after the nanowire etching. It can be assumed that silicon oxide may exist on the surface of Si powders which have been used for the hot pressing. Moreover, it is supposed that an oxide layer is sandwiched between the neighboring grains after the hot pressing sintering as well as after the laser recrystallization processes. In this case, such oxide layer can be etched away by the HF during the nanowire etching, which results in the formation of a hollow “grain boundary” structure. To verify the above-discussed assumptions, more detailed analysis of interfaces of Si powder-based structures, as well as an optimization of the hot pressing process, is required. The observed small grains embedded in the larger

grains could be a result of the oxide shell, which does not allow for Si powders to be merged.

It is still unclear if what causes the difference between the as-cut and the polished pc-wafers for the results of nanowire etching, supposed that there is a defective surface layer on the pc-Si wafers after the wire sawing, which will disturb the MAWCE, and this defective layer will be removed by polishing, so that the nanowires can be etched on the polished pc-Si wafer. This explanation is consistent with the results observed on the samples treated with laser, where a defective surface layer is induced after a LPC process at laser power at 13.5 kW cm^{-2} due to the rapid quenching at the surface region, while the SPC process treated at laser power at 12.0 kW cm^{-2} will heal some of the defects, so that the surface gets improved, which allow the MAWCE. The latter case could be applied for the annealed reference sample, in which some solid phase transformation happens at the surface region, which will heal the defects at the surface region to a certain extent but not enough to allow triggering the MAWCE. However, this explanation should be tested with further experiments including structure analysis by transmission electron microscope.

3. Conclusion

The following trends of the structural modifications of pc-Si-based structures caused by laser treatments have been established:

- (i) Wire-sawed pc-Si wafers produced from silicon powder can be recrystallized by a high-power diode laser scan, and the grain size in the top layer can be enlarged through the LPC mechanism
- (ii) The a-Si layer deposited by the e-beam evaporation on top of the pc-Si wafers can be crystallized by the diode laser scan. However, a breakage-free crystallization can only be achieved by a SPC-based process
- (iii) No nanowires can be etched on the as-cut pc-Si wafers. Instead, a surface texturing of such pc-Si occurs
- (iv) Nanowires can be etched on polished pc-wafers as well as in the regions treated with the medium level laser power
- (v) Crack formation of the pc-Si wafers occurs during the laser scan and has to be investigated in order to obtain large-area crack-free wafers, and the laser parameters such as power, scan speed, focus, and the substrate temperatures require careful optimizations

Data Availability

The data used to support the findings of this study are available from the corresponding author upon request.

Conflicts of Interest

The authors declare that there are no conflicts of interest regarding the publication of this paper.

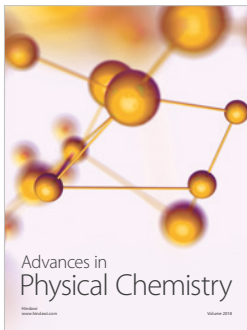
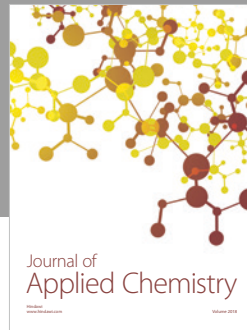
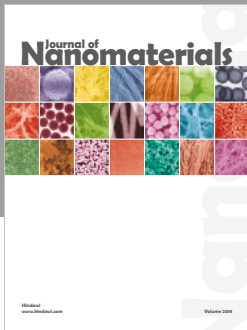
Acknowledgments

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