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Review of technologies for DC grids – power conversion, flow control and protection

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Grain Philip Adam[1] ✉, Til Kristian Vrana[2], Rui Li[1], Peng Li[3], Graeme Burt[1], Stephen Finney[4]

[1]*University of Strathclyde, UK*
[2]*SINTEF Energi, Norway*
[3]*University of Aberdeen, UK*
[4]*University of Edinburgh, UK*
✉ *E-mail: grain.adam2010@gmail.com*

Abstract: This study presents a comprehensive review of dc transmission technologies for future power grids, with particular emphasis on the attributes of the system components that could enhance system controllability and stability, resiliency to ac and dc network faults (fault-tolerant operation) and encourage increased exploitation of renewable energy resources for power generation. A detailed discussion of ac–dc and dc–dc converters show that the self-commutated dc transmission system technologies are critical for better utilisation of large renewable energy resources which are dispersed over wide geographical areas while offering the control flexibility needed for proper operation of centralised and decentralised power grids. It is concluded that besides dc voltage matching and power control, the use of expensive and high loss isolated dc–dc converter could be justified in exceptional cases and as part of overall protection systems to prevent dc fault propagation, by splitting large multi-terminal dc networks into several isolated protection zones. Cheaper non-isolated dc–dc converters could be used for dc voltage tapping and matching and power regulation in less critical power corridors, where the loss of control for short periods will not lead to catastrophic impact on system stability (all non-isolated dc–dc converters are unable to prevent a ground potential shift in symmetrical monopole systems). All hybrid dc circuit breakers (DCCBs) to date are aimed for fast dc fault isolation, within 3–5 ms, while the majority of resonance-based DCCBs with forced current zeros are aimed for relatively slow dc fault clearance times, ranging from 8 to 12.5 ms in an attempt to reduce the cost compared with the former type. Series-type dc power flow controllers offer the cheapest way to optimise power flow in highly meshed dc networks.

1 Introduction

Renewable power generation has increased substantially in all major developed and developing countries, presenting significant challenges to grid operators at generation, transmission and distribution levels. Some of these challenges can be summarised as follows [1–6]:

- Wide spread uses of high-voltage dc (HVdc) links and wind generators with fully rated back-to-back converters deprive ac grids of the contribution of the generators' rotating inertias to damping of low-frequency power oscillations following major ac network disturbances.
- Intermittent nature of renewable energy resources exacerbates the problems of power balance and poor utilisation of the ac lines due to undesirable power flow in ac power systems with high penetration of renewable power generation.
- Operation of power electronic-based solar and wind generators, which are less sensitive to frequency variation (±2.5 Hz) alongside the frequency sensitive large conventional synchronous generators, render most existing protection philosophies inadequate. This is because the stability margins of the latter dictate the overall stability of the entire power system, leading to unnecessary loss of generation or tripping of conventional power plants due to loss of synchronism.

Some of these challenges could be addressed with well-designed smart grids that employ both ac and dc transmission systems with state-of-arts control and communication systems, where the vast energy stored in the dc lines and converters' cell capacitors of the asynchronous connections could be manipulated to mitigate the effect of renewable energy resources variability on power quality, and improve transient stability by splitting large ac power systems into several independent asynchronous ac protection zones in order to prevent ac fault propagation throughout the system [4, 5, 7]. In this manner, conventional synchronous and doubly fed induction generators can contribute to power oscillation damping in their respective zone alongside the synthetic inertia from the capacitors of asynchronous links. The trend of data driven power consumption at lower distribution systems of smart grids (380–415 V) may require agile generation and transmission system infrastructures which are able to cope with rapid change in power demand, mainly driven by electricity prices, consumer behaviour and other autonomous smart devices for demand-side management [8–11]. To avoid poor utilisation of the generation and transmission infrastructures in data drove smart grids, fast and secure communication systems capable of dealing with large data and a number of high-level controllers will be required to optimise the power flow at the transmission level. This flow optimisation can be done with:

- converter terminals of the HVdc interconnectors;
- embedded HVdc links within some of the ac protection zones;
- flexible ac transmission system (FACTS) devices; and
- HV dc–dc converters, which manage the power flow in meshed parts of the dc infrastructure.

Instead of the present large centralised power grids, centralised operation of large smart grids that spread over wide areas such as Europe, USA, China and India are necessary for better utilisation of the diversity of renewable energy resources across different regions; thus, leading to provision of cheap, reliable and sustainable power throughout all four seasons of the year. In this manner, power plant types which are operated with fixed output power such as nuclear and other fossil fuel-based plants could be reduced [10, 12–17]. In contrast, the planned transition of smart grids from centralised to decentralised operation could be executed during major network faults or outages of the critical power corridors, with no or minimum loss of power supply, provided the

said ac protection zones are designed to be self-contained (each must be able to satisfy the grid code as an independent ac network). In being able to operate in centralised and decentralised modes, smart grids have the potential to avoid the problem of total system blackout.

The multi-terminal HVdc transmission network concept is attractive to many transmission system operators, and for future smart grids because of the following reasons:

- real power can be exchanged over a wide geographical area at reduced transmission power loss;
- increased control flexibility over power flow (magnitude and direction) using a reduced number of converters and dc cables (hence, offers a cost-effective solution);
- dc line conductor cross-section areas are fully utilised for carrying real power (no parasitic current or reactive current); and
- dc line loadability is not limited by its surge impedance loading as in equivalent ac lines, and dc lines are magnetic field neutral (less harmful to nearby wildlife and sea creatures).

However, because of low resistance and rapidly diminishing effect of the line inductance during a dc short-circuit fault, the speed of dc fault propagation is much faster than an ac fault. Also, because of the dc fault current increases rapidly within the first 3 ms of the fault initiation, the dc short-circuit fault has to be interrupted within an ac sub-fundamental cycle to avoid irreparable damage to expensive and vulnerable part of the dc network such as power converters. Recently, significant effort has been invested in the development of new types of power converters that do not increase the fault level in the dc network and can survive dc faults for extended periods (several milliseconds without the risk of damage). This has been done in an attempt to relax dc circuit breakers (DCCB) requirements (in terms of let-through current, current breaking capacity and operating speed). Although some of the emerged converters and DCCBs are designed to cope with the high demands of dc faults, most of these circuit breakers require a number of sizable extra dc inductors to be incorporated into the dc link or converter control modification to slow down the rate of rise of the dc fault current at the dc link of each converter and rate of fall of the dc-link voltage or actively control the fault current [1, 3, 10, 18, 19]. Research is needed into protection aspects related to fault detection and discrimination and in coordination between ac and dc sides, protection to avoid catastrophic outcomes of miss-operation.

This discussion shows that besides complex control and communication systems, line and self-commutated FACTS devices and HVdc transmission systems and HVdc–dc converters are all critical in achieving the increased control flexibility expected from smart grids. Besides increased controllability, smart grids provide platforms to facilitate a cheap way to integrate many renewable power plants into power grids, without the need for energy storage systems, benefiting from the diversity of renewable energy resources in different regions. Therefore, this paper presents a comprehensive review of the transmission system technologies for smart grids, with a particular focus on components of dc transmission systems. Although a qualitative discussion is used as the main tool to articulate the attributes and limitations of different components or solutions, in general, and from a smart grid prospective, quantitative substantiation is used in a limited number of cases.

2 Modular multilevel AC–DC converters

Fig. 1 shows the modular multilevel converter (MMC) [20–27]. Each phase leg of the MMC comprises of upper and lower arms, and each arm consists of 'N' cascaded cells such as in Fig. 1, and must support the full dc-link voltage 'V_{dc}'. The voltage across each cell capacitor must be regulated around $V_{cell} = V_{dc}/N$ or $V_{cell} = V_{cref}/N$, depending on the control method employed. Correct operation of the MMC is achieved when each of phase leg inserts a sufficient number of cell capacitors into conduction path to counter the input dc-link voltage, and this imposes complementary operation of the upper and lower arms of the same phase leg according to the following insertion functions: $n_{a1}(t) = \frac{1}{2}N_1[\alpha_d - m\sin(\omega t + \delta)]$ and $n_{a2}(t) = \frac{1}{2}N_1[\alpha_d + m\sin(\omega t + \delta)]$, where $\alpha_d = V_{dc1}/V_{cref}$ is the dc modulation index; m is the ac amplitude modulation index; δ is arbitrary load angle; V_{cref} is the desired set-point for the sum of the cell capacitor voltages of each arm, and n_{a1} and n_{a2} are the number of cells to be inserted into the power path from the upper and lower arms at each instant. Instantaneous voltage across the upper and lower MMC arms are: $v_{a1} = n_{a1}(t) \times V_{cell} = \frac{1}{2}V_{cref}[\alpha_d - m\sin(\omega t + \delta)]$ and $v_{a2} = n_{a2}(t) \times V_{cell} = \frac{1}{2}V_{cref}[\alpha_d + m\sin(\omega t + \delta)]$ [18, 28]. Considering phase 'a' as an example, MMC terminal phase voltage (v_{ao}) at output 'a_o' relative to ground (O_1) represents the different-mode voltage of phase leg 'a' and is given by: $v_{ao1} = v_{a2} - v_{a1} = \frac{1}{2}mV_{cref}\sin(\omega t + \delta)$. During normal operation, V_{cref} is regulated around V_{dc}; thus, $\alpha_d \simeq 1$. This operation allows each MMC phase leg to present sufficient dc or common-mode voltage ($v_{a1} + v_{a2} \simeq \alpha_d V_{cref}$) to counter the input dc-link voltage (V_{dc1}), while maintaining a small voltage mismatch between the two voltages to allow the dc current flow; thus, power exchanges between the ac and dc sides. The arm inductor L_d in Fig. 1 limits the inrush current due to a mismatch between common-mode voltage and input dc-link voltage. This operation means the MMC is the only voltage-source converter (VSC), where the upper and lower arms of the same phase leg conduct simultaneously; with arms containing continuous ac and dc currents. The fundamental components of the arm currents are used to exchange active power between the converter and ac sides, while the dc components of the arm currents provide power transfer from the converter to the dc side [29]. When i_{a1} and i_{a2} are phase 'a' upper and lower arm currents as defined in Fig. 1, phase 'a' output current (i_{ao}) represents the differential-mode current ($i_{ao} = i_{a1} - i_{a2}$). The current component that circulates between the upper and lower arms of phase 'a', without reaching the output circuit, is denoted as common-mode current 'i_{com}' and is given by $i_{com} = (1/2)(i_{a1} + i_{a2})$. Without dedicated active or passive countermeasure, the MMC arm or common-mode currents may contain some parasitic components such as second-order harmonic current that could increase semiconductor losses and cell capacitor voltage ripple. The main attributes and drawbacks of MMCs are [20–27]:

- The MMC generates sinusoidal output voltages, with near-zero harmonics and extremely low-voltage stresses (dv/dt) on the interfacing transformer; thus, ac filters and phase interfacing reactors are not needed.
- Besides the known attributes of conventional VSCs {xx], the circuit structure of the MMC permits the power rated and dc operating voltage of VSC-HVdc links to be increased to a level comparable with that of conventional of line commutated converter (LCC)-HVdc links; and internal fault management, which is necessary for continued operation during cell failure (cell capacitors or switching devices). Moreover, the use of distributed cell capacitors in MMCs reduces the first peak (or transient component) of the let-though currents that may flow in the DCCB before its opening; thus, allowing DCCB design requirements to be relaxed.

However, the large footprint of the MMC due to the use of a large number of cell capacitors represents a major drawback from the scenery point of view and costs of right-of-way. The ratings for MMCs have reached 1000 MW and 525 kV [30].

The properties of the MMC highly depend on the internal structure of the utilised cells. The following sections give an overview of the most prominent proposed cell types.

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2.1 Half-bridge (HB) cell MMC

Fig. 2*a* shows an HB cell [23, 25, 26]. The HB cell MMC (HB-MMC) offers low semiconductor losses, which is in line with the decarbonisation efforts of transmission networks; however, it is subject to the same constraints of conventional VSCs such as operation with unipolar dc-link voltage and vulnerability to dc faults. All existing MMC-type HVdc links currently operational are HB-MMCs.

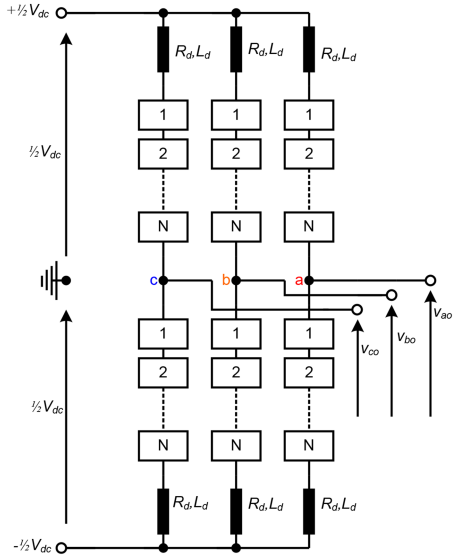

Fig. 1 *Schematic diagrams of the generic MMC*

2.2 Full-bridge cell MMC

Fig. 2*b* shows an FB cell. Although the Full-bridge cell MMC (FB-MMC) has high semiconductor losses, it offers dc fault reverse blocking capability; and operation with variable and bipolar dc-link voltage including zero dc voltage, while retaining full control over active and reactive power exchanges between converter ac and– dc sides [28, 31, 32]. This feature means the FB-MMC handles dc faults without the need to block the converter, while full control over the ac current in-feed from the ac side is retained. Additionally, bipolar dc voltage operation allows the FB-MMC to operate in a generic dc grid, side by side to line commutated converters (as the FB-MMC can change power flow direction with the change of dc current or dc voltage polarities). These attributes are expected to be invaluable in the delivery of increased control flexibility needed in smart grids.

FB-MMC technology has been proposed for an HVdc link with overhead lines in Germany: the ULTRANET project (±380 kV, 2 GW) [33]. The main reason for applying FB technology was better fault handling ability since the project uses overhead lines, where the likelihoods of dc faults are much higher compared with its counterpart with cables.

2.3 Doubled clamped cell MMC

Fig. 2*c* shows a three-level double clamped cell. Each cell of the doubled clamped cell MMC (DCL-MMC) is equivalent to two HB

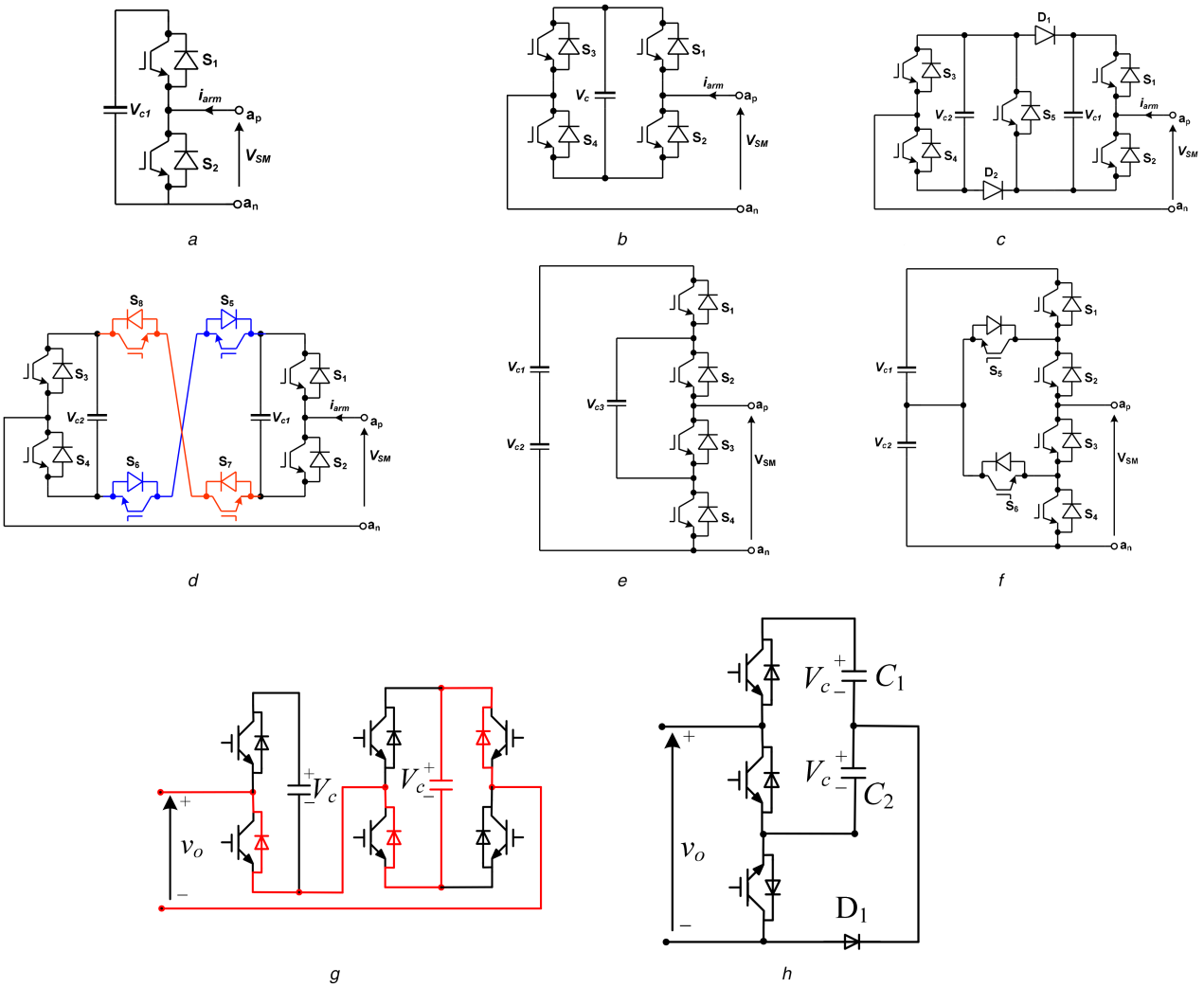

Fig. 2 *Examples of MMC cells*

(a) HB cell, ***(b)*** FB cell, ***(c)*** Three-level double clamped cell, ***(d)*** Symmetrical bipolar five-level cross-connected cell, ***(e)*** Three-level unipolar FC cell, ***(f)*** Three-level unipolar ANPC cell, ***(g)*** Hybrid or MC, ***(h)*** SC cell

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cells as it uses two capacitors and generates three viable voltage levels ($2V_c$, V_c and 0) provided the cell capacitor (C_1 and C_2) voltages are maintained such that $V_{c1} \simeq V_{c2} \simeq V_c$ (this is contrary to that explained in [34]). However, each double clamped cell in Fig. 2*c* inserts three semiconductor switching devices in the conduction path, instead of two switches with equivalent HB cells, but offers dc fault reverse voltage blocking capability, lacked in the HB-MMC. The main weaknesses of the DCL-MMC are:

- The inability of DCL cell to generate a negative voltage level for both polarities of arm current restricts its operation to unipolar dc-link voltages. Thus, it is unable to facilitate operation with a reduced dc-link voltage, unlike the mixed cells MMC (MCs-MMC).
- Activation of dc fault blocking capability [switching off all insulated-gate bipolar transistors (IGBTs)] creates a special state, where the two capacitors of each DCL cell are connected in parallel. This may create a large surge current due to the voltage difference between capacitors C_1 and C_2, depending on the current-limiting resistances in series with diodes D_1 and D_2.

2.4 Five-level cross-connected cell MMC

Fig. 2*d* shows a symmetrical five-level cross-connected cell that can generate voltage levels $2V_c$, V_c, 0, $-V_c$ and $-2V_c$, provided the cell capacitor voltages are regulated such that $V_{c1} \simeq V_{c2} \simeq V_c$ [34]. The five-level cross-connected cell in Fig. 2*d* is equivalent to two symmetrical FB cells (four devices in the conduction path, generate the same voltage levels); thus, its loss performance and control range and flexibility are expected to be similar to that of the FB-MMC including operation with positive and negative dc-link voltages.

2.5 Flying capacitor (FC) cell MMC

Fig. 2*e* shows an HB flying capacitor unipolar cell, where each cell generates three voltage levels 0, V_c and $2V_c$ [34]. This FC cell is equivalent to two HBs, where both insert two switches in the conduction path, but uses two capacitors rated at different voltages ($2V_c$ and V_c), compared with V_c in the equivalent HB cells. Therefore, the FC-MMC is expected to be subject to the same control range limitations as the HB-MMC and unipolar dc-link voltage operation and lack of dc reverse blocking. Capacitors with different rated voltages compromise power circuit modularity, thus is less attractive in terms of cell manufacture and maintenance. Although the FC cell can be configured as a symmetrical bipolar cell, similar to FB and five-level cross-connected cells described previously, this possibility is unattractive due to a large number of cell capacitors required.

2.6 Active neutral-point-clamped unipolar cell MMC

Fig. 2*f* displays the MMC that uses an active neutral-point-clamped (ANPC) unipolar cell to generate three voltage levels per cell (0, V_c and $2V_c$) [34]. Operationally, the control range of an ANPC-MMC is limited to unipolar positive dc-link voltages as with the HB-MMC, where power reversal is only achieved by changing the polarity of the dc-link current, and it is unable to block dc faults or decouple cell capacitor regulation from the dc-link voltage (V_{dc}) over a wide range; especially, when V_{dc} falls below the peak of the line-to-line voltage, the interfacing transformer imposes at the converter terminals. Owing to the lack of redundant switch states at the cell level, which restricts the selection of the upper capacitor (C_1), cell capacitor voltages of the ANPC-MMC may exhibit larger capacitor voltage ripple than HB-MMC and FC-MMC of similar rating and energy content. Although all the devices of the ANPC structure have the same voltage rating, two more IGBTs S_5 and S_6 are required, resulting in higher capital cost. Hence, they are not preferable in the practical application, compared with the HB cells.

2.7 Mixed cells MMC

It is possible to employ a combination of different cells within an MMC, with Fig. 2*g* depicts an example of an MC. A lot of combinations are theoretically possible, but most commonly referred to is a combination of HB and FB cells in order to reduce semiconductor losses to less than that of the FB-MMC [34, 35], while retaining some of the control flexibility of the FB-MMC such as:

(a) Resiliency to dc network faults including dc fault reverse blocking capability and controlled operation with reduced and zero dc-link voltage.
(b) Bipolar dc-link voltage operation can be achieved over a limited range, determined by the ratio $\gamma = N_{FB}/N_{HB}$, where $N_{FB} = N\gamma/(\gamma + 1)$, $N_{HB} = N/(\gamma + 1)$, N is the total number of cells per arm ($N = N_{FB} + N_{HB}$) and N_{FB} and N_{HB} are the number of FB and HB cells per arm. This feature is necessary for arc extinction following a dc fault.
(c) The tributes and flexibilities in (a) and (b) show that the MC-MMC could be used to deliver customised features for a given level of semiconductor losses.

Theoretically, the MC-MMC operates using a similar principle as the FB and HB-MMC and adheres to the same insertion functions described in Section 2. However, its operation limits including bipolar dc voltage operation are determined by the ratio 'γ' that defines the control range for 'α_d'. For example, when $\gamma = 1$, $N_{FB} = N_{HB} = (1/2)N$, which implies that the control range for dc modulation index 'α_d' is: $0 \leq \alpha_d \leq 1$; thus, each MC-MMC arm is able to synthesise any voltage level between V_{dc0} and $-(1/2)V_{dc0}$. Within this envelope, each MC-MMC arm can generate the necessary negative voltage to enable operation with any dc-link voltage from rated positive dc voltage (V_{dco}) to $V_{dc} = 0$, without jeopardising the converter ability to synthesise the rated ac voltage. The combination of HB and FB cells as depicted in Fig. 2*g* generates two positive voltage levels ($2V_c$ and V_c) and one negative voltage ($-V_c$) and zero; therefore, it belongs to the family of asymmetric cells (or simply refer to as asymmetric cell).

2.8 Single-clamped (SC) cell MMC

The SC cell shown in Fig. 2*h* [36] provides small negative voltage sufficiently for blocking a dc fault, exploiting additional clamp diode D_1 which is connected to the mid-point of the dc capacitors C_1 and C_2 and middle IGBT. Compared to FB cells, the SC cell requires a reduced number of IGBTs, thus, leading to relatively lower capital cost. It is worth stressing that only half of the cell capacitor voltage per cell is utilised to block dc faults, and the unidirectional conduction of clamping diode D_1 makes the SC cell unable to generate a negative voltage when the MMC is under active control, resulting in restricted control range and flexibility.

2.9 Other cell topologies

Besides the aforementioned cells, more unipolar, asymmetric and symmetric bipolar cells can be found in [34, 36].

3 Special multilevel AC–DC converters

Fig. 3 shows the phase legs of some common modular and hybrid multilevel converters. The following sections discuss the attributes and shortcomings of these converters, and potential relevance to smart transmission systems.

3.1 Alternative arm converter

Fig. 3*a* shows the alternative arm converter (AAC) proposed in [37, 38], which aims to reduce semiconductor losses and converter footprint (size and weight by reducing the number of cells per arm) compared with the FB-MMC, while retaining some of the attributes of the FB-MMC such as dc fault reverse voltage blocking

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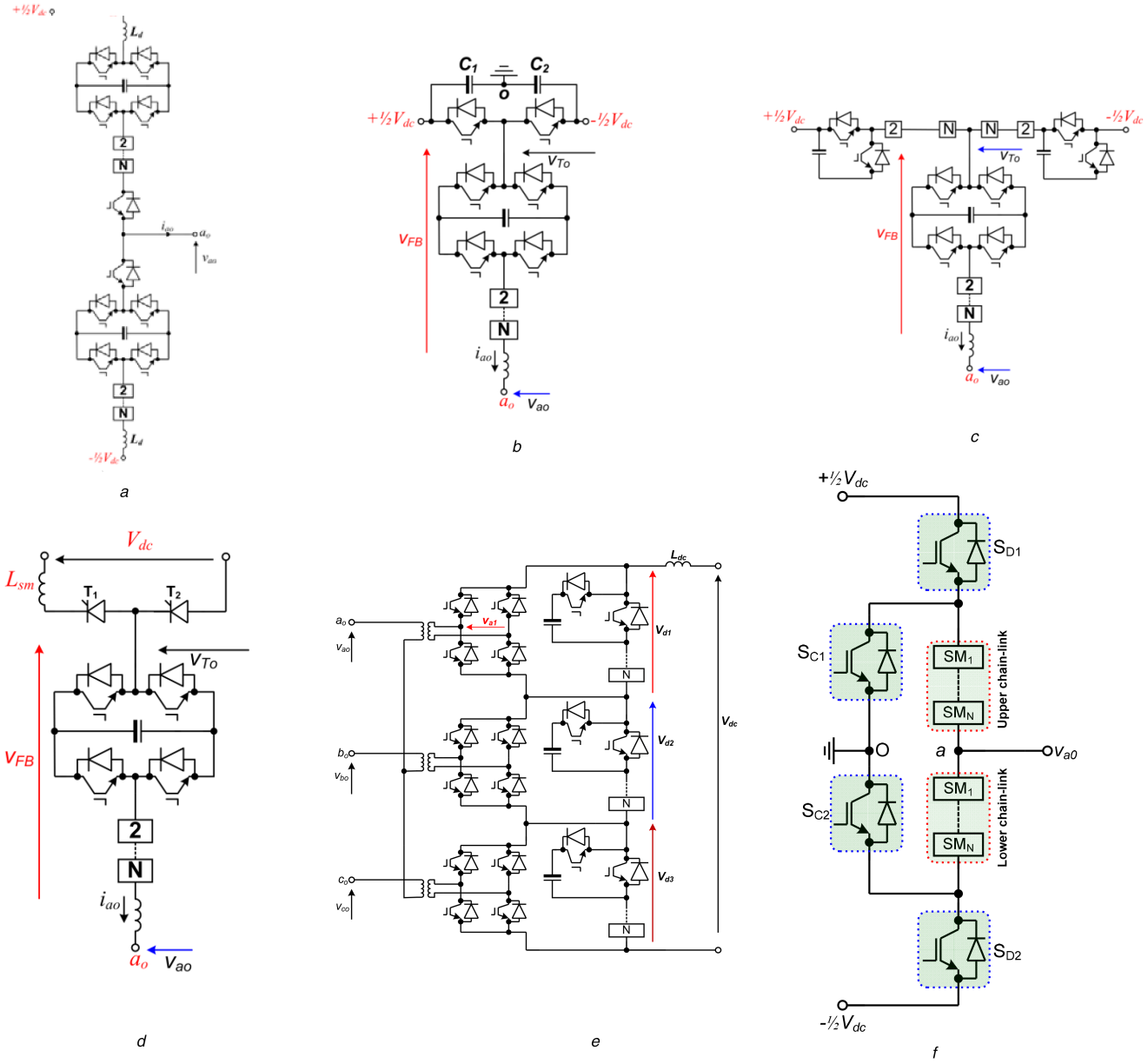

Fig. 3 *Examples of converter (leg) topologies for HVdc transmission systems*

(a) Phase leg of AAC, ***(b)*** HC2LC, ***(c)*** HC-MMC, ***(d)*** Hybrid converter with LCC and ACFB cells, ***(e)*** Hybrid converter with HB cells across the dc-link, ***(f)*** Hybrid multilevel converter with SMs connected to ac terminal (HMC-AC)

ability and reduced dc-link voltage operation. However, in retaining these attributes, the FB cells in each arm of the AAC must be able to block a dc voltage greater than $(1/2)V_{\rm dc}$, as originally envisaged ($\sum_{j=1}^{N} v_{cj}^{\rm FB} > \frac{1}{2}V_{\rm dc}$). Unlike MMC-type converters with concurrent conduction in the upper and lower arms of the same phase leg, each arm of the AAC conducts for 180° with the director switch in each arm used to commutate currents between arms and ensure that each arm is able to block the full dc-link voltage ($V_{\rm dc}$). With the aid of a brief overlap period at the '0' voltage level, where both upper and lower arms of the AAC conduct simultaneously, the director switch of each arm is used to facilitate current commutation between the upper and lower arms. Thus, seamless current commutation is achievable for a limited range of power factors, and beyond which large inrush current occurs in the AAC arms. Its input dc-link capacitors may increase the peak of dc fault current transient component [39].

In an effort to address the aforementioned problems and ensure satisfactory operation over full modulation index linear range and all power factors, extended overlap operation of AAC was proposed [40].

In summary, this discussion shows that the AAC is inferior to MC-MMC in terms of performance, flexibility and control.

3.2 Hybrid cascaded (HC) two-level converter

Fig. 3*b* presents the HC two-level converter (HC2LC) which uses a two-level converter as the main power stage that manipulates the phase and magnitude of the fundamental voltage of the switched voltage ($V_{\rm To}$) to control the converter output active and reactive powers [41]. The ac-side cascaded FB chain link (ACFBCL) of each phase operates as a series active power filter (wave shaping circuit) to inject the necessary voltage harmonics ($V_{\rm FB}$) to cancel the inherent harmonics in the switched output voltage of the two-level converter stage ($V_{\rm To}$), thus a pure sinusoidal output voltage ($v_{\rm ao}$) is generated at output pole '$a_{\rm o}$' relative to dc-link mid-point 'o'. If the orthogonality relationship between $v_{\rm FB}$ and $i_{\rm ao}$ is maintained, the linear range for modulation index control of the HC2LC can be extended to 1.27 without compromise to cell capacitor voltage balancing. This means the *P*–*Q* envelope of the HC2LC will be larger than all MMC-type converters. In the case of reactive power applications, the modulation index control range can be extended further to 2. The HC2LC is expected to be smaller

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than all MMC-type converters as the number of cell capacitors required per phase is a quarter that of the HB and FB-MMC. The main shortcomings of the HC2LC are [42]:

- dc fault reverse blocking capability if achieved at the expense of high semiconductor losses as the number of devices in the conduction path, carrying full load current, is higher than that of the AAC and MC-MMC;
- its input dc-link capacitors contribute substantial discharge current into a dc fault, and this increases the current stresses on the dc switchgear connected to its positive and negative dc poles;
- ensuring synchronisation between the switching of the two-level converter and the chain link is challenging, and it may expose the converter transformer to HV spikes of $\pm 2V_{dc}$ in the worst case, and with a period corresponding to miss-synchronisation period. These spikes tend to introduce low-order harmonics into the baseband and need filtering using ac tuned filters; and
- its operation is limited to positive dc-link voltages, and reduced dc voltage operation is possible and should the number of FB cells in the chain link be increased to be able to synthesise the nominal terminal ac voltage when the dc link is suppressed to zero; thus, operating as a typical cascaded multilevel converter.

3.3 Hybrid cascaded MMC

Fig. 3*c* displays one-phase leg of a hybrid converter that employs an HB-MMC in the main stage (instead of a two-level converter as in the HC2LC described in Section 3.2) to control the fundamental voltage and power exchange between the converter ac and dc sides [43]. The operation of the ac-side FB chain link of each phase leg is as explained for the HC2LC. The low dv/dt of the staircase multilevel voltage waveform 'V_{To}' at its terminal means switching synchronisation to the FB chain link involves a maximum voltage error of one cell capacitor voltage. The HB-MMC in the main stage that allows the FB chain links of the HC-MMC to be used as ac circuit breakers, while the cell capacitors of the HB-MMC facilitate controlled recharge of the dc-link following dc fault clearance [43]. The HC-MMC has a large footprint, high semiconductor losses and high cost due to its larger semiconductor area and a large number of capacitors.

3.4 Line commutated converter with ACFBCL

Fig. 3*d* shows a phase leg of a line commutating converter that uses cascaded FB cells in its ac side as a series active power filter to ensure that the LCC stage receives a distortion free (or pure sinusoidal) commutation voltage, independent of the system operating condition at the point of common coupling [44]. Thus, LCC commutation failure is avoided [44], and the entire LCC reactive power needs can be provided by manipulating the magnitude of the commutation voltage (v_{To}) relative to the magnitude of the grid voltage (v_{ao}) at the point of common coupling. A limited number of tuned ac filters are needed to attenuate the characteristic harmonic currents injected by the LCC stage. The main attributes and limitations of the LCC-FBCL are:

- Lower semiconductor loss than hybrid counterparts such as the HC2LC and HC-MMC.
- Increased power handling of LCC-type HVdc links, without extra equipment dedicated for the provision reactive power support.
- LCC limitations related to power flow direction and reversal remain.

3.5 Hybrid converter with HB cells across the dc-link

Fig. 3*e* shows a three-phase hybrid converter with three limbs of cascaded HB cells connected across the dc link (one limb per phase) [45]. Each limb comprises of N HB cells, supports $(1/2)V_{dc}$ (where V_{dc} is the dc-link voltage) and presents a rectified dc voltage [$V_{d1} = (1/2)V_{dc}|\sin(\omega t + \theta)|$] at the input dc terminals of the HV FB cell of each phase that synthesises an output ac voltage such as (v_{a1}) to be imposed on each isolated winding of the interfacing transformer (thus, switching devices of the HV FB cell must be rated for $(1/2)V_{dc}$). At each instant, '2N' HB cells are selected from the '3N' available cells in the three limbs of the three-phase converter to be used to synthesise rectified dc voltages V_{d1}, V_{d2} and V_{d3} to be presented at dc terminals of the HV FB cell of each phase leg. The HV FB cell connected to output circuit of each phase leg exploits its bipolar switching capability to generate positive and negative halves of the output phase voltages (such as v_{a1} for phase a) from the rectified dc voltages (such as V_{d1} for phase 'a') being presented by the cascaded HB cells of the three limbs. To avoid uncontrolled inrush current, the HB cells to be inserted into the power path at each instant all three limbs must be selected and must be sufficient to match the input dc-link voltage (V_{dc}), i.e. $V_{d1} + V_{d2} + V_{d3} \simeq V_{dc}$. Thus, a large dc inductor (L_{dc}) is needed in the dc link in order to supress any potential inrush current that may arise due to any voltage mismatch between ($V_{d1} + V_{d2} + V_{d3}$) and the input dc-link voltage (V_{dc}). This constraint makes the hybrid converter in Fig. 3*e* unable to generate an ac voltage with variability magnitude, and this is the main weakness of this hybrid converter.

3.6 Other hybrid multilevel converters

Oates and Dyke [46] and Oates *et al.* [47] proposed a controlled transition bridge (CTB) converter that avoids high dv/dt and excessive switching losses of the conventional two-level converter by employing FB chain links rated for half of the dc voltage (V_{dc}) and trapezoidal-type modulation to facilitate stepped transitions of the output voltage between two extrema of $+(1/2)V_{dc}$ and $-(1/2)V_{dc}$, with each voltage step defined by the voltage of one cell capacitor of the FB chain link. The director switches of CTB converter experience slow and gradual build-up of the voltage and switch at zero voltage; director switches do not require stringent series connection of IGBTs and incur zero switching losses. However, trapezoidal modulation imposes limited control range and high ac-side filtering. Extensive discussion of the sinusoidal operation of CTB proposed in [48, 49] show that it generates high-quality multilevel ac voltage as MMCs, and requires large dc-side filtering which increases dc fault level.

Yang *et al.* [50] have proposed a hybrid multilevel converter that represents a modified version of an AAC, but with the node between the director switch (S_{D1} or S_{D2}) and cascaded HB or FB chain link of each arm is clamped to ground (O) through additional director switch (S_{C1} or S_{C2}), see Fig. 3*f*. The chain links of upper and arms of each phase leg are utilised to shape the output ac voltage (v_{ao}), with the director switches operate alternately every half fundamental cycle. It has been claimed in [50] that the proposed converter requires fewer cells and reduced energy storage requirement over full power factor range. As in an AAC, its director switches operate at zero voltage switching, hence, leading to reduced switching losses. However, the director switches of the proposed converter must be designed to withstand voltage stresses amount to half of the rated dc voltage; thus, a large number of series-connected IGBTs are required.

In [51], an improved alternate arm converter (IAAC) was presented, in which the director switches of each phase leg are realised by FC cell. The proposed IAAC addresses the problem of current commutation between the arms and eliminate the dependency on power factor and modulation depth, and no sizable input capacitors or inductors are required for filtering as in conventional AAC.

In [52, 53], a compact MC-MMC which is created by realising the director switch in each arm of conventional AAC by the HV HB cell is proposed. The proposed CMC-MMC offers all the attributes of conventional MC-MMC described earlier.

Recently, a hybrid converter based on the active forced commutated bridge (AFC-B) is proposed for UHVdc transmission systems with rated powers and voltages up to 3000 MW and 800 kV per converter [53, 54]. The proposed hybrid converter requires large ac- and dc-side filtering, and apart from that, it offers many of

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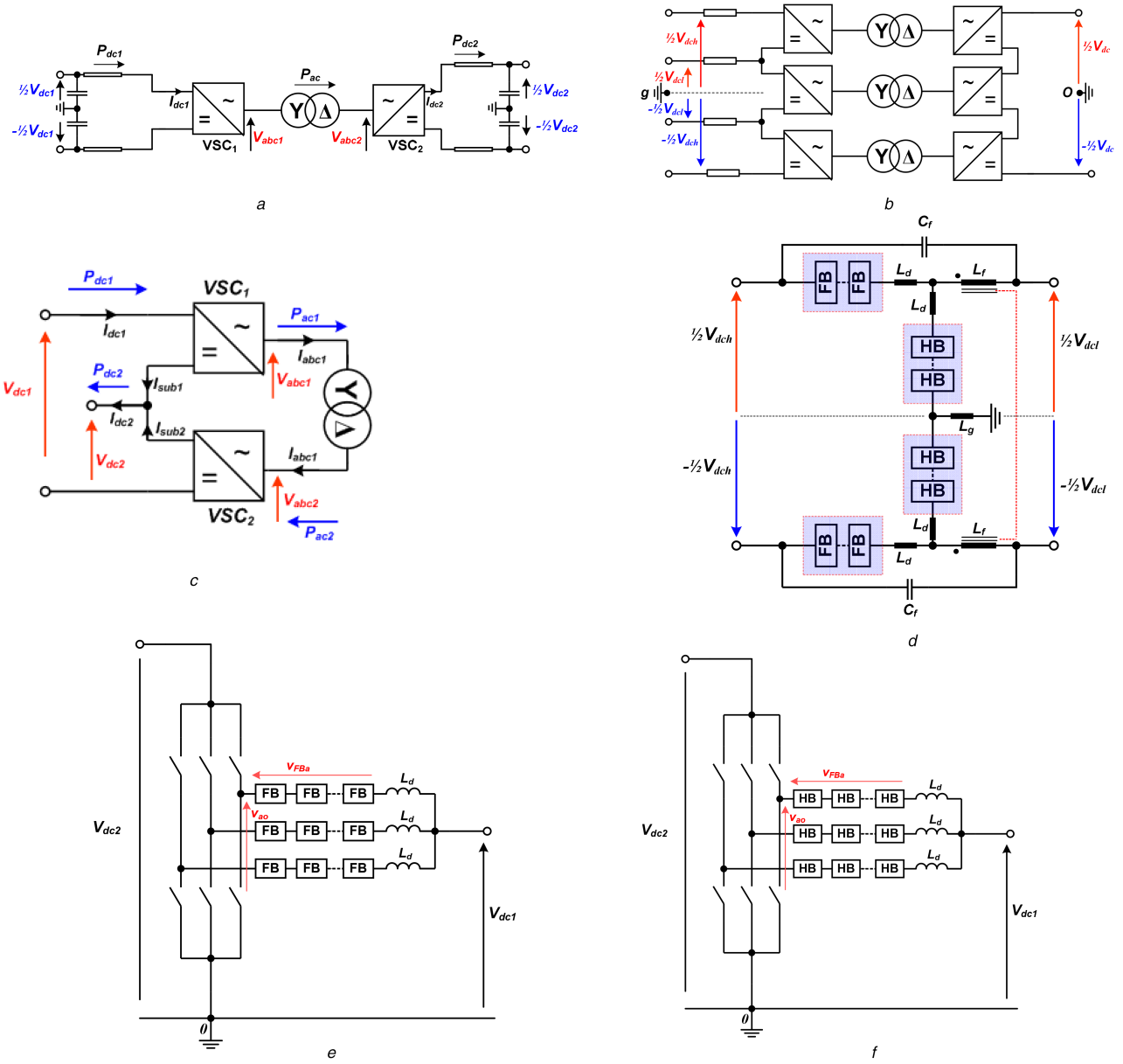

Fig. 4 *Other examples of dc–dc converter topologies*

(a) F2F dc–dc converter, ***(b)*** Isolated F2F dc–dc converter with one side connected to multi-pole dc system, ***(c)*** Partially isolated dc–dc converter, ***(d)*** Non-isolated MMC-based dc–dc converter, ***(e)*** Non-isolated HC two-level dc–dc converter, ***(f)*** HB-based non-isolated HC two-level dc–dc converter

the features of the FB-MMC at reduced semiconductor losses, thanks to the use of symmetrical thyristors in the main conduction paths. Moreover, it employs the FB chain links in its limbs to actively commutate the current between the upper and lower arms of the same phase leg; with no risk of commutation failure. The proposed converter can block dc fault, operate with positive and negative dc voltages, reverse active power with a change of polarity of dc current or voltage polarity, generate leading and lagging reactive powers and resilient to both ac and dc faults.

Bakas *et al.* [55] presented a novel hybrid converter with alternate common arm and director switches that resembles a further improvement to the AFC-B converter in [53, 54]. The presented converter uses thyristors in alternate arms that operate as director switches, and FB chain link in common arm and in the upper and lower arms similar to that of the conventional FB-MMC. In this way, it nearly doubles the current capability of each arm, hence, the power rating, while retaining the power quality of the ac and dc sides as that of the MMCs.

4 DC–DC converters

Fig. 4 shows examples of dc–dc converter topologies with potential to be applied in large-scale HVdc transmission networks to perform voltage matching or tapping and can act as flexible dc controllers to regulate power in highly meshed dc networks [56].

4.1 Front-to-front (F2F) dc–dc converter topology

The F2F dc–dc converter is described in [57–62]. The converter terminals VSC_1 and VSC_2 can employ any of the converter topologies summarised in Figs. 1 and 3, with one converter, act as a reference that defines the ac voltage and frequency in the internal ac link and other converter controls dc power or dc voltage. Although high-frequency square waveform voltage operations of VSC_1 and VSC_2 have been adopted in low- and medium-voltage applications for many years [57–62], sinusoidal or trapezoidal (quasi-two-level) voltage waveform in the ac link with fundamental frequency ranging from 200 to 500 Hz is likely to be adopted in HVdc applications, with dc operating voltages up to 800 kV [56, 63–65].

Besides dc voltage matching, power regulation and dc voltage regulation, the F2F dc–dc converter decouples the dc systems as it can block dc fault propagation from the faulty system to the healthy system. Therefore, the F2F dc–dc converter is suitable for splitting large dc networks into several protection zones to contain

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the impact of dc fault within a well-defined zone. The main shortcomings of the F2F dc–dc converter are:

- Both converter terminals must be fully rated (1 pu); thus, its semiconductor losses resemble that of the two-terminal HVdc link.
- Its dc voltage matching range is limited by the current stresses in the converter switches of the low-voltage side.

The isolated F2F dc–dc converter is shown in Fig. 4*a*. The provided galvanic isolation is necessary for connection of dc system with a separate dc ground.

The F2F converter can also be realised without isolation. In this case, the transformer is replaced by a simple inductor. Although a non-isolated F2F dc–dc converter in HVdc applications can reduce costs, there are major drawbacks of not having isolation. The implication of undermodulation in the non-isolated F2F dc–dc converter is that the switching devices of its HV converter are subjected to the same ac currents as that of the low-voltage converter, which is higher than its isolated counterpart. Thus, high semiconductor losses are incurred in the HV side.

4.2 Multi-pole multi-module F2F dc–dc converter topology

Fig. 4*b* shows a configuration that employs series-input and series-output to connect a symmetrical monopole dc system to a symmetrical multi-pole dc system, with each sub-converter in Fig. 4*a* realised with modular-type converters, or two-level or NPC converters, with each rated at a higher dc voltage and power than in traditional medium-voltage applications. With the multi-pole side being limited to tri-pole, the voltage stresses on the upper and lower transformers in the ac link could be limited to slightly higher than that of conventional bipolar HVdc link [66].

4.3 Partially isolated dc–dc converter topology

Fig. 4*c* shows a schematic diagram of an efficient partially isolated dc–dc converter that can be used for voltage matching and tapping in dc systems with a common dc ground [67, 68]. The total dc power at the HVdc terminal (P_{dc1}) transfers to the low-voltage dc terminal (P_{dc2}), without the need for the switching devices of any of the sub-converters to be rated for full power. The power flow between the two dc terminals of dc–dc converter topology in Fig. 4*b* is explained, assuming the power flow is from the HV to low-voltage dc terminals as follows:

- The total dc power P_{dc2} splits into ac power P_{ac} and dc power P_{dc12}.
- P_{ac} represents the component transferred through the ac side and it determines the magnitudes of ac and dc currents in the arms of VSC_1 and VSC_2 for a given transformer voltage ratio. This component can be approximated by $P_{ac} \simeq (V_{dc1} - V_{dc2})I_{dc1} \simeq P_{dc1}(n-1)/n$, where $n = V_{dc1}/V_{dc2}$.
- P_{dc12} represents the power component transferred directly to the low-voltage dc terminal using dc components of the arm currents, without passing through the switching devices of VSC_2; and can be approximated by $P_{dc12} \simeq I_{dc1}V_{dc2} \simeq P_{dc1}/n$.

In this manner, the switching devices of VSC_1 and VSC_2 must be rated to handle the current stresses corresponding to ac power of $P_{dc1}(n-1)/n$, and dc operating voltage of $V_{dc1}(n-1)/n$ and V_{dc1}/n, respectively.

4.4 Non-isolated MMC-based dc–dc converter

The converter in Fig. 4*d* is formed by series connection of two MMCs (HB or MCs type); however, the MCs approach is preferred because it blocks dc fault propagation from the faulty side to the healthy side, due to its FB dc fault blocking capability [58]. Although this dc–dc converter does not use an isolation transformer, the coupling inductor being employed in the positive and negative poles of the low-voltage dc terminal must be insulated to withstand the high dc voltage stress corresponding to the dc-link voltage of the low-voltage dc terminal, V_{dcl}. An additional weakness of this topology is that the fundamental ac component being used to exchange power between converter arms needs to be filtered using large passive filters (L_f and C_f). On the basis of this discussion, this non-isolated dc–dc converter topology is inferior to the partially isolated topology, as described in the previous section.

4.5 FB-based non-isolated HC two-level dc–dc converter

Fig. 4*e* shows an FB-based non-isolated HC two-level dc–dc converter, where the dc-link of the two-level converter stage represents the HV side ($V_{dc2} > V_{dc1}$) [69]. The submodules of each limb at the low-voltage side must be of the FB type so that it can inject the necessary bipolar ac voltage waveform to cancel some of the generated voltage by the two-level converter stage. In this way, a ripple-free fully controlled dc voltage with magnitude V_{dc1} will be generated at the low-voltage dc terminal. This means the series-connected switching devices of the two-level converter stage must be rated for HV-side voltage (V_{dc2}). Inhibiting the gating signals is sufficient to prevent dc fault propagation from one side to the other, independent of the fault location (dc short circuit). Lack of isolated dc ground may require system shutdown during a pole-to-ground (P2G) dc fault to prevent exposure of the healthy pole to excessive dc voltage stresses. In this topology, the number of semiconductor devices in the conduction path (thus, conversion loss) is the same as in F2F dc–dc two-level converter, but its overall losses and semiconductor area remain lower than F2F dc–dc converter topologies.

4.6 HB-based non-isolated HC two-level dc–dc converter

Fig. 4*f* shows an HB-based non-isolated HC two-level dc–dc converter, where the dc-link of the two-level converter stage represents the low-voltage dc terminal ($V_{dc1} > V_{dc2}$), and cascaded HB cells are used (instead of the FB cells) as each limb only needs to inject a unipolar voltage waveform to boost the output dc voltage [69]. In this scenario, the chain link of each limb must be able to support the full dc voltage of the HV side.

5 Series-type DC flow controlling devices

Besides dc fault ride-through challenges highlighted in previous sections, full utilisation of dc lines in meshed multi-terminal HVdc transmission networks that contain a number of floating dc nodes is extremely important for efficient operation of dc grid. However, control of the dc power flows on the individual dc lines that form a mesh is technically challenging [70] as the current split between parallel paths is solely determined by the Ohm and Kirchoff laws. Unlike in an ac system, a dc system does not have a phase angle or reactive power, giving less degree of freedom to control the power flow. To realise better utilisation of dc cables in a meshed MT-HVdc network, the dc equivalent of the FACTS devices such as power shifters, are beneficial to optimise the power flow within the dc network.

This task can be performed by incorporating appropriate dc–dc converters or interline series-type current controlling devices [71–73]. Although series-type power controlling devices appear effective and cost-effective, their ability to survive dc short-circuit faults are yet to be demonstrated. Apart from isolating transformers, all the power electronic parts are fractionally rated. In addition to dc–dc converter discussed in Section 5, some of the proposed methods for power flow control in MT-HVdc networks are discussed briefly in the following sections.

5.1 Controlled series resistor

Fig. 5*a* shows a dc power controller that uses a series switched resistor to regulate the power flow between two dc nodes by manipulating the dc voltage drop of the line that connects these dc nodes [71–73]. Although this solution seems to be simple and effective, it has a limited control range.

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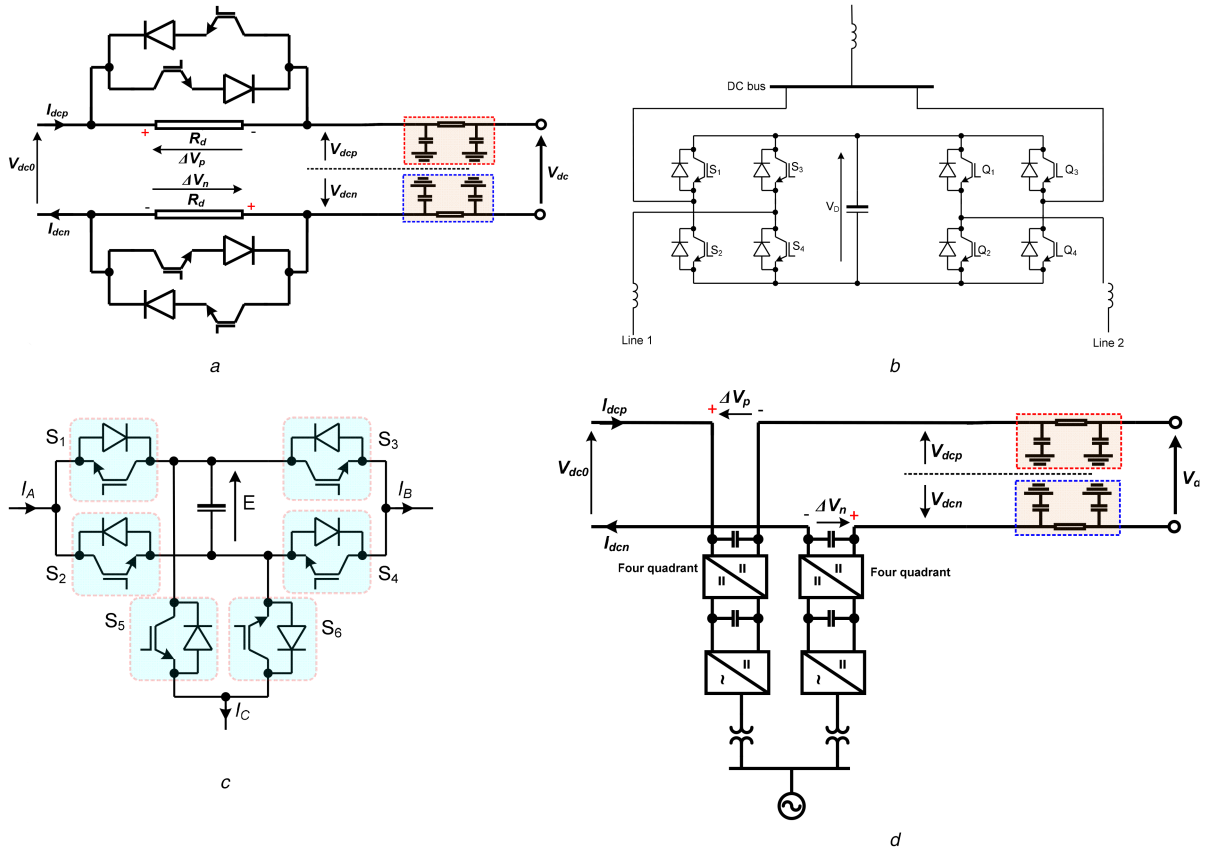

Fig. 5 *Controlled series resistor*

(a), ***(b)*** Examples fractionally rated dc series power controller for highly meshed multi-terminal HVdc network

5.2 Series current flow controllers

Amongst several series current flow controllers proposed in [72, 74–78], Figs. 5*b* and *c* show examples of series-connected bidirectional dc current or power flow controllers capable of controlling power flow in individual dc lines by inserting small positive or negative dc voltage in series with a given dc line, depending on the power flow direction [72, 76–78]. These power flow controllers incur low on-state losses as they present a small number of semiconductor devices in conduction path. Extensive studies performed in [72, 76–78] show these series controllers are able to operate satisfactorily over a wide range of operating conditions and can survive dc faults.

5.3 Series voltage injection

The solution in Fig. 5*d* can control dc power in a given dc line from zero to the rated power and in a reverse direction due to its ability to inject positive or negative dc voltage in series with the line [71–73]. This device is equivalent to a unified power flow controller in an ac system.

6 DC circuit breakers

The current absence of a cost-effective HV DCCB is the main missing element that prevents bringing dc grids in line with ac counterpart. Its absence denies the ability to isolate the faulty dc part while allowing the remaining healthy parts of the dc grid to operate normally. Being able to continuously exchange power is paramount from supply reliability and security point of view. Although the technology for solid-state DCCBs has existed since the 1990s and is improving, they incur excessive semiconductor losses and cost [79–87]. Figs. 6 and 7 summarise some of the main DCCBs being suggested for dc fault current interruption in multi-terminal dc networks, targeting different fault clearance times.

6.1 Hybrid DCCBs

Figs. 6*a* and *b* show types ‘1’ and ‘2’ hybrid DCCBs that exploit a voltage injection method to force the fault current to zero, where the injected dc voltage must be larger and oppose that being presented by the faulty line [79, 86, 87]. During normal operation, the main conduction path for the dc current is through a low-voltage-rated semiconductor switch known as a load commutation switch (LCS) and low-resistance mechanical ultra-fast disconnector (UFD) with SF6 as insulation media and a 2 ms opening time. The mechanical UFD must be designed to support the prospective dc voltage when opened. When the dc fault is detected in the type ‘1’ DCCB, the LCS is turned off to initiate commutation of the dc fault current from the principle conduction path to the main circuit breaker (MCB), which is a typical HV semiconductor switch, capable of carrying high current for short period (<10 ms) [88, 89]. After the entire dc fault current is commutated to the MCB, the mechanical UFD is opened at near-zero current and voltage, and during this period the fault current continues to flow in the MCB, and then, the MCB is opened to interrupt the dc fault current. More details in Fig. 6*a* are presented in [86, 87].

The type ‘2’ DCCB in Fig. 6*b* turns off LCS when a dc fault is detected and triggers the switching delay branches in a progressive manner in order to commutate the fault current from the main conduction path to the arming branch. The current in each switching delay branch drops to zero when its capacitor charges to the blocking voltage across the LCS. After the entire fault current is transferred to the arming branch and all thyristors of the switching delay branches are off and carry zero current, the mechanical UFD is turned off. This is followed by gating off the composite thyristor of the arming branch to interrupt the fault current to force the surge arrester across the arming branch to absorb the entire inductive energy of the faulty line and to force the fault current to zero [79]. The hybrid DCCBs in Figs. 6*a* and *b* are intended for the faster current interruption, ranging from 3 to 5 ms.

The hybrid DCCB in Figs. 6*c* and *d* [85, 90] have similar on-state losses and operating speed as the counterparts in Figs. 6*a* and *b*.

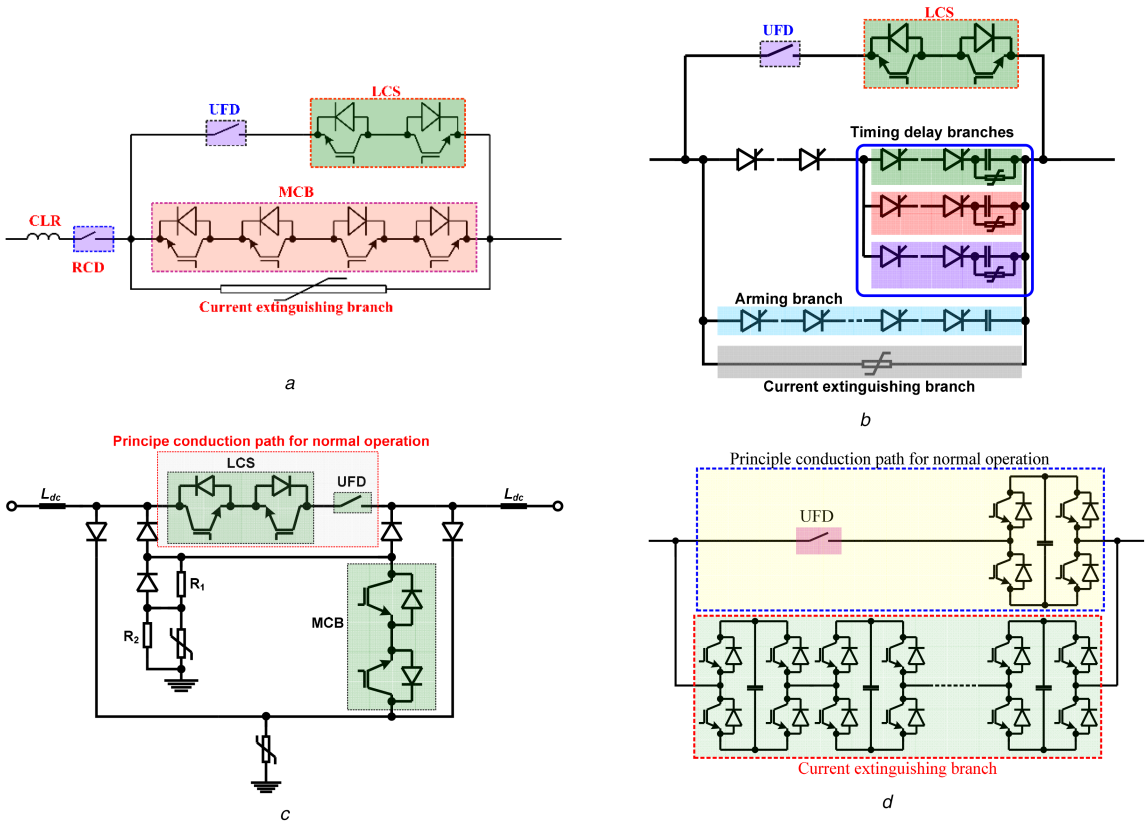

Fig. 6 *Some hybrid DCCBs being proposed for use for dc fault isolation in dc grids*
(a) Type 1 hybrid DCCB, ***(b)*** Type 2 hybrid circuit breaker, ***(c)*** Type 3 hybrid DCCB, ***(d)*** Type 4 hybrid DCCB

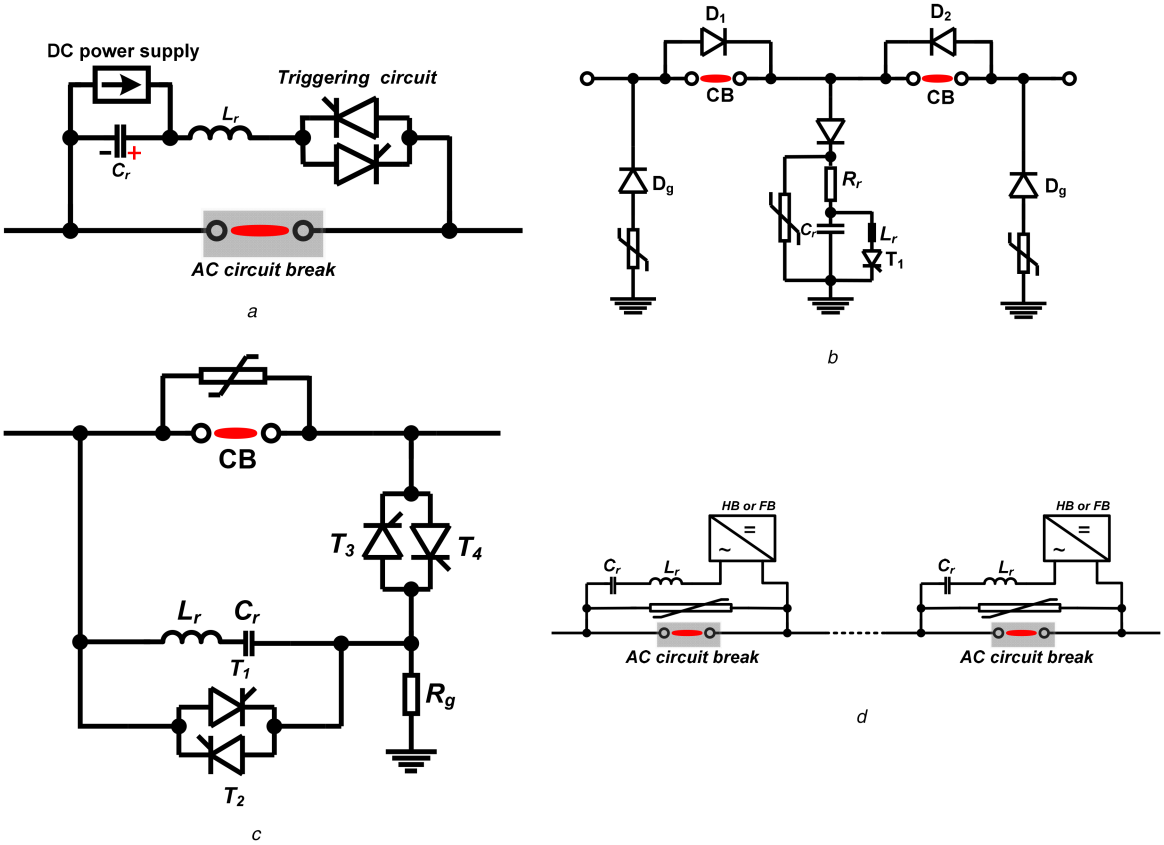

Fig. 7 *Some resonant DCCBs being proposed for use for dc fault isolation in dc grids*
(a) Forced current zero resonance circuit breaker (type 1), ***(b)*** Forced current zero resonance circuit breaker (type 2), ***(c)*** Forced current zero resonance circuit breaker (type 3), ***(d)*** Forced current zero resonance DCCB (type 4)

6.2 Resonant DCCBs

Fig. 7*a* shows a forced current zero resonance DCCB that uses a pre-charge capacitor to initiate resonance with the aim of creating a speedy current zero when the negative peak of the resonant current component is larger than the dc component of the fault current [83]. In [83], this approach interrupts a dc fault current up to 21 kA, within 8–10 ms.

Figs. 7*b* and *c* show other versions of low-loss active resonance-based DCCBs [82]. The versions of the active resonance DCCBs displayed in Figs. 7*b* and *c* are expected to have similar performance (on-state loss, current breaking capability and operating speed) as that presented in Fig. 7*a*, where the options in Figs. 7*a* and *b* permit easy incorporation of additional resonance branches that facilitate execution of several successive fault clearance attempts.

Besides relatively slow resonant DCCBs discussed above, Ängquist *et al.* [91] presented a cost-effective fast acting resonant-based hybrid DCCBs that use vacuum ac circuit breaker technology in parallel with resonance branch that uses HB or FB cells to initiate high-frequency resonance, see Fig. 7*d*. Each resonance branch consists of an HB or FB cell in series with inductor and capacitor, and when the fault is detected the HB or FB cell will be switched at 10 kHz to impose bipolar square waveform voltage in each resonance branch, causing high-frequency bipolar oscillating current with increasing magnitude to be superimposed on the dc fault current. Operation of HB or FB cell at each resonance branch at 10 kHz permits creation of multiple current zeros within 1 ms (recall that the current zeros are created when the negative peaks of the oscillating current equal or exceed the magnitude of the actual dc fault current). In this manner, the DCCB in [91] is able to interrupt dc faults within sub-milliseconds, provided that the protection systems responsible for fault discrimination are able to operate with such speed.

7 Discussion

On the basis of a critical review of the open literature, the main findings of this work are highlighted as follows:

i. MMCs: It is established that the MMCs with asymmetrical and symmetrical bipolar cells can block and control dc fault current, and remain controllable for a wide range of dc voltages, and these features are useful for pole restraining during a P2G dc fault. Therefore, MC-MMC as a representative of the MMCs with asymmetric bipolar cells offers all flexibilities needed for efficient, reliable and fault-tolerant operation of VSC-based dc grids. Nonetheless, extra control range offered by the MMCs with symmetrical bipolar cells such as the FB-MMC is well-suited for generic dc grids that employ both VSCs and LCCs (thanks to the ability to operate with positive and negative dc voltages and reverse power flow direction by the change of dc current or voltage polarities).
ii. *Hybrid multilevel converters*: Section 3 establishes that the AFC-B converter and hybrid converter with alternate common arm and director switches in [53–55] offer most of the features of the FB-MMC at much lower semiconductor losses. The former increases the power capability at reduced semiconductor losses, but requires substantial ac and dc filtering. Whilst the latter increases the power capability with no filtering requirements at ac and dc sides, thanks to additional current path provided by the thyristor-based director switches which conduct alternately, i.e. upper director switch conducts for half fundamental cycle with the upper arm of the FB-MMC and vice versa. The latter hybrid converter resolves the current commutation problem of the conventional AAC and its variants [37, 38, 40, 51, 52, 92, 93]. These hybrid converters are well-suited for generic and large dc grids, where the LCCs are expected to operate alongside VSCs. On another hand, hybrid converters in [51, 52] are a viable alternative to conventional AAC and MC-MMC and most of the MMCs with asymmetric bipolar cells, particularly in applications with confined space as they offer all features of MC-MMC with arguably reduced footprint and power circuit and control complexity.
iii. *dc–dc Converters*: Isolated F2F dc–dc converters offer many desirable features for reliable operation of dc grids such as prevention of dc fault propagation and pole shifting in the healthy side during pole-to-pole (P2P) and P2G dc faults, respectively, and dc voltage matching and power control (it is worth stressing that these features are essential for partial selective dc grid protection strategies that employ the zoning concept). However, high capital cost and semiconductor losses may hinder their acceptance as an economic solution. Non-isolated F2F dc–dc converters are unable to prevent pole shifting during P2G dc fault and suffer from high losses and poor utilisation of the semiconductor of the HV converter; therefore, not viable for dc grids. Partially isolated dc–dc converter in [67, 68, 94] is attractive economically as it permits the transformer in its ac link and sub-converters to be fractionally rated. Its multi-port version that generates multiple and independent dc and ac voltages are attractive for the complex hub that facilitates dc and ac voltage tapping and matching and power control, with the bespoke ability to precisely define the route of the power flow from a given input to a given output [94, 95]. The non-isolated MMC and HC two-level dc–dc converters in [69, 96] offer a cost-effective solution for dc voltage matching between two dc systems with common ground.
iv. *Series current flow controllers*: Fractionally rated bidirectional interline current or power flow controllers in [72, 74–78] offer low cost solutions for controlling and rerouting dc currents or dc powers within the dc grids away from the bottlenecks and over-loaded dc cables; thus, these devices are expected to play major roles in large dc grids that include floating dc nodes.
v. DCCBs: Section 6 reviews a number of basic DCCB technologies, covering fault isolation time scales ranging from 2 to 15 ms. It is found that though the hybrid DCCBs offer faster fault clearance times (2–5 ms) which is critical for continued operation of dc grids, their large semiconductor areas make them expensive and vulnerable to rapid rise of fault current, particularly, in large dc grids that operate at dc voltages above 640 kV and contain a number of long dc cables. Resonance-based mechanical DCCBs offer slower fault clearance time (up to 15 ms) and require large dc inductances to be installed strategically across the dc grid to slowdown the rate of rising of fault currents and fault propagation through the dc grid. Nevertheless, mechanical DCCBs remain practically attractive because of their relatively low cost and small semiconductor areas, primarily, in the resonant branch. Active resonance DCCB with reduced semiconductor area proposed in [91] offers the best overall trade-offs between performance (fault clearance times in the order of 3–5 ms) and cost. However, an economic mechanism for sustaining the dc voltage of the fractionally rated VSC that responsible for initiation of high-frequency resonant as soon as dc fault is detected remains to be solved. The concept of multiline DCCB proposed in [97, 98] represents an economic way to protect multiple dc cables connected to a single dc node using one current breaking branch. In this way, the overall cost of the dc grid protection can be reduced substantially.

In summary, Tables 1–5 provide a high-level summary of the main aspects discussed earlier.

8 Conclusions

Recognising its limitations, LCC-HVdc links could act as backbones for highly complex power grids, so that they can operate with nearly constant power, meaning that the required power balancing and frequency control function could be performed by VSC-HVdc links, some of the generators and other FACTS devices.

HB-MMCs and its variants are expected to dominate HVdc parts of future smart grids due to their high efficiency and fault-tolerant circuit structure, which can facilitate continued operation

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during internal faults (cell failures) and resiliency to ac network faults. This is enabled by recent progress in the DCCBs developments (summarised in Section 7). There are a number of established and successful methods available that allow the HB-MMC and its variants to survive a dc fault for extended periods prior to the opening of the dc circuit such as diversion of part or the entire fault current to thyristors or mechanical switch. However, successful isolation of the faulty part, while ensuring uninterrupted power exchange through the healthy parts of the HVdc network, relies on the incorporation of large dc inductances in order to prevent the rapid collapse of the dc voltage in the healthy parts; thus, slowing down the dc fault propagation within the dc network.

FB-MMCs and its inferior derivatives (from a control aspect) offer a solution for less critical power corridors in future power grids, where the entire dc network which is affected by a dc short-circuit fault could be allowed to briefly stop operation. During this, dc fault clearance can be done using fast disconnectors or ac circuit breakers, and the system could afterwards be reenergised quickly from the ac grids or stored energy in the converters' cell capacitors in a controlled manner. In such a scenario, the dc fault current could be extinguished rapidly by a brief period of negative polarity dc voltage injection. Additionally, these converters can prevent exposure of the healthy pole to twice the rated dc voltage during a P2G dc fault (pole restraining); thus, facilitating continued operation during a P2G dc fault. These power converter groups could be designed for a customised level of fault-tolerant operation against semiconductor losses.

dc–dc Converters are essential for proper operation of highly meshed MT-HVdc networks (power flow optimisation, dc voltage matching and segmentation of large MT-HVdc networks into several protection zones). F2F dc–dc converters offer all these features, but at a high level of losses and cost as both its converters and transformer have to be rated for 1 pu power. Non-isolated or partially isolated auto dc transformers offers dc voltage matching and power flow optimisation at reduced semiconductor loss and cost. However, they compromise the dc fault protection offered by

Table 1 High-level comparison MMCs employ unipolar cells, and asymmetric and symmetric bipolar cells [40, 48, 51, 52, 99–110], where P and Q stand for active and reactive powers, V_{dc} is the dc voltage and V_{dc0} stand for rated dc voltage

	MMC with unipolar cells	**MMC with asymmetric bipolar cells**	**MMC with symmetric bipolar cells**
dc fault blocking	no	yes	yes
control of fault current	no; therefore, necessitates the use of fast acting DCCBs plus large dc inductors to quickly isolate dc faults and prevent over stressing of the converters' semiconductor switches	yes; therefore, a range of options available, ranging from relatively cheap mechanical DCCBs to simple ultra-fast dc switches could be combined with fault current capability of the MMCs with asymmetric bipolar cells to isolate dc faults	yes; therefore, a range of options available, ranging from relatively cheap mechanical DCCBs to simple ultra-fast dc switches could be combined with fault current capability of the MMCs with symmetric bipolar cells to isolate dc faults
active and reactive powers	(a) independent control of P and Q, with maximum capacitive Q, is limited by dc voltage limit and inductive Q by current limit (b) P reversal is achieved by change direction of I_{dc}, while V_{dc} remains positive (c) losses control over P and Q when the V_{dc} falls below line-to-line voltage at converter ac side	(a) independent control of P and Q, with maximum capacitive Q, is limited by dc voltage limit and inductive Q by current limit (b) P reversal is achieved by change direction of I_{dc}, while V_{dc} polarity remains positive (c) retains control over P and Q for wide range of positive dc voltage, $0 \le V_{dc} \le V_{dc0}$, where V_{dc0} is the rated dc voltage	(a) independent control of P and Q, with maximum capacitive Q, is limited by dc voltage limit and inductive Q, but current limit However, maximum capacitive reactive power can be extended if the overmodulation capability is exploited (b) P reversal can be achieved by changing the polarities of I_{dc} or V_{dc} (c) Retains control over P and Q for very wide range of dc voltage $-V_{dc0} \le V_{dc} \le V_{dc0}$
dc voltage polarity and range	remain controllable for narrow range of positive dc voltages which are greater than the peak of the line-to-line voltages interfacing transformers impose at MMCs ac terminals. Therefore, MMCs with unipolar cells only applicable to VSC-based dc grids	remain controllable for a wide range of positive dc voltages, $0 \le V_{dc} \le V_{dc0}$. Therefore, MMCs with asymmetric bipolar cells applicable to VSC dc grids, and hybrid dc grids with combinations of VSCs and LCCs provided that unidirectional power flows are contemplated in all LCC terminals	remain controllable for very wide range of positive and negative dc voltages $-V_{dc0} \le V_{dc} \le V_{dc0}$. This feature permits operation in generic dc grids alongside LCCs, without compromising bidirectional power flow at LCC terminals
internal fault management	yes, and realized by bypassing of faulty cells; hence, simpler cell structures such as HB are preferred for ease of identification of the faulty cells	yes, and realized by bypassing of faulty cells; hence, simpler cell structures such as HB and FB are preferred for ease of identification of faulty cells	yes, and it is realized by bypassing of faulty cells; hence, simpler cell structures such as FB are preferred for ease of identification of faulty cells. Five-level cross-connected cell is an alternative for FB cell that delivers MMC with similar features as FB-MMC, but its complex structure increases the complexity of internal fault management
over modulation	no, even though the MMCs with unipolar cells include redundant cells to facilitate continued operation during internal faults, these cells remain unusable for extension of modulation index linear beyond 1.155; this limit is due to single polarity of the voltages that the unipolar cells generate	yes, should the MMCs with asymmetric bipolar cells include redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the maximum achievable ac voltage, exploiting limited bipolar capability of the asymmetric bipolar cells	yes, should the MMCs with asymmetric bipolar cells include redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage, exploiting full bipolar capability of the symmetric bipolar cells
semiconductor losses	low	medium	high

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Table 2 High-level comparison selected hybrid converters (A≡AAC, B≡CMC-MMC, C≡AFC-B converter and D≡hybrid converter with alternate common arm and director switches) [40, 52–55, 93, 111–117]

	A	B	C	D
dc fault blocking	yes	yes	yes	yes
resiliency to ac faults	resilient to symmetrical ac fault, but unsatisfactory performances during severely unbalanced ac grids and asymmetrical ac faults	yes, resilient to symmetrical and asymmetrical ac faults	yes, resilient to symmetrical and asymmetrical ac faults	yes, resilient to symmetrical and asymmetrical ac faults
control of fault current	yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical DCCBs to simple ultra-fast dc switches could be used to ride-through dc faults	yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical DCCBs to simple ultra-fast dc switches could be used to ride-through dc faults	yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical DCCBs to simple ultra-fast dc switches could be used to ride-through dc	yes, therefore, a range of options available, ranging from relatively cheap and slow mechanical DCCBs to simple ultra-fast dc switches could be used to ride-through dc faults including fault clearance
active and reactive power control	(a) independent control of P and Q, but with very limited reactive power (b) P reversal is achieved by change polarity of I_{dc}, while V_{dc} polarity remains positive (c) retains control over P and Q for wide range of positive dc voltage $0 \le V_{dc} \le V_{dc0}$	(a) independent control of P and Q (b) P reversal is achieved by change polarity of I_{dc}, while V_{dc} polarity remains positive (c) retains control over P and Q for wide range of positive dc voltage $0 \le V_{dc} \le V_{dc0}$	(a) independent control of P and Q (b) P reversal is achieved by change of polarities of I_{dc} or V_{dc} (c) retains control over P and Q for very wide range of positive and negative dc voltages $-V_{dc0} \le V_{dc} \le V_{dc0}$	(a) independent control of P and Q (b) P reversal is achieved by change of polarities of I_{dc} or V_{dc} (c) retains control over P and Q for very wide range of positive and negative dc voltages $-V_{dc0} \le V_{dc} \le V_{dc0}$
dc voltage polarity and control range	remain controllable for wide range of positive dc voltages, $0 \le V_{dc} \le V_{dc0}$. Despite the above features, compatibility of AAC with other VSC topologies such as MMC in dc grids, and hybrid dc grids with combinations of VSCs and LCCs remain debatable	remain controllable for wide range of positive dc voltages $0 \le V_{dc} \le V_{dc0}$. Therefore, CMC-MMC is applicable to VSC-based dc grids, and hybrid dc grids with combinations of VSCs and LCCs provided that the unidirectional power flows are contemplated in all LCC terminals	remain controllable for very wide range of positive and negative dc voltages $-V_{dc0} \le V_{dc} \le V_{dc0}$. This feature permits operation in generic dc grids alongside LCCs, without compromising bidirectional power flow at LCC terminals	remain controllable for very wide range of positive and negative dc voltages $-V_{dc0} \le V_{dc} \le V_{dc0}$. This feature permits operation in generic dc grids alongside LCCs, without compromising bidirectional power flow at LCC terminals
internal fault management	yes, faulty cells of the FB chain-links are bypassed, while the director switches necessitate the use of press-pack IGBTs or IGCTs with fail safe short-circuit mode. Thus, redundant cells and press-pack IGBTs must be incorporated in the FB chain links and director switches, respectively	yes, faulty cells of the FB chain-links are bypassed, while the director switches necessitate the use of press-pack IGBT with fail safe short-circuit mode. Thus, redundant cells and press-pack IGBTs must be incorporated in the FB chain links and director switches, respectively	yes, faulty cells of the FB chain-links are bypassed, while the director switches necessitate the use of symmetrical thyristors that fail in safe short circuit mode. Thus, redundant cells and thyristors must be incorporated in the FB chain links and director switches, respectively	yes, faulty cells of the FB chain-links are bypassed, while the director switches necessitate the use of symmetrical thyristors that fail in safe short-circuit mode. Thus, redundant cells and thyristors must be incorporated in the FB chain links and director switches, respectively
over modulation	yes, should the AAC contains redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage	yes, should the CMC-MMC contains redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage	yes, but limited to maximum modulation index of 1.27; thus, the magnitude of the maximum achievable ac voltage	yes, should the hybrid converter with alternate common arm and director switches include redundant cells to facilitate continued operation during internal faults, and these cells could be used to extend modulation index linear range beyond 1.155; thus, the magnitude of the maximum achievable ac voltage
semiconductor losses	medium	medium	low	low
applications	point-to-point HVDC links with rated power up to 1000 MW	point-to-point and multi-terminal HVDC systems with rated power up to 1000 MW and dc voltage up to 640 kV	point-to-point and multi-terminal UHVDC systems with rated power up to 3000 MW and dc voltage up to 800 kV	point-to-point and multi-terminal UHVDC systems with rated power up to 3000 MW and dc voltage up to 800 kV
remarks	offers most features of MMCs with asymmetric bipolar cells	offers all features of MMCs with asymmetric bipolar cells	offers most features of MMCs with symmetric bipolar cells	offers most features of MMCs with symmetric bipolar cells

the F2F topology. This means cost-effective dc auto-transformers could be used in less critical power corridors of smart grids.

Series-type power flow controllers such as in Fig. 5 offer the possibility for optimising dc power flow in highly meshed MT-HVdc networks without excessive power loss and the high cost of dc transformers (dc–dc converters).

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Table 3 High-level comparison of dc–dc converters for HVdc applications [56, 63, 95, 118–122]

	Non-isolated F2F	Isolated F2F	Partially isolated	Non-isolated MMC	Non-isolated HC
dc voltage matching	yes	yes	yes	yes	yes
dc voltage and power control	yes	yes	yes	yes	yes
control flexibility	normal	normal	high	normal	normal
dc fault containment	stops P2P dc fault from spreading to healthy side, but unable to prevent pole shifting as a result of P2G dc fault	stops P2P dc fault from spreading to healthy side, and prevents pole shifting in the healthy side as a result of P2G dc fault	stops P2P dc fault from spreading to healthy side, and prevents pole shifting in the healthy side as a result of P2G dc fault	stops P2P dc fault from spreading to healthy side, and prevents pole shifting in the healthy side as a result of P2G dc fault	stops P2P dc fault from spreading to healthy side, and prevent pole shifting in the healthy side as a result of P2G dc fault
power losses	very high	high	low	moderate	moderate
cost	very high	high	moderate	moderate	moderate

Table 4 High-level comparison of series power flow controllers [72, 74, 76–78]

	Controlled series resistor	Interline series power flow controllers	Isolated series voltage injection
control range	control dc line power flow in one direction	control dc line power flow in both directions	control dc line power flow in both directions
power losses	low	low	relatively high
complexity (circuit and control)	low	low, thanks to low-voltage-rated IGBTs and capacitors	relatively high (two back-to-back converters and isolation transformers)
vulnerability to dc faults	manageable	manageable	manageable
cost	low	high	moderate

Table 5 High-level comparison of low-loss DCCBs [18, 76, 85, 89, 91, 97, 98, 123–138]

	Hybrid DCCBs	Resonance-based DCCBs
target operating speeds	3–5 ms	8–15 ms, except type 4 DCCB in Fig. 7*d*
cost	high, because of their large semiconductor areas	relatively low, because of their relatively low semiconductor areas
current breaking capacity	relatively low (semiconductor switches of the breaking branch restrict its current breaking capability); therefore, relatively large dc inductors are needed to slow the rate of rising of dc fault currents	high; however, large dc inductors are needed to slow the rate of rising of dc fault currents and extend the fault clearance time, without posing risk to semiconductor switches of the converters
footprint	large, mostly dominated by semiconductor devices	relatively small due to small semiconductor areas

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10 References

[1] Xiaolin, L., Zhichang, Y., Jiao, F., *et al.*: 'Nanao multi-terminal VSC-HVDC project for integrating large-scale wind generation'. 2014 IEEE PES General Meeting | Conf. & Exposition, 2014, pp. 1–5

[2] Wang, W., Barnes, M., Marjanovic, O.: 'The impact of control design on dynamic behaviour of multi-terminal VSC-HVDC (MTDC) system under AC grid fault conditions'. Seventh IET Int. Conf. Power Electronics, Machines and Drives (PEMD 2014), 2014, pp. 1–6

[3] Le Blond, S.P., Deng, Q., Burgin, M.: 'High frequency protection scheme for multi-terminal HVDC overhead lines'. 12th IET Int. Conf. Developments in Power System Protection (DPSP 2014), 2014, pp. 1–5

[4] Hadjikypris, M., Terzija, V.: 'Active power modulation assisting controller scheme implemented on a VSC-HVDC link establishing effective damping of low frequency power oscillations'. 2014 IEEE Int. Energy Conf. (ENERGYCON), 2014, pp. 295–302

[5] Paul, S., Rabbani, M.S., Kundu, R.K., *et al.*: 'A review of smart technology (smart grid) and its features'. 2014 First Int. Conf. Non-conventional Energy (ICONCE), 2014, pp. 200–203

[6] Wang, L., Thi, M.S.: 'Comparisons of damping controllers for stability enhancement of an offshore wind farm fed to an OMIB system through an LCC-HVDC link', *IEEE Trans. Power Syst.*, 2013, **28**, pp. 1870–1878

[7] Wang, L., Vo, Q.S., Prokhorov, A.V.: 'Comparative stability analysis of a DFIG-based offshore wind farm fed to a multi-machine power system through an LCC-HVDC link and an HVAC line'. 2016 IEEE/PES Transmission and Distribution Conf. Exposition (T&D), 2016, pp. 1–6

[8] Erol-Kantarci, M., Mouftah, H.T.: 'Energy-efficient information and communication infrastructures in the smart grid: a survey on interactions and open issues', *IEEE Commun. Surv. Tutor.*, 2015, **17**, pp. 179–197

[9] Rietveld, G., Braun, J.P., Martin, R., *et al.*: 'Measurement infrastructure to support the reliable operation of smart electrical grids', *IEEE Trans. Instrum. Meas.*, 2015, **64**, pp. 1355–1363

[10] Martinez, E.V., Serna, J.A.D.L.O.: 'Smart grids part 1: instrumentation challenges', *IEEE Instrum. Meas. Mag.*, 2015, **18**, pp. 6–9

[11] Veldman, E., Verzijlbergh, R.A.: 'Distribution grid impacts of smart electric vehicle charging from different perspectives', *IEEE Trans. Smart Grid*, 2015, **6**, pp. 333–342

[12] Chiu, T.C., Shih, Y.Y., Pang, A.C., *et al.*: 'Optimized day-ahead pricing with renewable energy demand-side management for smart grids', *IEEE Internet Things J.*, 2016, **PP**, p. 1

[13] Xu, S., Qian, Y., Hu, R.Q.: 'On reliability of smart grid neighborhood area networks', *IEEE Access*, 2015, **3**, pp. 2352–2365

[14] Picciariello, A., Alvehag, K., Löder, S.: 'Impact of network regulation on the incentive for DG integration for the DSO: opportunities for a transition toward a smart grid', *IEEE Trans. Smart Grid*, 2015, **6**, pp. 1730–1739

[15] Cassidy, A., Strube, M., Nehorai, A.: 'A framework for exploring social network and personality-based predictors of smart grid diffusion', *IEEE Trans. Smart Grid*, 2015, **6**, pp. 1314–1322

[16] Hernandez, L., Baladron, C., Aguiar, J.M., *et al.*: 'A survey on electric power demand forecasting: future trends in smart grids, microgrids and smart buildings', *IEEE Commun. Surv. Tutor.*, 2014, **16**, pp. 1460–1495

[17] Ziadi, Z., Taira, S., Oshiro, M., *et al.*: 'Optimal power scheduling for smart grids considering controllable loads and high penetration of photovoltaic generation', *IEEE Trans. Smart Grid*, 2014, **5**, pp. 2350–2359

[18] Adam, G.P., Li, R., Holliday, D., *et al.*: 'Continued operation of multi-terminal HVDC networks based on modular multilevel converters'. Cigre Symp. 2015, Lund, 2015

[19] McNamara, P., Negenborn, R.R., De Schutter, B., *et al.*: 'Optimal coordination of a multiple HVDC link system using centralized and distributed control', *IEEE Trans. Control Syst. Technol.*, 2013, **21**, pp. 302–314

[20] Allebrod, S., Hamerski, R., Marquardt, R.: 'New transformerless, scalable modular multilevel converters for HVDC-transmission'. Power Electronics Specialists Conf. 2008 PESC 2008, 2008, pp. 174–179

[21] Balzani, M., Reatti, A., Salvadori, G.: 'Design, assembly and testing of modular multilevel converter with multicarrier PWM method'. 2006 Ph.D. Research in Microelectronics and Electronics, 2006, pp. 57–60

[22] Pirouz, H.M., Bina, M.T., Kanzi, K.: 'A new approach to the modulation and DC-link balancing strategy of modular multilevel AC/AC converters'. Int. Conf. Power Electronics and Drives Systems 2005 PEDS 2005, 2005, pp. 1503–1507

[23] Glinka, M., Marquardt, R.: 'A new AC/AC multilevel converter family', *IEEE Trans. Ind. Electron.*, 2005, **52**, pp. 662–669

[24] Glinka, M.: 'Prototype of multiphase modular-multilevel-converter with 2 MW power rating and 17-level-output-voltage'. 2004 IEEE 35th Annual Power Electronics Specialists Conf. 2004 PESC 04, 2004, vol. **4**, pp. 2572–2576

[25] Lesnicar, A., Marquardt, R.: 'An innovative modular multilevel converter topology suitable for a wide power range'. 2003 IEEE Bologna Power Tech Conf. Proc., 2003, pp. 1–6

[26] Glinka, M., Marquardt, R.: 'A new AC/AC-multilevel converter family applied to a single-phase converter'. The Fifth Int. Conf. Power Electronics and Drive Systems 2003 PEDS 2003, 2003, vol. **1**, pp. 16–23

[27] Jacobson, B., Karlsson, P., Asplund, G., *et al.*: 'VSC-HVDC transmission with cascaded two-level converters'. CIGRE 2010, 2010

[28] Adam, G.P., Davidson, I.E.: 'Robust and generic control of full-bridge modular multilevel converter high-voltage DC transmission systems', *IEEE Trans. Power Deliv.*, 2015, **30**, pp. 2468–2476

[29] Adam, G.P., Williams, B.W.: 'Half and full-bridge modular multilevel converter models for simulations of full-scale HVDC links and multi-terminal DC grids', *IEEE J. Emerging Sel. Top. Power Electron.*, 2014, **PP**, p. 1

[30] Vrana, T.K.: 'Review of HVDC component ratings: XLPE cables and VSC converters'. IEEE EnergyCon, Leuven, Belgium, 2016

[31] Adam, G.P.: 'Improved control strategy of full-bridge modular multilevel converter'. 2015 IEEE Electrical Power and Energy Conf. (EPEC), 2015, pp. 326–331

[32] Chao, C., Adam, G.P., Finney, S., *et al.*: 'H-bridge modular multi-level converter: control strategy for improved DC fault ride-through capability without converter blocking', *IET Power Electron.*, 2015, **8**, pp. 1996–2008

[33] SIEMENS: 'The energy transition in Germany – Siemens supplies converters for grid expansion to amprion and TransnetBW', Siemens Presentation, 2016

[34] Nami, A., Liang, J., Dijkhuizen, F., *et al.*: 'Modular multilevel converters for HVDC applications: review on converter cells and functionalities', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 18–36

[35] Rong, Z., Lie, X., Liangzhong, Y., *et al.*: 'Design and operation of a hybrid modular multilevel converter', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 1137–1146

[36] Konstantinou, G., Zhang, J., Ceballos, S., *et al.*: 'Comparison and evaluation of sub-module configurations in modular multilevel converters'. 2015 IEEE 11th Int. Conf. Power Electronics and Drive Systems, 2015, pp. 958–963

[37] Merlin, M.M.C., Green, T.C., Mitcheson, P.D., *et al.*: 'A new hybrid multi-level voltage-source converter with DC fault blocking capability'. IET ACDC2010, London, UK, 2010

[38] Luth, T., Merlin, M.M.C., Green, T.C., *et al.*: 'High-frequency operation of a DC/AC/DC system for HVDC applications', *IEEE Trans. Power Electron.*, 2014, **29**, pp. 4107–4115

[39] Wickramasinghe, H.R., Konstantinou, G., Li, Z., *et al.*: 'Alternate arm converters-based HVDC model compatible with the CIGRE B4 DC grid test system', *IEEE Trans. Power Deliv.*, 2018, p. 1

[40] Liu, S., Saeedifard, M., Wang, X.: 'Zero-current switching control of the alternate arm HVdc converter station with an extended overlap period', *IEEE Trans. Ind. Electron.*, 2019, **66**, pp. 2355–2365

[41] Adam, G.P., Finney, S.J., Williams, B.W., *et al.*: 'Network fault tolerant voltage-source-converters for high-voltage applications'. Ninth IET Int. Conf. AC and DC Power Transmission 2010 ACDC, 2010, pp. 1–5

[42] Zhang, Y., Adam, G., Finney, S., *et al.*: 'Improved pulse-width modulation and capacitor voltage-balancing strategy for a scalable hybrid cascaded multilevel converter', *IET Power Electron.*, 2013, **6**, pp. 783–797

[43] Li, R., Adam, G.P., Holliday, D., *et al.*: 'Hybrid cascaded modular multilevel converter with DC fault ride-through capability for the HVDC transmission system', *IEEE Trans. Power Deliv.*, 2015, **30**, pp. 1853–1862

[44] Xue, Y., Zhang, X.P., Yang, C.: 'Elimination of commutation failures of LCC HVDC system with controllable capacitors', *IEEE Trans. Power Syst.*, 2016, **31**, pp. 3289–3299

[45] Feldman, R., Tomasini, M., Clare, J.C., *et al.*: 'A hybrid voltage source converter arrangement for HVDC power transmission and reactive power compensation'. Fifth IET Int. Conf. Power Electronics, Machines and Drives (PEMD 2010), 2010, pp. 1–6

[46] Oates, C., Dyke, K.: 'The controlled transition bridge'. 2015 17th European Conf. Power Electronics and Applications (EPE'15 ECCE-Europe), 2015, pp. 1–10

[47] Oates, C., Dyke, K., Trainer, D.: 'The use of trapezoid waveforms within converters for HVDC'. 2014 16th European Conf. Power Electronics and Applications, 2014, pp. 1–10

[48] Adam, G., Alsokhiry, F., Abdelsalam, I., *et al.*: 'Controlled transition bridge converter: operating principle, control and application in HVDC transmission systems', *Electr. Power Syst. Res.*, 2018, **163**, pp. 98–109

[49] Li, P., Adam, G.P., Holliday, D., *et al.*: 'Controlled transition full-bridge hybrid multilevel converter with chain-links of full-bridge cells', *IEEE Trans. Power Electron.*, 2017, **32**, pp. 23–38

[50] Yang, J., He, Z., Ke, J., *et al.*: 'A new hybrid multi-level DC–AC converter with reduced energy storage requirement and power losses for HVDC applications', *IEEE Trans. Power Electron.*, 2018, p. 1

[51] Vozikis, D., Adam, G., Holliday, D., *et al.*: 'An improved alternate arm converter for HVDC APPLICATIONS'. IEEE 44th Annual Conf. IEEE Industrial Electronics S (IECON 2018), Washington, D.C., USA, 2018

[52] Adam, G.P., Li, R., Xu, L., *et al.*: 'Compact mixed cell modular multilevel converter'. 2018 IEEE Int. Conf. Industrial Technology (ICIT), 2018, pp. 646–651

[53] Li, P., Adam, G.P., Finney, S.J., *et al.*: 'Operation analysis of thyristor-based front-to-front active-forced-commutated bridge DC transformer in LCC and VSC hybrid HVDC networks', *IEEE J. Emerging Sel. Top. Power Electron.*, 2017, **5**, pp. 1657–1669

[54] Li, P., Finney, S.J., Holliday, D.: 'Active-forced-commutated bridge using hybrid devices for high efficiency voltage source converters', *IEEE Trans. Power Electron.*, 2017, **32**, pp. 2485–2489

[55] Bakas, P., Ilves, K., Harnefors, L., *et al.*: 'Hybrid converter with alternate common arm and director thyristors for high-power capability'. 2018 20th European Conf. Power Electronics and Applications (EPE'18 ECCE Europe), 2018, pp. P.1–P.10

[56] Adam, G.P., Gowaid, I.A., Finney, S.J., *et al.*: 'Review of dc–dc converters for multi-terminal HVDC transmission networks', *IET Power Electron.*, 2016, **9**, pp. 281–296

[57] De Doncker, R.W.A.A., Divan, D.M., Kheraluwala, M.H.: 'A three-phase soft-switched high-power-density DC/DC converter for high-power applications', *IEEE Trans. Ind. Appl.*, 1991, **27**, pp. 63–73

[58] Engel, S.P., Stieneker, M., Soltau, N., *et al.*: 'Comparison of the modular multilevel DC converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 124–137

[59] Soltau, N., Stagge, H., De Doncker, R.W., *et al.*: 'Development and demonstration of a medium-voltage high-power DC–DC converter for DC distribution systems'. 2014 IEEE Fifth Int. Symp. Power Electronics for Distributed Generation Systems (PEDG), 2014, pp. 1–8

[60] Soltau, N., Engel, S.P., Stagge, H., *et al.*: 'Compensation of asymmetric transformers in high-power DC–DC converters'. 2013 IEEE ECCE Asia Downunder (ECCE Asia), 2013, pp. 1084–1090

[61] Steigerwald, R.L., De Doncker, R.W., Kheraluwala, M.H.: 'A comparison of high power DC-to-DC soft-switched converter topologies'. Conf. Record of the 1994 IEEE Industry Applications Society Annual Meeting, 1994, vol. **2**, pp. 1090–1096

[62] De Doncker, R.W., Demirci, O., Arthur, S., *et al.*: 'Characteristics of GTOs and high voltage MCTs in high power soft-switching converters'. Conf. Record of the 1991 IEEE Industry Applications Society Annual Meeting, 1991, vol. **2**, pp. 1539–1545

[63] Gowaid, I.A., Adam, G.P., Massoud, A.M., *et al.*: 'Quasi two-level operation of modular multilevel converter for use in a high-power DC transformer with DC fault isolation capability', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 108–123

[64] Gowaid, I.A., Adam, G.P., Williams, B.W., *et al.*: 'The transition arm multilevel converter – a concept for medium and high voltage DC–DC transformers'. 2015 IEEE Int. Conf. Industrial Technology (ICIT), 2015, pp. 3099–3104

[65] Gowaid, I.A., Adam, G.P., Ahmed, S., *et al.*: 'Analysis and design of a modular multilevel converter with trapezoidal modulation for medium and high voltage DC–DC transformers', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 5439–5457

[66] Adam, G.P., Williams, B.W.: 'Multi-pole voltage source converter HVDC transmission systems', *IET Gener. Transm. Distrib.*, 2016, **10**, (2), pp. 496–507. Available at http://digital-library.theiet.org/content/journals/10.1049/iet-gtd.2015.0894

[67] Schon, A., Bakran, M.M.: 'A new HVDC–DC converter with inherent fault clearing capability'. 2013 15th European Conf. Power Electronics and Applications (EPE), 2013, pp. 1–10

[68] Schon, A., Bakran, M.M.: 'High power HVDC–DC converters for the interconnection of HVDC lines with different line topologies'. 2014 Int. Power Electronics Conf. (IPEC-Hiroshima 2014 – ECCE-ASIA), 2014, pp. 3255–3262

[69] Jie, Y., Zhiyuan, H., Hui, P., *et al.*: 'The hybrid-cascaded DC–DC converters suitable for HVdc applications', *IEEE Trans. Power Electron.*, 2015, **30**, pp. 5358–5363

[70] Vrana, T.K., Bell, K., Sørensen, P.E., *et al.*: 'Definition and classification of terms for HVDC networks', *CIGRE Sci. Eng.*, 2015, **3**

[71] Dirk Van, H., Oriol, G.-B., Jun, L.: 'DC grid power flow control devices', in (Eds.): '*HVDC grids: for offshore and supergrid of the future*' (Wiley-IEEE Press, 2016), p. 528

[72] Diab, H.Y., Marei, M.I., Tennakoon, S.B.: 'Operation and control of an insulated gate bipolar transistor-based current controlling device for power flow applications in multi-terminal high-voltage direct current grids', *IET Power Electron.*, 2016, **9**, pp. 305–315

[73] Mu, Q., Liang, J., Li, Y., *et al.*: 'Power flow control devices in DC grids'. 2012 IEEE Power and Energy Society General Meeting, 2012, pp. 1–7

[74] Balasubramaniam, S., Ugalde-Loo, C.E., Liang, J., *et al.*: 'Experimental validation of dual H-bridge current flow controllers for meshed HVdc grids', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 381–392

[75] Barker, C.D., Whitehouse, R.S.: 'A current flow controller for use in HVDC grids'. Tenth IET Int. Conf. AC and DC Power Transmission (ACDC 2012), 2012, pp. 1–5

[76] Cwikowski, O., Sau-Bassols, J., Chang, B., *et al.*: 'Integrated HVDC circuit breakers with current flow control capability', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 371–380

[77] Sau-Bassols, J., Prieto-Araujo, E., Gomis-Bellmunt, O.: 'Modelling and control of an interline current flow controller for meshed HVDC grids', *IEEE Trans. Power Deliv.*, 2017, **32**, pp. 11–22

[78] Hassan, F., King, R., Whitehouse, R., *et al.*: 'Double modulation control (DMC) for dual full bridge current flow controller (2FB-CFC)'. 2015 17th European Conf. Power Electronics and Applications (EPE'15 ECCE-Europe), 2015, pp. 1–9

[79] Davidson, C.C., Whitehouse, R.S., Barker, C.D., *et al.*: 'A new ultra-fast HVDC circuit breaker for meshed DC networks'. 11th IET Int. Conf. AC and DC Power Transmission, 2015, pp. 1–7

[80] Cwikowski, O., Chang, B., Barnes, M., *et al.*: 'Fault current testing envelopes for VSC HVDC circuit breakers'. 11th IET Int. Conf. AC and DC Power Transmission, 2015, pp. 1–8

[81] Smeets, R.P.P., Yanushkevich, A., Belda, N.A., *et al.*: 'Design of test-circuits for HVDC circuit breakers'. 2015 Third Int. Conf. Electric Power Equipment – Switching Technology (ICEPE-ST), 2015, pp. 229–234

[82] Kim, B.C., Chung, Y.H., Hwang, H.D., *et al.*: 'Development of HVDC circuit breaker with fast interruption speed'. 2015 Ninth Int. Conf. Power Electronics and ECCE Asia (ICPE-ECCE Asia), 2015, pp. 2844–2848

[83] Tahata, K., Oukaili, S.E., Kamei, K., *et al.*: 'HVDC circuit breakers for HVDC grid applications'. 11th IET Int. Conf. AC and DC Power Transmission, 2015, pp. 1–9

[84] Chaffey, G., Green, T.C.: 'Directional current breaking capacity requirements for HVDC circuit breakers'. 2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 5371–5377

[85] Sander, R., Suriyah, M., Leibfried, T.: 'A novel current-injection based design for HVDC circuit breakers'. Proc. PCIM Europe 2015 Int. Exhibition and Conf. for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, 2015, pp. 1–7

[86] Häfner, J., Jacobson, B.: 'Proactive hybrid HVDC breakers – a key innovation for reliable HVDC grids'. Cigre 2011 The Electric Power System of the Future-Integrating Supergrids and Microgrids Int. Symp., Bologna, 2011

[87] Callavik, M., Blomberg, A., Häfner, J., *et al.*: 'The hybrid HVDC breaker: an innovation breakthrough enabling reliable HVDC grids', ABB Grid Systems, 2012

[88] Cwikowski, O., Wickramasinghe, H.R., Konstantinou, G., *et al.*: 'Modular multilevel converter DC fault protection', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 291–300

[89] Wang, S., Li, C., Adeuyi, O.D., *et al.*: 'Coordination of MMCs with hybrid DC circuit breakers for HVDC grid protection', *IEEE Trans. Power Deliv.*, 2018, p. 1

[90] Tang, G., He, Z., Pang, H., *et al.*: 'Basic topology and key devices of the five-terminal DC grid', *CSEE J. Power Energy Syst.*, 2015, **1**, pp. 22–35

[91] Ängquist, L., Norrga, S., Modéer, T.: 'A new dc breaker with reduced need for semiconductors'. 2016 18th European Conf. Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1–9

[92] Farr, E.M., Feldman, R., Clare, J.C., *et al.*: 'The alternate arm converter (AAC) – 'short-overlap' mode operation – analysis and design parameter selection', *IEEE Trans. Power Electron.*, 2017, **PP**, p. 1

[93] Soto-Sánchez, D., Hernández, M., Andrade, I., *et al.*: 'Control of an asymmetric alternate arm converter for HVDC'. 2017 CHILEAN Conf. Electrical, Electronics Engineering, Information and Communication Technologies (CHILECON), 2017, pp. 1–6

[94] Alsokhiry, F., Al-Turki, Y., Abdelsalam, I., *et al.*: 'Multi-port converter for medium and high voltage applications'. Seventh IEEE Int. Conf. Renewable Energy Research and Applications (ICRERA2018), Paris, France, 2018

[95] Adam, G.P., Abdelsalam, I., Xu, L., *et al.*: 'Multi-tasking dc–dc and dc–ac converters for dc voltage tapping and power control in highly meshed multi-terminal HVDC networks', *IET Power Electron.*, 2017, **10**, pp. 2217–2228

[96] Zhang, X., Xiang, X., Green, T.C., *et al.*: 'Operation and performance of resonant modular multilevel converter with flexible step ratio', *IEEE Trans. Ind. Electron.*, 2017, **64**, pp. 6276–6286

[97] Kontos, E., Schultz, T., Mackay, L., *et al.*: 'Multiline breaker for HVdc applications', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 1469–1478

[98] Jehle, A., Peftitsis, D., Biela, J.: 'Unidirectional hybrid circuit breaker topologies for multi-line nodes in HVDC grids'. 2016 18th European Conf. Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1–10

[99] Guo, D., Rahman, M.H., Adam, G.P., *et al.*: 'Interoperability of different voltage source converter topologies in HVDC grids'. 15th IET Int. Conf. AC and DC Power Transmssion Systems, Coventry, UK, 2019

[100] Adam, G.P., Abdelsalam, I., Fletcher, J.E., *et al.*: 'New efficient submodule for a modular multilevel converter in multiterminal HVDC networks', *IEEE Trans. Power Electron.*, 2017, **32**, pp. 4258–4278

[101] Freytes, J., Bergna, G., Suul, J.A., *et al.*: 'Improving small-signal stability of an MMC with CCSC by control of the internally stored energy', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 429–439

[102] Xu, D., Han, M., Gole, A.M.: 'Propagation of AC background harmonics in MMC HVdc multiterminal systems due to resonances and mitigation measures', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 229–238

[103] Shinoda, K., Benchaib, A., Dai, J., *et al.*: 'Virtual capacitor control: mitigation of DC voltage fluctuations in MMC-based HVdc systems', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 455–465

[104] Cwikowski, O., Wood, A., Miller, A., *et al.*: 'Operating DC circuit breakers with MMC', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 260–270

[105] Tünnerhoff, P., Ruffing, P., Schnettler, A.: 'Comprehensive fault type discrimination concept for bipolar full-bridge-based MMC HVDC systems with dedicated metallic return', *IEEE Trans. Power Deliv.*, 2018, **33**, pp. 330–339

[106] Wickramasinghe, H.R., Konstantinou, G., Pou, J., *et al.*: 'Interactions between indirect DC-voltage estimation and circulating current controllers of MMC-based HVDC transmission systems', *IEEE Trans. Power Syst.*, 2018, **33**, pp. 829–838

[107] Hu, J., Xiang, M., Lin, L., *et al.*: 'Improved design and control of FBSM MMC with boosted AC voltage and reduced DC capacitance', *IEEE Trans. Ind. Electron.*, 2018, **65**, pp. 1919–1930

[108] Luo, L., Zhang, Y., Jia, L., *et al.*: 'A novel method based on self-power supply control for balancing capacitor static voltage in MMC', *IEEE Trans. Power Electron.*, 2018, **33**, pp. 1038–1049

[109] Wang, J., Ma, H., Bai, Z.: 'A submodule fault ride-through strategy for modular multilevel converters with nearest level modulation', *IEEE Trans. Power Electron.*, 2018, **33**, pp. 1597–1608

[110] Kong, Z., Huang, X., Wang, Z., *et al.*: 'Active power decoupling for submodules of a modular multilevel converter', *IEEE Trans. Power Electron.*, 2018, **33**, pp. 125–136

[111] Wickramasinghe, H.R., Konstantinou, G., Pou, J., *et al.*: 'Comparison of bipolar sub-modules for the alternate arm converter'. IECON 2016 – 42nd Annual Conf. IEEE Industrial Electronics Society, 2016, pp. 6482–6487

[112] Wickramasinghe, H.R., Konstantinou, G., Pou, J., *et al.*: 'Asymmetric overlap and hysteresis current control of zero-current switched alternate arm converter'. IECON 2016 – 42nd Annual Conf. IEEE Industrial Electronics Society, 2016, pp. 2526–2531

[113] Heinig, S., Ilves, K., Norrga, S., *et al.*: 'On energy storage requirements in alternate arm converters and modular multilevel converters'. 2016 18th European Conf. Power Electronics and Applications (EPE'16 ECCE Europe), 2016, pp. 1–10

[114] Zhao, C., Xu, Y., Xu, J., *et al.*: 'Optimal redundancy configuration method of wave-shaping circuits and director switches in hybrid multi-level converters'. 12th IET Int. Conf. AC and DC Power Transmission (ACDC 2016), 2016, pp. 1–8

[115] Moreno, F.J., Merlin, M.M.C., Trainer, D.R., *et al.*: 'Zero phase sequence voltage injection for the alternate arm converter'. 11th IET Int. Conf. AC and DC Power Transmission, 2015, pp. 1–6

[116] Fan, B., Wang, K., Li, Y., *et al.*: 'Module-capacitor voltage fluctuation optimization control for an alternate arm converter'. 2015 IEEE Energy Conversion Congress and Exposition (ECCE), 2015, pp. 3326–3330

[117] Li, J., Wickramasinghe, H.R., Konstantinou, G., *et al.*: 'Limitations of overlap control for energy balancing of the alternate arm converter under imbalanced ac grid conditions'. 2017 Asian Conf. Energy, Power and Transportation Electrification (ACEPT), 2017, pp. 1–6

[118] Gowaid, I.A., Adam, G.P., Massoud, A.M., *et al.*: 'Hybrid and modular multilevel converter designs for isolated HVDC–DC converters', *IEEE J. Emerging Sel. Top. Power Electron.*, 2018, **6**, pp. 188–202

[119] Li, P., Adam, G.P., Finney, S.J., *et al.*: 'Operation analysis of thyristor based front-to-front active-forced-commutated bridge DC transformer in LCC and VSC hybrid HVDC networks', *IEEE J. Emerging Sel. Top. Power Electron.*, 2017, **PP**, pp. 1–1

[120] Ren, Q., Sun, C., Xiao, F.: 'A modular multilevel DC–DC converter topology with a wide range of output voltage', *IEEE Trans. Power Electron.*, 2017, **32**, pp. 6018–6030

[121] Dey, S., Samajdar, D., Bhattacharya, T., *et al.*: 'A modular DC–DC converter topology for HVDC applications'. IECON 2017 – 43rd Annual Conf. IEEE Industrial Electronics Society, 2017, pp. 595–600

[122] Xing, Z., Ruan, X., You, H., *et al.*: 'Soft-switching operation of isolated modular DC–DC converters for application in HVDC grids', *IEEE Trans. Power Electron.*, 2016, **31**, pp. 2753–2766

[123] Belda, N.A., Smeets, R.P.P.: 'Test circuits for HVDC circuit breakers'. 2017 IEEE Manchester PowerTech, 2017, p. 1

[124] Feng, L., Gou, R., Yang, X., *et al.*: 'A 320 kV hybrid HVDC circuit breaker based on thyristors forced current zero technique'. 2017 IEEE Applied Power Electronics Conf. Exposition (APEC), 2017, pp. 384–390

[125] Majumder, R., Auddy, S., Berggren, B., *et al.*: 'An alternative method to build DC switchyard with hybrid DC breaker for DC grid', *IEEE Trans. Power Deliv.*, 2017, **32**, pp. 713–722

[126] Liu, G., Xu, F., Xu, Z., *et al.*: 'Assembly HVDC breaker for HVDC grids with modular multilevel converters', *IEEE Trans. Power Electron.*, 2017, **32**, pp. 931–941

[127] Kontos, E., Schultz, T., Mackay, L., *et al.*: 'Multi-line breaker for HVDC applications', *IEEE Trans. Power Deliv.*, 2017, **PP**, p. 1

[128] MacIver, C., Bell, K.R.W., Nedi, D.P.: 'A reliability evaluation of offshore HVDC grid configuration options', *IEEE Trans. Power Deliv.*, 2016, **31**, pp. 810–819

[129] Döring, D., Ergin, D., Würflinger, K., *et al.*: 'System integration aspects of DC circuit breakers', *IET Power Electron.*, 2016, **9**, pp. 219–227

[130] Fu, S., Xu, Y., Chen, L., *et al.*: 'The status and prospects of VSC-HVDC reliability research'. 2016 China Int. Conf. Electricity Distribution (CICED), 2016, pp. 1–6

[131] Kontos, E., Bauer, P.: 'Reactor design for DC fault ride-through in MMC-based multi-terminal HVDC grids'. 2016 IEEE Second Annual Southern Power Electronics Conf. (SPEC), 2016, pp. 1–6

[132] Tahata, K., Uda, R., Kuroda, K., *et al.*: 'Mitigation on requirement of DCCB by DC reactor for multi-terminal HVDC operation'. 12th IET Int. Conf. AC and DC Power Transmission (ACDC 2016), 2016, pp. 1–6

[133] Rahman, M.H., Xu, L., Liangzhong, Y.: 'DC fault protection strategy considering DC network partition'. 2016 IEEE Power and Energy Society General Meeting (PESGM), 2016, pp. 1–5

[134] Hajian, M., Zhang, L., Jovcic, D.: 'DC transmission grid with low-speed protection using mechanical DC circuit breakers', *IEEE Trans. Power Deliv.*, 2015, **30**, pp. 1383–1391

[135] Tahata, K., Tokoyoda, S., Kikuchi, K., *et al.*: 'Investigation of suppression effect of short-circuit current and voltage drop in multi-terminal HVDC by DC reactor'. 2015 Third Int. Conf. Electric Power Equipment – Switching Technology (ICEPE-ST), 2015, pp. 240–245

[136] Wen, W., Huang, Y., Al-Dweikat, M., *et al.*: 'Research on operating mechanism for ultra-fast 40.5 kV vacuum switches', *IEEE Trans. Power Deliv.*, 2015, **30**, pp. 2553–2560

[137] Hassanpoor, A., Häfner, J., Jacobson, B.: 'Technical assessment of load commutation switch in hybrid HVDC breaker'. 2014 Int. Power Electronics Conf. (IPEC-Hiroshima 2014 – ECCE-ASIA), 2014, pp. 3667–3673

[138] Kontos, E., Rodrigues, S., Pinto, R.T., *et al.*: 'Optimization of limiting reactors design for DC fault protection of multi-terminal HVDC networks'. 2014 IEEE Energy Conversion Congress and Exposition (ECCE), 2014, pp. 5347–5354

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