



14th Deep Sea Offshore Wind R&D Conference, EERA DeepWind'2017, 18-20 January 2017, Trondheim, Norway

## Development of a scale model of a Modular Multilevel Converters

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### Abstract

Modular Multilevel Converters are now being introduced in the power grid. Control systems for these converters are complex with many degrees of freedom. Simulation models are useful for exploring control algorithms, but there is still a need for acquiring experience from real converters. As extensive experiments on full-scale converters are not always feasible due to the cost and potential consequences, reduced-scale models that correctly reproduce the salient characteristics of the original converters are necessary. This paper describes the development of 60 kVA scaled models of modular multilevel converters with 6 halfbridge, 12 fullbridge and 18 halfbridge cells per arm, respectively. Most parameters scale naturally, but the equivalent series resistance and therefore the per-unit losses due to load current tend to increase, giving more damping of oscillation than in the full-scale reference.

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Peer-review under responsibility of SINTEF Energi AS.

*Keywords:* Modular Multilevel Converter; HVDC; scale model; laboratory model

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### 1. Introduction

A large-scale transition to renewable energy has a significant impact on the electrical power grid. This can be seen in northern Europe where many new large wind farms located in the North Sea are going to be connected to the grid via subsea HVDC cables. This and the use of HVDC transmission lines to the consumers in central Europe, leads to a significant number of HVDC converters in the grid. The large total power rating of the HVDC converters has a significant impact on the power system as converter dominated grids have different properties than traditional grids where most of the power was provided by rotating machines. Individual HVDC links may also be merged to form HVDC grids in order to handle the demands for large-scale power transmission.

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Modular Multilevel Converters (MMC) are quickly becoming the preferred choice for new HVDC implementations [1]. They are able to generate smooth AC voltages without requiring large filter components, and have an inherent energy storage capability that can be utilized to reduce propagation of power transients through the converters. As these converters are new and quite complex, it is necessary to gain insight and experience on their interaction with other components in the grid, especially in strained operating conditions and during faults.

Simulations give extensive insight, but there is still a need for experience building from the use of real converters. Full-scale MMC converters can give experience about close to normal operating conditions, but they cannot be used to perform fault condition experiments due to the potential consequences and the safety issues caused by the high power level. Such experiments can instead be done on a scaled-down laboratory grid with line equivalents and converters. This paper describes the development of a set of low power (60 kVA) scale models of MMC converters. These converters are designed for laboratory use as testbeds for converter control algorithms, and for system studies where interaction between grid components in abnormal operating conditions are investigated.

## 2. MMC converter topology

A Modular Multilevel Converter consists of a large number of series connected converter cells, each with its individual DC link capacitor (Fig 1a). The circuitry inside the cells is not exposed to the full converter voltage, so they can be made using low voltage (1- 10kV) components. The voltage across a string of cells, an arm, is determined by the number of cell capacitors that are engaged at any time, so the output voltage can be changed in small steps approaching a sinusoidal voltage without large voltage switching transients.

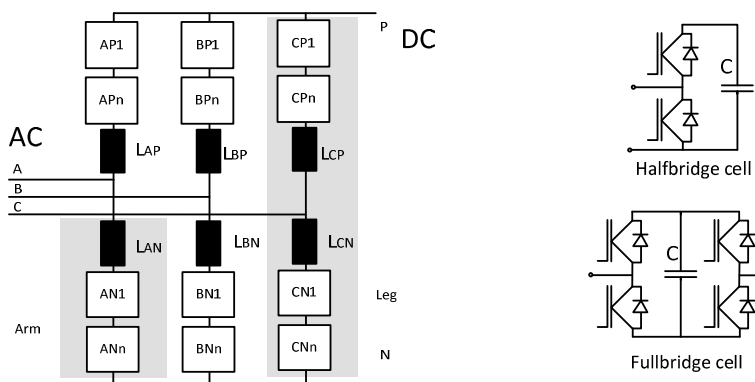


Fig. 1 (a) MMC converter topology;

(b) MMC cell topologies.

A halfbridge cell can switch its capacitor either in or out of the string, while a full bridge can insert it into the string in either positive or negative direction. A converter with halfbridge cells has unipolar arm voltage while a fullbridge converter has bipolar arm voltage (Fig 1b). This means that the DC voltage of a fullbridge converter can drop below the peak AC voltage, or even be reversed, giving the fullbridge converter an inherent ability to handle faults on the DC side without requiring a separate DC breaker. For DC grid systems, this ability may outweigh the higher losses in a fullbridge converter in some cases.

The control system is complex with a large number of switches and measurement signals. There are many degrees of freedom, giving many choices for control methods and tradeoffs between losses (number of switching actions), waveform quality, energy storage requirements, and component stress. For each arm, the sum of the cell capacitor voltages must be maintained, and the distribution of the voltages between the individual cells in an arm must be managed with a reasonable number of cell switching events. The arm currents consist of two components: one contributing to the phase output current and the other, the so-called circulating current, flowing between the different converter phases. Each of the six arm currents are controlled individually.

### 3. Simulation and laboratory models.

Laboratory and simulation models are intended to reproduce the properties of a real system, but there will always be deviations from the real system. A key factor for establishing a model is to know and to manage these deviations properly. Properties that are important for the actual case requires careful handling, while less relevant properties can be handled in a simplified way, or disregarded completely. A model that gives accurate results in one case can give very misleading results if it is used for cases where the assumptions the model is based on are stretched too far outside their validity range. Simple simulation models using ideal components and ideal conditions are useful for exploring basic properties of a system, as they are easy to manage and require short runtimes, but many important aspects are not covered by them. Complex models with detailed representation of actual components are useful for studying concrete cases, but can be difficult to manage and require long runtimes.

Power electronics converters contains a lot of complexity, both in power circuit domain and in the control system domain, so simulation models must contain many simplifications to be usable. Especially switching of power semiconductors, which involves events in the nanosecond range, requires simplifications. For power flow investigation, switching can be omitted completely by using average models [2], while more detailed studies of transients and control system behavior may use models with ideal switches.

Laboratory experiments using real hardware can be used to explore things that are difficult to model, as transformer and inductor saturation, nonlinearities in semiconductors, sampling effects in converter control systems, and EMC issues. Experiments can be used for verifying simulation models by running simulation using the parameters of the actual lab setup, and compare the results with measurements. Unexpected interactions between components in a system, especially during abnormal operating conditions, can also be revealed. The issue of underlying assumptions and simplification is present for laboratory models too, so awareness about the consequences of the omissions is crucial. Transmission level converters are fairly large and complex systems, so some simplifications are required in order to make a laboratory model feasible.

#### 3.1. Scaling

The choice of power level to be used in the scaled model is the most critical decision and is typically the result of a trade-off process where several factors are weighed against each other. Low power models are safe, have low cost, and are usually easy to operate. On the other hand, high series resistances and non-scalable auxiliary losses give significant deviations from the behavior observed on the full-scale reference case. High power models give moderate scaling effects due to their low scaling ratios, with properties close to those of the full-scale reference. However, they are expensive to build and use. Reconfiguration is also cumbersome and expensive due to size and weight of the components. They also give considerable safety issues due to large amount of energy involved.

Choice of voltage level is linked to the choice of power level, as it determines the impedances in the model. Unreasonably low or high impedances make it difficult to find suitable components and tend to give problems caused by parasitic side-effects. Voltage levels choices falls naturally in three groups:

- < 50V: Considered to be safe. Used for low power models, < ~1 kW.
- < 1000V: Governed by low voltage safety regulations.
- > 1000V. Governed by high voltage safety regulations Used for high power models, > ~1MW.

Power and voltage levels give the basis for determining the Per Unit system used for scaling the parameters:

$$S_{\text{base}} = \sqrt{3} \cdot U_{\text{ll base}} \cdot I_{\text{base}} \quad Z_{\text{base}} = U_{\text{ll base}} / (\sqrt{3} \cdot I_{\text{base}}) \quad U_{\text{base cell}} = U_{\text{ll base}} / n_{\text{cell}}$$

The converter cell parameters have a separate set of base values determined by the number of cells. The ratio between the base impedances for reference and model then determines the scaling of resistance, capacitances and inductances for the converter model.

$$Z_{\text{base cell}} = Z_{\text{base}} / n_{\text{cell}}, \quad C_{\text{model}} = C_{\text{ref}} \cdot Z_{\text{base cell ref}} / Z_{\text{base cell model}} \quad L_{\text{model}} = L_{\text{ref}} \cdot Z_{\text{base model}} / Z_{\text{base ref}}$$

It is important to be aware of scaling effects that may give deviation between reference and model, though. Many parameters, as inductance and capacitances can be scaled without major issues, but others require special attention.

Voltage drop in semiconductor devices cannot be scaled directly, but can to some extent be scaled indirectly by manipulating the number of devices in series/parallel, or using different device types.

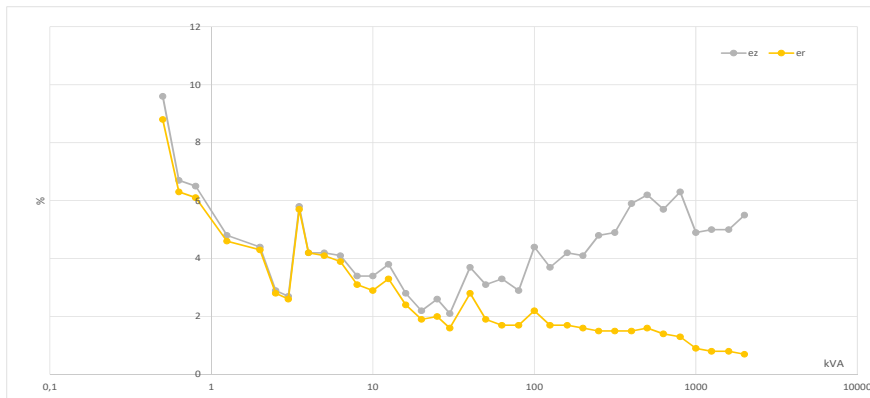


Fig. 2 Series resistance and impedance as function of power rating for low voltage transformers (Noratel 3LT-series) [3].

Series resistance, especially in inductors and transformers, does not scale as easily as the other parameters, as its per-unit value tends to increase when power rating is reduced. Resistance values picked from a catalogue for standard low voltage transformer shows this clearly in Fig 2. Inductance does not seem to have this correlation; it seems to increase with size instead. Strict scaling of resistance could be possible, but tend to give unreasonably large components.

### 3.2. Laboratory converter design

Some design aspects are specific for the laboratory converters. Separate auxiliary supply and main power circuit supply makes it possible to run the converter at near zero voltage. This is especially useful for control algorithm testing.

Sufficient design effort should be spent on topics where attention during use is unwanted. Requirements will usually change, so it is important to make a flexible design that can allow extensive modifications. This can be achieved with a modular design approach where the system is split into multiple building blocks. It is usually well worth the effort to try to look further ahead, having possible future use in mind during the design process, in order to make the modules as versatile building blocks that can easily be reused in other applications.

Design of mechanical and electrical interfaces between building blocks requires extra care, as poor design choices in the interfaces tend to give problems for a long time, as blocks often are replaced at different times, so new blocks must be designed to be compatible with the old, replicating any problems. Signals states should be defined according to a Fail-to-safe philosophy, where Enable and OK states are given by active signals. This ensures that power units are kept off, and that false OK signals are not reported when control units are unpowered or not connected. Separating control system and power circuit domain ensures that power transistor drivers, snubbers and protection circuitry can be developed and tested independent of the control electronics.

Laboratory converters are expected to be exposed to overload and fault condition experiments, so oversizing its components is generally a good practice, as it gives inherent robustness and ability to survive abuse and accidents caused by errors and misconfigurations. For scale model converters, oversizing also reduces series resistance, bringing it closer to the full-scale value. As the converters are intended to be used as platforms for development of control methods, they must be able to handle various forms of control system failures such as misconfiguration, software

crashes etc. A laboratory converter should have a protection and interlock system that prohibits illegal operations, detects overcurrent, overvoltage and overtemperature conditions and shuts it off well before any damage occurs.

## 4. Converter design considerations

### 4.1. Choice of rating

Parameters for the converters in a HVDC link between France and Spain are used as reference case for determining component values for the model converters [4].

60 kVA is chosen as nominal power for the laboratory converters. This is high enough to give representative behaviour while the equipment size and weight remain reasonable. Fault handling experiments can be performed without too far reaching consequences, as the amount of energy involved is manageable. This power level also fits well with the available laboratory infrastructure at the NTNU/SINTEF smart grid laboratory [5].

400V AC is a natural choice for rated AC voltage, being a widespread standard supply voltage level. On the DC-side, 700V DC gives reasonable headroom above peak AC voltage for control of DC load flow. The nominal cell voltage is chosen so that the sum of the cell voltages in each arm is ca 120 % of the DC link voltage, leaving headroom for cell voltage balancing. (It can be worth noting that the nominal cell voltage is not the same as the per unit base AC voltage that is used for parameter scaling.)

Table 1. Converter parameters.

Converter parameters	Reference	18 HB model	12 FB model	6 HB model
Rated power	1059MVA	60 kVA	60 kVA	60 kVA
Rated DC voltage	640 kV DC	700V	700V	700V
Rated AC voltage	333 kV	400V	400V	400V
Rated AC current	1836A	86A	86A	86A
Cells per arm	400	18 Halfbridge	12 Fullbridge	6 Halfbridge
Number of halfbridges	2400	108	144	36
Nominal cell voltage (DC)	2 kV *calculated	50V	80V	160V
Base impedance: converter / cell	105Ω / 0,26Ω	2,66Ω / 0,15Ω	2,66Ω / 0,22Ω	2,66Ω / 0,44Ω
Arm inductance	50 mH (0,15 pu)	1,5 mH (0,18 pu)	1,5 mH (0,18 pu)	1,5 mH (0,18 pu)
Cell capacitance	10 mF (1,2pu)	20 mF (1,07 pu)	15 mF (0,95 pu)	7,5 mF (0,95 pu)

Keeping the same number of cells as the reference would make the model converters very large and expensive. Nominal cell voltages would also be very low, resulting in unfeasible requirements for series resistances in the cells. Too low number of cells would, on the other hand, give large distortion in the output voltage and current waveforms, and not give a realistic representation of the properties of a full-scale converter. A trade-off based on these considerations led to the choice of number of cells for each variant of the model converters. Values for nominal cell voltages, inductances and cell capacitances are found using per unit calculations, and then adjusted to give a good fit to the available components. Resulting parameters are given in Table 1.

#### 4.2. Power circuit components

The IGBTs used in a full-scale converter have a forward voltage drop in the 2V range per transistor, regardless of current and voltage ratings. Scaling of cell voltages give voltage drops in the 100 mV range for the model converters. IGBT's are therefore replaced by low ohmic power MOSFET's. The intrinsic body diode in power MOSFET transistors has poor switching characteristics, so MOSFETs types with enhanced body diodes are required here. Devices rated for 150V and having an on-state resistance of about 5 mOhm were selected for the 12 and 18 cell converters, while 250V transistors with 15 mOhm on-state resistance were selected for the 6 cell converter. Five transistors in parallel give forward voltage drops that matches the scaling requirements quite well, and give good overload current capability. Transistor switching, especially body diode reverse recovery snap off, are very fast events even though the switching frequency is low. This means that PCB layout is extremely critical in order to obtain proper current sharing during switching of the parallel MOSFETS.

As the five parallel MOSFETs would give very large short-circuit current, the transistor drivers are equipped with a conduction voltage drop monitor that trips the converter at a fairly low threshold voltage. A trip level of 0.7 V gives peak circuit currents of ca 700A, which is manageable without excessive overvoltage transients.

The constant forward voltage drop in IGBTs could have been modelled by inserting antiparallel rectifier diodes in series with each arm. This was not done due to the added losses, though.

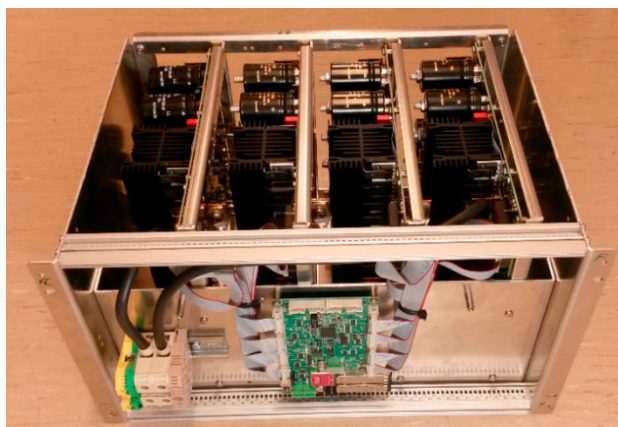
Foil capacitors have low internal resistance and are well suited at the voltage level of full-scale converter cells. However, they were considered to be too large and expensive for the model converters, so electrolytic capacitors were used instead, despite their higher losses. The capacitance values determined by the scaling operation were quite low for electrolytic capacitors, so the ratio between internal resistance and capacitance became an important selection criterion for capacitor types. Multiple parallel small can capacitors gave reasonable series resistance.

#### 4.3. Converter hardware

Three different converters were made: Two converters with a high number of cells per arm, one with 12 fullbridge cells and one with 18 halfbridge cells, intended for staircase modulation; one converter with a fairly low number of cells, 6 halfbridges, intended for pulse width modulation.



Fig. 3. (a) 12 level full bridge converter;



(b) A power cell group module.

All converter variants share a common hardware design. The basic building block is a power cell board which consists of two independent halfbridges, equipped with components for 50V, 80V or 160V nominal cell voltage, and configured either as two halfbridges in series, or as a single full bridge (Fig 4a). A group of three to four power cell boards are mounted in a module equipped with a local control board, the group control board (Fig.3b). Power and signal connections are located at the front of the module, in order to make connection work easy when modules are mounted back to back in a 19-inch cabinet (fig. 3a). Arm inductors, power terminals and AC switchgear are located in the bottom of the cabinet. The switchgear consists of a main contactor, a precharging circuit and interlock circuitry. The 12 and 18 cell converters consist of two cabinets; one cabinet contains common equipment and power cell modules for one phase while the second contains power cell modules for two phases. Auxiliary components and wires are oversized whenever it is considered reasonable, in order to keep the efficiency not too much lower than a full scale converter.

#### 4.4. Control system structure

The converter control system has a hierarchical structure, based on FPGAs with embedded processors. The power cell board does not contain any control system functions except basic interlock and protection functions. Measurement and protection functions for cell capacitor voltage and heatsink temperature are also located here. The core of the group control board is a small FPGA with an embedded soft processor. This board generates and distributes control signals to the drivers and gathers measurements and status signals from all the power cell boards in the module. It also distributes 24V supply to the power cell boards.

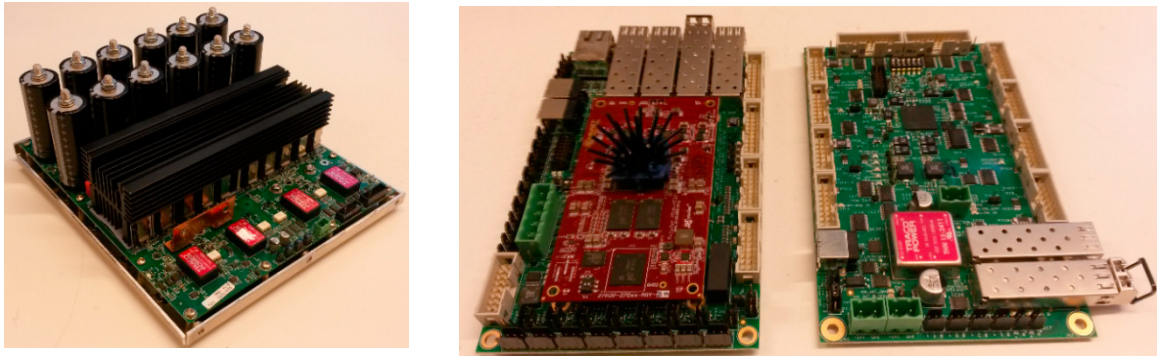


Fig. 4. (a) Power cell board;

(b) Converter control board (left) and group control board (right)

The converter control board is designed as a general-purpose converter control board based on a PicoZed7030 System On Chip module, featuring on the same chip two independent ARM-A9 processor cores with embedded peripherals and a large FPGA (user-programmable logic area) section (fig 4b). An eight channel 40 MHz AD converter allows high oversampling rates and use of control algorithms that require low signal latency. This board gathers arm currents, AC and DC voltage measurements, and controls the AC grid connection switchgear.

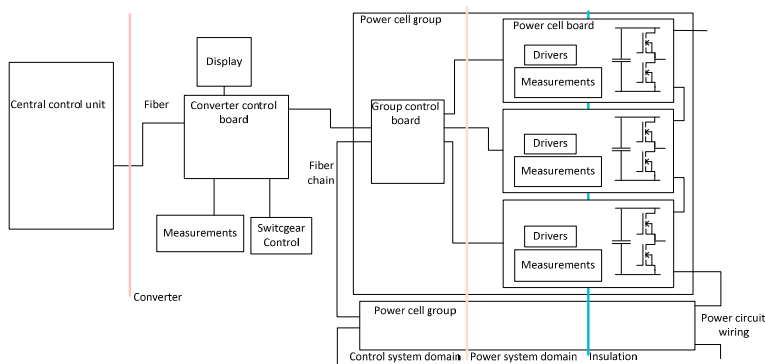


Fig. 5. Converter control system structure

A chain of fiber links provides communication between the group control boards and the converter control board (Fig 5). The chain structure is based on the Aurora point-to-point protocol that is developed by Xilinx. A high bitrate, 3,75 Gbit/s, allows transfer of large amounts of data with a high update rate. Using a chain instead of direct links drastically reduces the number of signal lines to the converter control unit, but increases the latency, the signal delay through the chain. This is critical for converter control loops, so in order to minimise latency each node in the chain forwards incoming data directly to the next Aurora link without any unpacking and repackaging. Each node also reads the incoming packets, and transmits its own packets when the link is not busy. The link management protocol also allows for strict synchronisation of all group control boards that are responsible for cell switching.

The converter control board receives control signals from an external control units through a separate fiber link. In normal operation mode the converter receives setpoint values that govern AC and DC line voltage and power flow. In development mode, the external unit can handle some of the converter control functions; state control and protection functions are however retained by the converter control board, avoiding serious failures in case of faulty behaviour of the external controller.



In the current implementation, the external controller is an OPAL-RT unit. This is a real-time Hardware in the Loop emulator platform featuring multiple processor cores and a large FPGA that are programmed and controlled using Matlab/Simulink environment.

## 5. Results

An initial test where a single converter phase drives an RL load shows that the modular multilevel converter models work as intended (Fig. 6b). During this test, the two arms runs at 100% modulation, without any circulating current control, and with a simple cell voltage sorting algorithm that determines which cells are engaged and disengaged in order to balance the cell voltages. Oscilloscope shots show that the cell string voltages change in steps from the bottom of the sine waves where no cells were engaged to the top where all cells were engaged (Fig 6a). The distorted voltage at the top of the voltage sine waves and the large 2.harmonic component in the arm current is due to the charging and discharging of the cell capacitors. Simulation of the test circuit gave similar waveforms, thus confirming correct operation of the system.

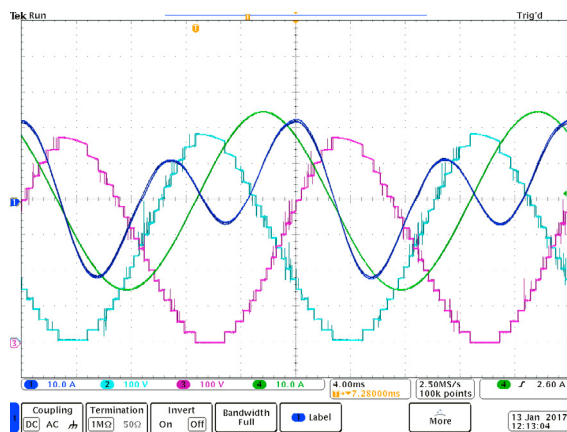
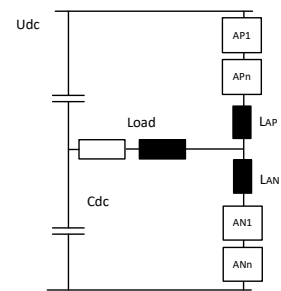


Fig. 6 (a) Single phase testing of 18 level converter. Ch1: Iarm, Ch2, Ch3: Uarm, Ch4: Iload.



(b) Test circuit

These converters are quite large compared to two-level converter with similar rating. They contain a large number of components; the control system must handle a large number of measurements and control signals as the 12 level fullbridge converter contains 144 bridgelegs. The modular design makes it quite straight forward to rearrange or extend the converters into other topologies such as, for instance, AC-AC converters with nine arms.

This converter design can also be a start point for developing converters with higher power and voltage rating. The existing low voltage power cell boards is then replaced with converter modules with higher voltage and current rating and sufficient insulation to ground, while the control system can be used without any major changes.

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