Short-Circuit Making of Medium Voltage Load Break Switches Using a Grid Connected Test Circuit

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***Abstract*—The load break switch is an important component in the distribution grid. Besides its capability to break load currents reliably, it has to be able to make short-circuit currents according to the IEC 62271 standard. In this paper, the process of making a short-circuit current and the used test methods are described. A synthetic test circuit using semiconductors instead of a triggered spark gap is proposed and described thoroughly. The basic working principle has been validated with simulations in Simulink.**

***Index Terms*—making, synthetic testing, load break switch**

I. Introduction

In a modern electrical power system, renewable power sources necessitate a more flexible electrical grid. In secondary distribution systems, load break switches provide a cost efficient solution for controlling loads. A load break switch is a mechanical switch, which is able to operate under normal grid conditions, i.e. able to conduct and break load currents [1]. There are several types of load break switches, which differ mainly on the principle of breaking load currents. The simple way is to use the dielectric and quenching capabilities of the insulating gas, e.g. SF_6. Another common way to extinguish the arc is to use ablation of an insulating medium, using the hartgas to quench the arc [2]. Designs that are more complex rely on forced cooling of the arc using puffer volumes or external pressure vessels [2],[3]. Nowadays, load break switches are constructed with separate arcing and main contacts to combine different material properties, especially low contact erosion for the arcing contact and high conductivity for the main contacts [2]. The rated voltage for a load break switch is in the range between $1\,\mathrm{kV}$ and $52\,\mathrm{kV}$ [4], with a rated current up to $1250\,\mathrm{A}$.

In addition to the capability of reliably interrupting load currents, the load break switch has to be able to close under short-circuit conditions (peak current typically up to $63\,\mathrm{kA}$). Furthermore, it has to withstand a high current of up to typically $25\,\mathrm{kA}$ for at least $0.2\,\mathrm{s}$, according to the IEC 62271 standard [5]. The common methods to validate the making capabilities of a switch involve synthetic test circuits. These are usually relying on triggered spark gaps to make the high current. A new approach is investigated, replacing the triggered spark gap with diodes.

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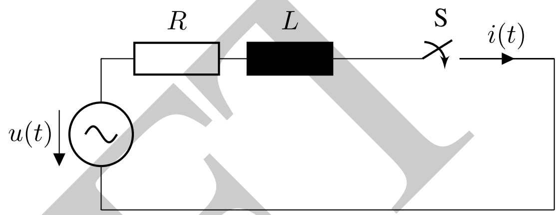

Fig. 1. Equivalent circuit to calculate the short-circuit current

II. Making of Short-Circuit Currents

The turn-on (making) process can be described with the simplified circuit in Figure 1. Without loss of generality, it can be assumed $u(t) = \hat{V}\cos(\omega t)$.

In case of a short-circuit, the grid voltage and the grid impedance consisting of R and L determine the prospected current. At a time t_0, a closing command is sent to the switch. As the distance between the contacts decreases, a dielectric breakdown occurs at the instant t_1, called pre-strike. This process strongly depends on the contact movement, the dielectric properties of the contact system and the governing voltage. For simplification, it is assumed that the switch is an ideal insulator before t_1 and an ideal conductor after t_1. The contact touches at t_2. To describe the current fully, the governing equation has to be solved:

$$L\frac{di}{dt} + Ri = \hat{V}\cos(\omega t), \tag{1}$$

$$\tau = \frac{L}{R}. \tag{2}$$

Here, $\hat{V}$ is the amplitude of the grid voltage, ω is the angular frequency of the grid, L is the stray inductance and R is the parasitic resistance. The time constant τ equals typically $45\,\mathrm{ms}$

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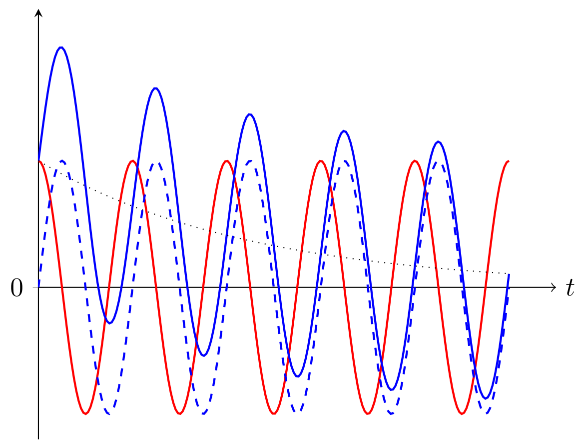

Fig. 2. Asymmetric (full blue) and symmetric (dotted blue) making current with the grid voltage (red)

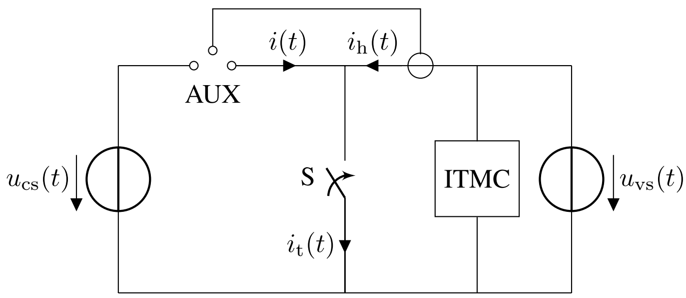

Fig. 3. Basic principle of a synthetic making test according to IEC 62271 (Part 101) [6]

[6]. With minor simplifications, solving equation (1) leads to the following current

$$i(t) \approx \frac{\hat{V}}{\omega L}\left(\sin(\omega t) - \sin(\omega t_1)e^{-\frac{t-t_1}{\tau}}\right) \quad (3)$$

The current is composed of two parts, shown in Figure 2. The first part describes the periodic behavior in steady state conditions. The second part describes the transient behavior directly after the pre-strike. The impact of the exponential decay is determined by the time of pre-strike t_1 in relation to the phase of the grid voltage. Two extreme cases exist. In the first case ($\omega t_1 = k \cdot \pi, \forall k \in \mathbb{N}_0$), the prestrike takes place at the peak of the driving voltage, leading to symmetric current, as the exponential term in (3) equals zero. The pre-strike arc burns from t_1 until the contact close t_2. The other extreme case is a contact touch at $\omega t_1 = \omega t_2 = \frac{\pi}{2} + k \cdot \pi, \forall k \in \mathbb{N}_0$. Here, the driving voltage has its zero crossing and the contacts touch without arcing. The exponential term has its maximum, which leads to an asymmetric current. The energy dissipated during arcing calculates to

$$W_{\text{arc}} = \int_{t_1}^{t_2} u_{\text{arc}}(t) i(t) dt, \quad (4)$$

where u_{arc} is the arc voltage. A high contact speed is desirable to keep $\Delta t = t_2 - t_1$ low. For the pre-strike happening at the peak of the driving voltage, it can be shown that an increase in contact speed from $1\,\mathrm{m/s}$ to $5\,\mathrm{m/s}$ results for a typical system in a decrease of $96\,\%$ of the pre-arcing time [1].

III. Testing of Making Capabilities

Apart from the possibility of direct testing, which requires an available high input power, the IEC 62271 (Part 100 [5] and 101 [6]) standard regulates the required parameters for synthetic making tests and provides the basic principle of a test circuit (Figure 3). For the synthetic test circuit, usually three main components can therefore classify the topology. Beside the voltage source u_{vs} and the current source u_{cs}, the high current making switch AUX plays a crucial role. It has to be fast enough in making the high current with a short delay and to conduct the high current. The initial transient making current (ITMC) is preferably supplied by the high voltage source. The IEC 62271 standard suggests the use of a triggered spark gap as a making switch.

Analog to the synthetic breaking tests of a circuit breaker, the high current part is separated from the high voltage part. First, the high voltage leads to the pre-strike across the contact gap. Afterwards, the high current part feeds the occuring arc with energy. Three main intervals during testing are defined:

1) *High Voltage Interval*: the time from the beginning of the test, with fully opened contacts until the moment of breakdown of the contact gap t_1. The applied voltage can be an AC source, a DC source or a combiantion of both. In case of an AC source, the phase shift between the high voltage and the high current source has to fulfill additional conditions.
2) *Pre-arcing Interval*: the time between the moment of breakdown t_1 and the touching of the contacts t_2. In other words, the time of the pre-strike, ending with a first galvanic contact. The current is the superposition of three components: the ITMC, typically provided by the high voltage source and the DC and AC component of the current supplied by the high current source. The ITMC describes the "transient current which flows through the circuit-breaker at the moment of voltage breakdown prior to the initiation of current from the current circuit during making" [6]. The injected current has to flow until the auxiliary making switch is turned on. The ITMC should be limited to a duration of $300\,\mu\mathrm{s}$ before the current from the high current side starts to flow. During the pre-arcing interval, the switch is exposed to high electrodynamic forces due to the current and to deterioration of the contacts due to the arc-energy. The arcing leads to a pressure rise in an encapsulated switch. The drive system of the switch has to be able to close reliably under these conditions.
3) *Latching Interval*: the time during the closing stroke from the touching of contacts (t_2) to the moment t_3 when the switch is fully closed. During this interval the switch is opposed to high electrodynamic forces due to the current and to contact friction forces.

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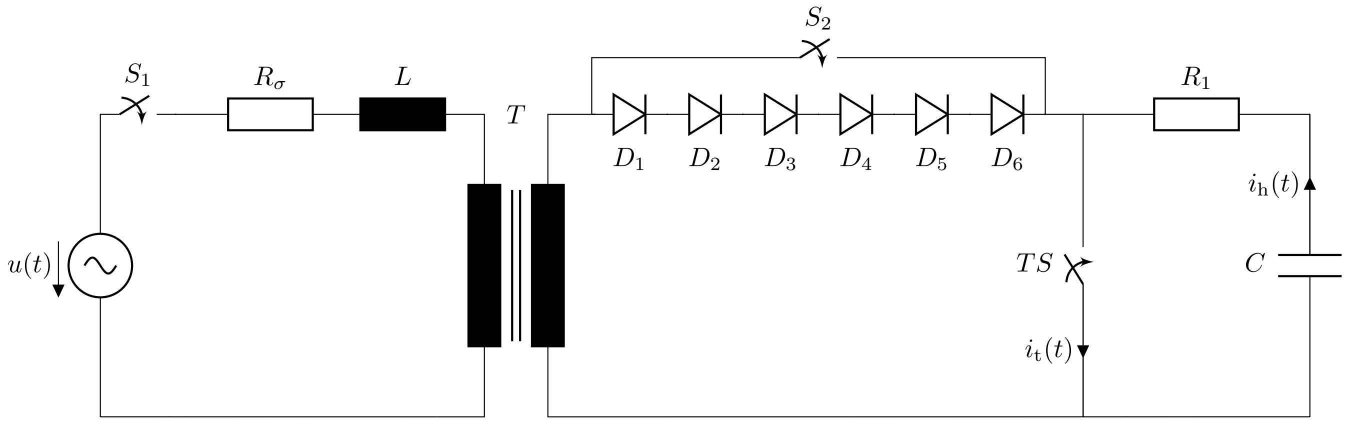

Fig. 4. Proposed test circuit

The contact welding has to be limited to assure an opening operation after closing on a short-circuit. The symmetrical case with higher pre-arcing times increases the stress on the switching device but decreases the peak mechanical forces, as the current peak is lower [7].

Several topologies exist to perform type tests and support the design of new switches. The high voltage for the pre-strike is usually supplied by a pre-charged capacitor. This DC voltage is then applied across the contact gap of the switch (e.g., [7]). Another possibility is to use a high voltage AC source [8]. The high current is supplied by short-circuit transfomers (e.g., [7],[8]).

Another distinction is the number of phases which are tested simultaneously. Following the IEC standard, it is sufficient for a three-pole switch to run single-phase tests. In some cases for the single-phase testing it can be needed to take the first-pole-to-clear factor into account. The influence of the contact speed and the first-pole-to-clear factor in a three-phase system on the making behavior has been described in [7].

IV. Proposed Circuit

The designated laboratory for the making tests is located at the Norwegian University of Science and Technology in Trondheim, Norway. It offers a high-current transfomer directly connected to the medium voltage grid. The key parameters of the transfomer are despicted in Table I. The transformer has different tap settings and the option of connecting the windings in parallel or series. This results in different possible nominal currents and voltages, indicated with the values in parenthesis. Figure 4 shows a proposed circuit. It is similiar to the typical used circuits in testing facilities. The specific element is the high current making switch. It consists of six diodes in series (D_1-D_6) with a commercially available vaccum breaker in parallel (S_2). The use of a spark gap instead is compounded by the low output voltage of the high current transformer. Table II shows the rating and specifications of the circuit elements. Noteably is the use of the surge current capability of the diodes, which explains the need of a parallel mechanical switch. It is important to use a surge arrester to protect the high-current transformer in case of a misoperation. It has to be capable of dissipating the energy stored in the high-voltage capacitor. The current limiting inductance on high voltage side of the transformer has multiple tap settings.

To explain the behavior of the test circuit, it is convenient

TABLE I
Transformer Parameters

Rated Specifications	
Apparant Power	3000 kVA
Frequency	50 Hz
Input Voltage	$6.6\,\mathrm{kV}{+}3\cdot5\%\text{-}2\cdot5\%(\Delta)$
	$11.43\,\mathrm{kV}{+}3\cdot5\%\text{-}2\cdot5\%$ (Y)
Output Voltage	115 V/230 V (Δ)
	697 V/398 V (Y)
Input Current	262.4 A (Δ)
	151.5 A (Y)
Output Current	15 061 A (115 V)
	2485 A (698 V)
Measured Parameters (115 V)	
e_z	3.43 %
e_r	0.83 %
Measured Parameters (698 V)	
e_z	4.09 %
e_r	0.66 %

TABLE II
Circuit Elements

Diodes	
Blocking Voltage (V_{RRM})	4.2 kV
Rated Current (I_{FAVM})	3470 A
Surge Current Capability (I_{FSM})	63 kA
Passive Elements	
R_1	200 Ω
C	100 nF
R_σ	0.18 Ω-0.89 Ω
L	9.5 mH-101 mH

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to look at the timing of the different switches and the current and voltage waveforms repectively. First, the high current side switch S_1 is turned on. The potential difference across the diodes is

$$u_\mathrm{D}(t < t_1) = u_\mathrm{cs}(t) - U_\mathrm{C} < 0 \quad (5)$$

due to the precharging of the high voltage capacitor C. This leads to a blocking state of the diodes for both positive and negative half cycle of the high current side. After closing S_1, the transformer will magnetize the main inductance.

Afterwards, two parallel closing commands to the test switch TS and the auxiliary vacuum breaker S_2 are sent. To compensate different making speeds of TS and S_2, a delay t_θ between the two closing commands is introduced. S_2 is supposed to conduct current shortly after TS, not later than $10\,\mathrm{ms}$. At the pre-strike instant t_1, the test switch starts to conduct and the diode voltage is

$$u_\mathrm{D}(t > t_1) = u_\mathrm{cs}. \quad (6)$$

The diode voltage u_D becomes positive in the positive half cycle of u_CS and the diodes start to conduct current, feeding the pre-arcing in the test switch with energy from the high current transformer. It is therefore crucial that the pre-strike in TS occurs in the positive half cycle of u_CS. Beside this limitation, the circuit shows the advantages of not relying on a pre-strike current detection, as proposed in the IEC standard, and a negligible voltage drop across the diodes in conducting state. With a certain jitter, the vacuum breaker S_2 will close in the first half-cycle of the high current. The current through the diodes will commutate to S_2 and limit the dissipated losses in the semiconductors.

After the needed amount of high current periods, an opening command to S_1 is sent to break the current.

Simulations with Simulink Simscape give a validation of the approach (see Figure 5). The current shows a minor asymmetry when commutating to the mechanical switch. This is explained by the different conductivity of switch and diodes. In reality, the timing between the closing of TS and S_2 can be challenging. If S_2 closes too early, the full voltage of the precharged capacitor is connected to high-current transformer. A surge arrestor protects the transformer in this case. If S_2 closes too late, the diodes stop conducting the current after the first positive half cycle and S_2 will make the current again at a later instant, when TS is (nearly) galvanically closed. If S_2 closes too late or not at all, the diodes start conducting a second half-cycle and will be thermally destroyed. This case has to be avoided by any means. Besides the timing, the voltage distribution across the series connected diodes has to be controlled. For this purpose, parallel connected high ohmic resistors will be connected in parallel to the diodes.

V. Conclusion

A new approach for the synthetic testing of the making capabilities of load break switches is discussed. Following the IEC 62271 standard, the basic processes during the making operation are described. To model these conditions, a test circuit using semiconductors has been proposed and simulated in Simulink Simscape. Its main advantage is the inherent high-current triggering and the low forward voltage drop, compared to the use of pre-strike triggered spark gap.

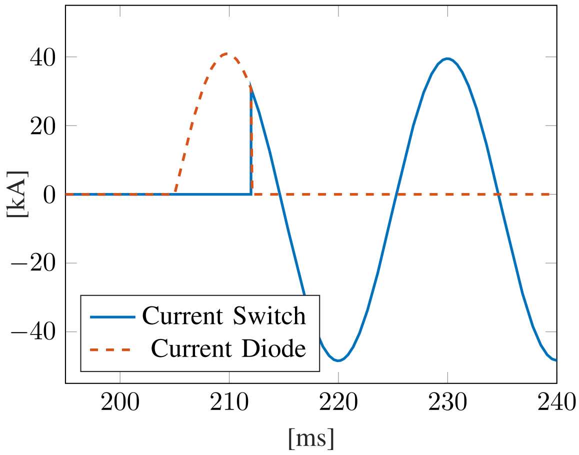

Fig. 5. Simulation of the making process

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