Interoperability of Modular Multilevel Converters and 2-level Voltage Source Converters in a Laboratory-Scale Multi-Terminal DC Grid

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***Abstract*-The prospect of future multivendor HVDC systems has led to concerns about interoperability between converter terminals based on different technologies. This paper investigates the interoperability of converter terminals in a small-scale experimental setup, consisting of two 2-level (2L) Voltage Source Converters (VSCs) and two Modular Multilevel Converters (MMCs) with different number of half-bridge sub-modules in each arm. The laboratory setup is utilized to demonstrate interoperability of a 2-level VSCs and an MMCs when operated in parallel on the dc-side as well as in parallel at a common connection point in an ac grid. Experimental results are presented for the investigated 4-terminal configuration with one 2L VSC controlling the dc voltage and all other converters controlling their active power flow. The presented results give an additional empirical confirmation that topological differences between properly designed converter terminals should have limited influence on system level operation and system interoperability of MT HVDC systems.**

Keywords— Interoperability, HVDC Transmission, Modular Multilevel Converter, Power-Hardware-in-the-Loop

I. INTRODUCTION

HVDC transmission based on Voltage Source Converter (VSC) technology is presently an established solution for interconnecting weak ac networks and for grid connection of far-offshore wind farms [1], [2]. With the introduction of Modular Multilevel Converters (MMCs) [3], VSC-based HVDC transmission is also becoming a viable option for bulk power transfer [4], [5]. Due to the flexibility and controllability of VSC technology, is also suitable for operation of Multi-Terminal (MT) HVDC grids [6]-[8]. Two examples of MT HVDC grids based on VSC terminals are already in operation in China [9], [10]. However, these two installations have been designed, constructed and commissioned as MT HVDC systems by an integrated process with a predefined topology and functionality.

Future multi-terminal HVDC grids in Europe are expected to be a result of gradual expansion from point-to-point transmission schemes. Thus, European Transmission System Operators (TSOs) require that future MT HVDC systems should be based on a technical foundation allowing for multi-vendor solutions in a similar way as in traditional ac systems. For reliable operation of such multi-vendor systems it is critical to ensure interoperability between installations from different manufacturers [6], [7], [11]. This implies that HVDC converter stations commissioned separately at different times during the development of a MT HVDC system should be able to operate together without causing problems due to differences in topologies or control system implementations.

In principle, interoperability should be ensured in any power system where two or more converters can interact. Indeed, the term "interoperability" includes many different aspects, from selection of voltage levels and component interfaces to control system compatibility. The potential causes for operational incompatibility in a multi-vendor system are also numerous, and can have different implications in practical and theoretical terms. However, in the context of HVDC transmission, the concerns regarding converter interoperability seems to have increased substantially with the introduction of the MMC, which has expanded the number of possible configurations and topologies that can potentially coexist in the same system. An example of simulation-based analysis for confirming successful interoperability of HVDC converter terminals with different topologies was provided in [11].

Considering that interoperability between component ratings and interfaces can be easily ensured in MT HVDC systems, it is useful for practical convenience to differentiate between interoperability issues associated with the converter topology and interoperability aspects related to the control strategies. Indeed, the theoretical framework and the tools suitable for analysis of these two critical aspects of interoperability will differ significantly. For example, investigation of potential interoperability issues related to operation of different converter topologies in the same system would require very detailed models, which in practice restricts the analysis to time-domain simulations or experimental testing, as in [11], [12], [13]. By contrast, it can be expected that interoperability issues related to the control strategies of

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the HVDC converter terminals, and especially interactions associated with the outer control loops and their tuning can be analyzed by average models, as discussed in [14]-[19].

Considering mainly the concerns of interoperability between different converter topologies in a MT HVDC system, this paper presents experimental results from a few selected cases that demonstrate interoperability of different VSC topologies. Thus, the paper attempts to advance from the experimental investigations presented in [12] and [13]. While successful operation of a point-to-point configuration combining a 2L VSC and an MMC terminal was demonstrated in [12], a multiterminal dc grid configuration based on 2L VSCs but with capability for Power-Hardware-in-the-Loop (P-HiL) simulation of the ac-side systems was presented in [13]. In this paper a four-terminal dc grid with two 2L VSCs and two MMCs with different number of half-bridge sub-modules, created within the Demo 1 of the BestPaths project is introduced [20]. According to the experience matured with the demonstrator and the test results presented in this paper, the VSC multiterminal configurations did not exhibit any interoperability issues due to the differences in the topologies. This gives an additional empirical evidence supporting that topological differences between properly designed converter terminals will have limited influence on system level operation and system interoperability of MT HVDC systems.

II. System Topologies and Control of VSC HVDC Converter Terminals

Although continuous research activities are being devoted to the improvement of design and control strategies for VSC-based HVDC converters, the basic control principles for HVDC terminals connected to large-scale ac systems are well established. For the investigations in this paper it is assumed that the converter stations will be operated by conventional vector-oriented control strategies that are synchronized to the ac grid voltage by a traditional Synchronous Reference Frame (SRF) Phase Locked Loop (PLL) [21]. A brief introduction to the assumed implementations for 2L VSCs and MMCs in the system configuration investigated in this paper is presented in the following.

A. Topology and control system for 2L VSCs

Fig. 1 shows an overview of the basic topology and control structure assumed for 2L VSCs. In addition to the 2-level topology, the system typically includes an LCL-filter (or another high order filter topology) on the ac-side and a relatively large capacitor on the dc-side [21]. The control system is usually based on an ac-side inner loop current controller in a synchronously rotating *dq* reference frame synchronized to the ac grid by a PLL [21]. The PLL detects the grid frequency, which is used in the decoupled PI current controllers, and the phase angle of the voltage measurements, which is needed for transformations between the stationary and synchronously rotating reference frames of the control system [21], [22].

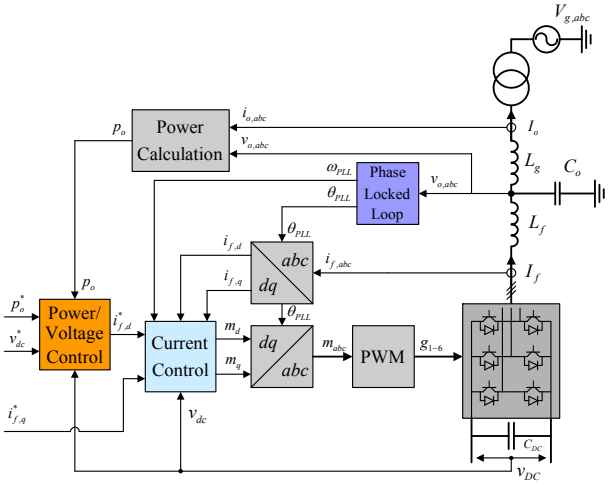

Fig. 1. Overview of assumed control system for 2L VSCs

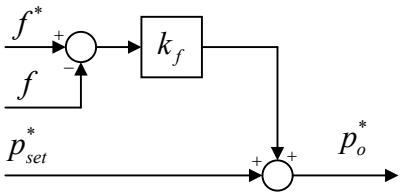

Fig. 2. Frequency droop controller

The control structure in Fig. 1 shows a general scheme where an outer loop controller regulates either the ac power or dc-side voltage by generating the active, d-axis, current reference to the inner loop current controller. In both cases, the outer loop is assumed to be based on a simple PI controller. It should be noted that an active power droop can easily be included in the dc voltage controller, or a dc voltage droop could be included in the power controller [16], [23]. For simplicity, operation with a single converter terminal controlling the dc voltage will be assumed in the following, while all other terminals will be operated with ac-side power control. However, it will be considered that an HVDC converter station can participate in the primary frequency control of the ac-grid [25], [24]. Thus, a frequency droop acting on the power reference for the control system can be introduced as shown in Fig. 2.

In this paper, the reactive q-axis current on the ac-side of the converter terminal is controlled to zero, implying unity power factor operation at the point of synchronization to the grid. However, a reactive power controller or an ac-voltage controller could easily be included in the control structure [21]. A reactive power controller could also be operated with an ac voltage droop, or an ac voltage controller could be operated with a reactive power droop. Such control system configurations would be most important in relatively weak ac systems and will not be explicitly studied in this paper.

B. Topology and control system for MMCs

An overview of the system topology and assumed control structure for MMCs is shown in Fig. 3. As can be seen from the figure, the MMC is assumed to be connected directly to the ac system without any capacitive filter. Furthermore, the MMC topology does

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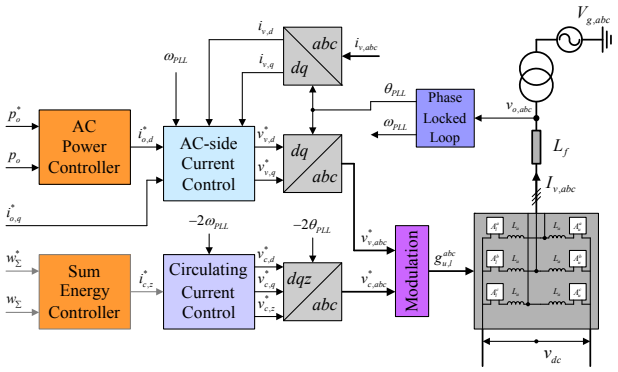

Fig. 3. Overview of assumed control system for MMCs

not depend on any capacitor at its dc-side terminals [3]. As also shown in Fig. 3, the assumed MMC control system has two parallel paths, for regulating the ac-side currents and the internal circulating currents, respectively. The ac-side control scheme is generally identical to the control scheme for the 2-L VSC from Fig. 1. Only an ac-side power controller will be considered in this paper as shown in Fig. 3 and it will be assumed that the reactive q-axis current component in the ac side will be controlled to zero. Nevertheless, the MMC could be also operated with the same combinations of control objectives and droop functions as outlined for the 2-L VSC.

From in Fig. 3, it can be seen that the ac-side current controllers generate the ac-side voltage references v^*_v, while the circulating current controller provides the internal voltage references v^*_c for each phase of the converter. These two voltage components are combined by a modulation strategy to generate a modulation signal for each arm of the MMC. The modulation strategy for an MMC can be implemented in several different ways, depending on whether the modulation signal is compensated for the continuous voltage oscillations in the total sum arm voltages or not [19]. In this paper, it is assumed that the modulation indices for upper (u) and lower (l) arm of the MMC are calculated by a division with the dc voltage as:

$$n_{u,k} \approx \frac{-v^*_{v,k} + v^*_{c,k} + v_{dc}}{v_{dc}}, \quad n_{l,k} \approx \frac{v^*_{v,k} + v^*_{c,k} + v_{dc}}{v_{dc}} \qquad (1)$$
$$for \quad k \in \{a,b,c\}$$

The modulation signals resulting from (1) are used as input to a capacitor voltage balancing algorithm which will generate the gate signals of each individual sub-module of the MMC [3].

The circulating currents of the MMC are assumed to be controlled by a Circulating Current Suppression Controller (CCSC) according to [26]. Thus, the second harmonic component of the internal circulating currents of the MMC are controlled to zero by a set of decoupled PI current controllers in the negative sequence double frequency SRF, as shown in the upper part of Fig. 4.

If only the double frequency dq components of the circulating currents are controlled to zero, the dc components of the circulating currents and the total capacitor voltage in each arm of the MMC will be left uncontrolled. Thus, they will stabilize in steady-state operation according to the power flow, the dc-side

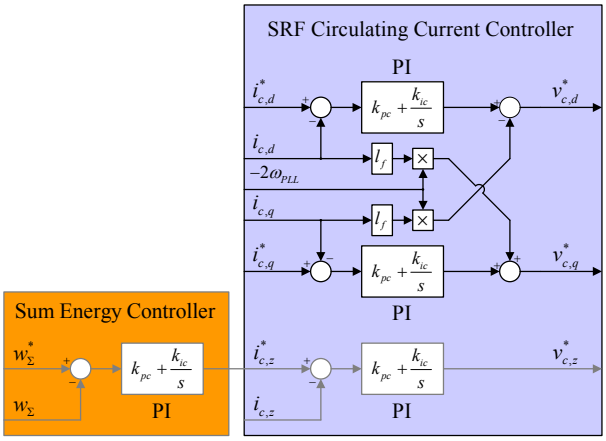

Fig. 4. Circulating current control of MMC

voltage and the equivalent resistance of each phase of the MMC. However, the dc-component of the circulating currents can be utilized to regulate the total energy stored in the internal capacitors of the MMC. Thus, the total arm voltage can be decoupled from the dc voltage of the converter.

A simple way to obtain control of the total energy stored in the MMC is to use a sum energy controller that provides a reference value for controlling the zero-sequence component of the circulating currents [27]. The corresponding controller implementation is shown in grey in the lower part of Fig. 4, where a PI controller is used to regulate the total energy stored in the MMC by providing a zero-sequence current reference. The feedback signal for the total energy can be calculated directly from the total capacitor voltages, as assumed in this paper, or it can be estimated from the currents and modulation signals of the MMC. If the sum energy controller is utilized, the zero-sequence component of the circulating currents must be regulated to its reference value. As shown in Fig. 4, this can be easily achieved with a PI current controller providing the zero sequence component of the internal voltage reference $v^*_{c,z}$.

III. Multi-Terminal DC System Configuration and Experimental Prototypes

The experimental setup utilized in this paper is based on results from a demonstration activity within the "BEST PATHS" project [20] supported by the European Union FP7 program. The studied configuration is installed in the National Smart Grid Laboratory of Norway [28]

A. System configuration of experimental setup

The investigated configuration represents a four-terminal dc grid interconnecting three asynchronous ac systems as represented in Fig. 5. Moreover, the setup includes a real-time simulator and a 200 kW high bandwidth grid emulator (EGSTON-COMPISO). This configuration allows for imposing controlled steady-state or transient conditions and offers the possibility for Power-Hardware-in-the-Loop (P-HiL) testing for investigating interoperability issues of MT HVDC systems. The two MMC-based terminals have different topologies and their control systems are based on

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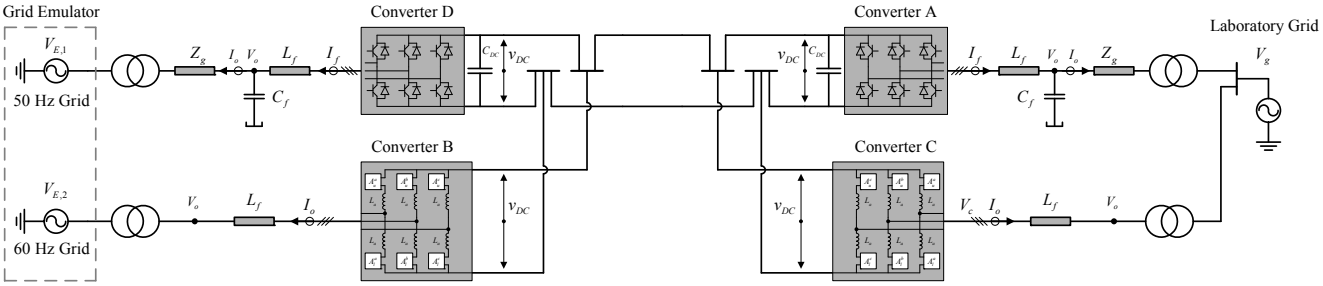

Fig. 5. Overview of MT DC grid configuration used for laboratory experiments

TABLE I AC GRID SPECIFICATION OF LABORATORY SETUP

AC grid	Rated voltage $V_{S,LL,RMS}$	Frequency	Converter Terminals
Laboratory grid, V_g	400 V	50 Hz (Nordic freq.)	A, C
Grid Emulator, V_{E1}	400 V	50 Hz (Regulated)	D
Grid Emulator, V_{E2}	400 V	60 Hz (Regulated)	B

different strategies for regulating the total energy stored within the internal capacitors.

The studied configuration is intended to trigger possible interoperability issues between the different converter topologies, on the dc-side and on the ac side. It consists of two 2L VSCs, denoted as Converter A and Converter D, and two MMCs denoted as Converter B and Converter C. All converters are connected in parallel on the dc side, forming a four-terminal dc grid. However, on the ac side, only Converter A (2L VSC) and C (MMC), with their associated transformers and filters, are connected in parallel to the same point in the power supply system available in the laboratory. Thus, these two converters operate at the frequency of the Nordic power system. The other two converters, Converter B (MMC) and D (2L VSC), are connected to independent ac grids established by the grid emulator to have a regulated grid frequency of 60 Hz and 50 Hz, respectively. Thus, three asynchronous ac systems are included in the experimental setup, as summarized in Table I.

For operating the system, Converter A acts as a slack-bus on the dc-side, since it is regulating its dc voltage, while the remaining three converters are power-controlled with references for the active (d-axis) current component generated by the outer loop active power controller. Furthermore, Converter B has a frequency droop controller that changes the power reference as a function of the deviation in the frequency of the associated ac grid according to Fig. 2. In all converters, the reactive (q-axis) current is controlled directly with a zero reference.

An OPAL-RT real-time simulator is utilized to implement the higher-level control of the converters and to coordinate their operation. The time step for both MMC and 2L converter controllers in the OPAL-RT was 100 µs. In addition, the real-time simulator controls the operation of the grid emulator, which was used to emulate two independent asynchronous ac grids with 50 Hz and 60 Hz frequency according to Fig. 5 and Table I.

B. Converter Prototypes

The converter units are custom-designed prototypes intended for laboratory-scale testing, and are rated for 60

Fig. 6. Overview of MMCs and view of a converter cell

TABLE II PARAMETERS OF THE VSCS AND ASSOCIATED GRID FILTER

Parameter	Value	Parameter	Value
Rated ac voltage $V_{S,LL,RMS}$	400 V	Filter inductance l_f	0.05 pu
Rated dc voltage V_{dc}	700 V	Filter resistance r_{Lf}	0.01 pu
Rated power S_b	60 kVA	Filter capacitance c_f	0.05 pu
Power controller gain: k_{pp}, k_{ip}	1, 10	Grid side inductance l_g	0.02 pu
DC voltage controller gain: k_{pvdc}, k_{ivdc}	10, 100	Grid side resistance r_g	0.01 pu
Current controller gain: k_{pc}, k_{ic}	0.5, 65	DC capacitance, c_{dc}	4 pu

kVA at 400 V ac (line-to-line RMS) and 700 V dc. The two 2L VSCs are identical in construction and are based on Semikron integrated IGBT modules. The converter terminals include an LCL filter on the ac side and a dc bus capacitor with parameters specified in the Table II. The control of the converters is implemented entirely in the OPAL-RT platform according to the scheme presented in section II. Indeed, the OPAL-RT platform contains a custom programmed FPGA, which is dedicated to sampling and conditioning of the measurements and to the generation of the gate signals. Conventional carrier-based PWM with third harmonic injection and 10 kHz switching frequency is applied.

The two MMC units are based on MOSFET half bridge cells and are connected without any external output filter or dc bus capacitor. The converters have been intentionally designed with different number of cells (i.e. Converter B and C have 18 and 6 cells per arm, respectively) to further expose potential interoperability issues associated with differences in the topology. This reflects in slight differences in the ratings of the power components mounted in each cell, due to the differences in the rated cell capacitor voltages A picture of main experimental setup showing the cabinets of the MMC prototypes and the power hardware of the MMC cells is shown in Fig. 6. The main design parameters for the two MMCs are summarized in Table III. Further information about the MMC prototypes and how they are designed to

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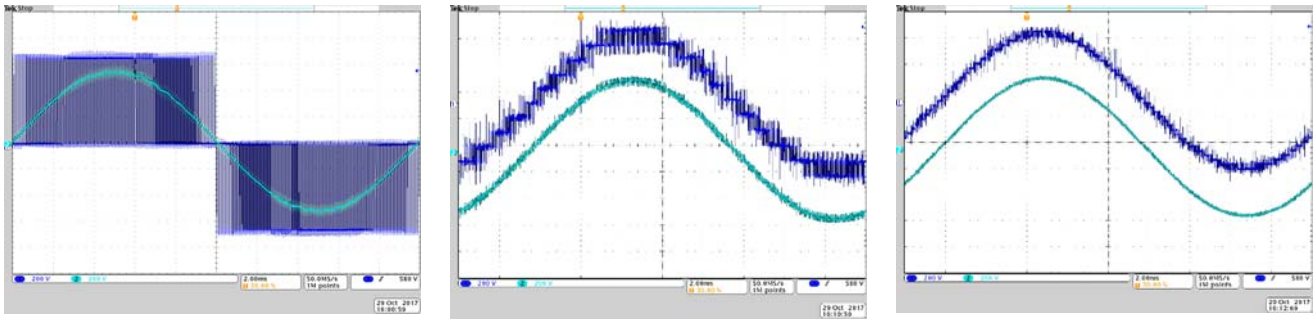

(a) 2L VSC (Converter D) (b) 6 level MMC (Converter C) (c) 18 level MMC (Converter B)

Fig. 7. Voltage wave forms before and after ac filter for all the different converter types

TABLE III
MAIN PARAMETERS OF THE REDUCED-SCALE MMC PROTOTYPE

Converter parameters	**6 HB model**	**18 HB model**
Name	*Converter C*	*Converter B*
Rated ac voltage $V_{S,LL,RMS}$	400V	400V
Rated dc voltage V_{dc}	700V	700V
Rated power S_b	60 kVA	60 kVA
Cells per arm	6 HB	18 HB
Nominal cell voltage	133V	44V
Arm inductance	1.4 mH	1,4 mH
Cell capacitance	5.9 mF	21.3 mF
Power controller gain: k_{pp}, k_{ip}	5e-4, 0.02	5e-4, 0.02
Current controller gain: k_{pc}, k_{ic}	0.5, 100	0.5, 100
Energy controller gain: k_{pc}, k_{ic}	-	1, 10
Circulating current controller gain: k_{pc}, k_{ic}	2, 100	2, 100

represent scaled models of a relevant HVDC terminal is available in [29].

The control hardware of the MMC prototypes is designed with a three-level hierarchical structure. At the lowest level, the cells are grouped into sets of 6, with each set connected to a local controller generating the gate signals of the 12 individual devices. These local controllers are daisy-chained with a fiber-optic link and connected to an upper layer controller responsible for controlling the two arms of a single phase. This controller implements the capacitor voltage balancing algorithms for selecting the cells to be switched within each arm. Finally, the three leg controllers are again daisy-chained and connected with an optical link to the OPAL-RT unit that implements the current controls, the grid synchronization and any other outer loop controllers.

IV. LABORATORY DEMONSTRATION OF AC- AND DC-SIDE INTEROPERABILITY OF 2L VSCS AND MMCS

This section presents experimental results obtained from the presented multiterminal configuration. As an example of converter interoperability, the configuration described in the previous sections was operated to transfer power between the three ac grids with the control modes and operating conditions already described in section III. It should be noted that for the following experiments, Converter B has an energy controller to regulate the total energy stored in the MMC, while Converter C has only a controller for the double frequency *dq* components of the circulating currents.

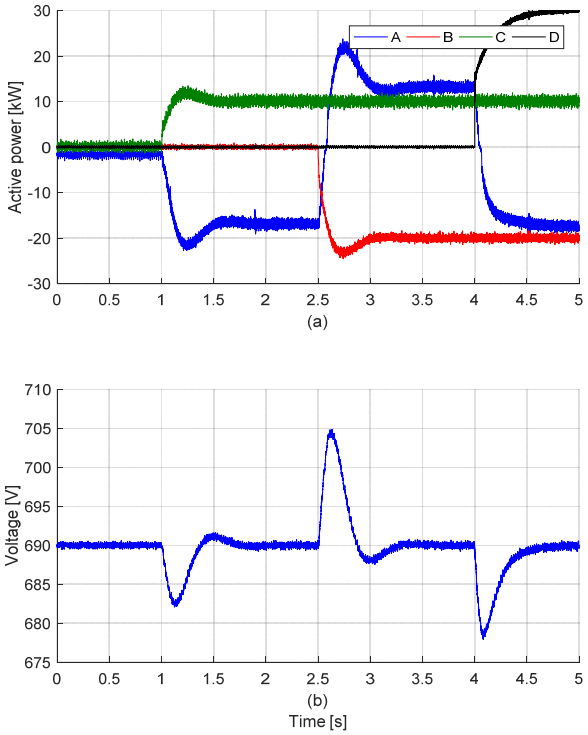

Fig. 8. (a) Measured active power on the ac side for all converters, and (b) Measured dc voltage

A. Steady-state operation

Fig. 7 shows oscilloscope screen-shots of the line-to-line voltage before the inductive output filter and after the filters, i.e. at the converter output terminals. The voltage in Fig. 7 (a) clearly highlights the characteristics of a 2L converter with the line-to-line voltage switching between the dc bus voltage and zero. In contrast, the voltages in Fig. 7 (b) and (c) present the behavior of a multilevel converter with clearly visible smaller steps corresponding to the cell voltage. It should be noted that the MMCs are not operated with nearest level modulation as commonly used for MMCs with hundreds of cells per arm: instead one cell in each arm is operated in PWM to reduce the THD of the voltage.

The expected steady state operation was observed, with power flow inside the dc grid and a net exchange of power between the different ac grids. For the specific choice of the references for the active power controlled converters (i.e. references equal to zero), the converter acting as a slack bus is operating with only a small active current to compensate for the system losses.

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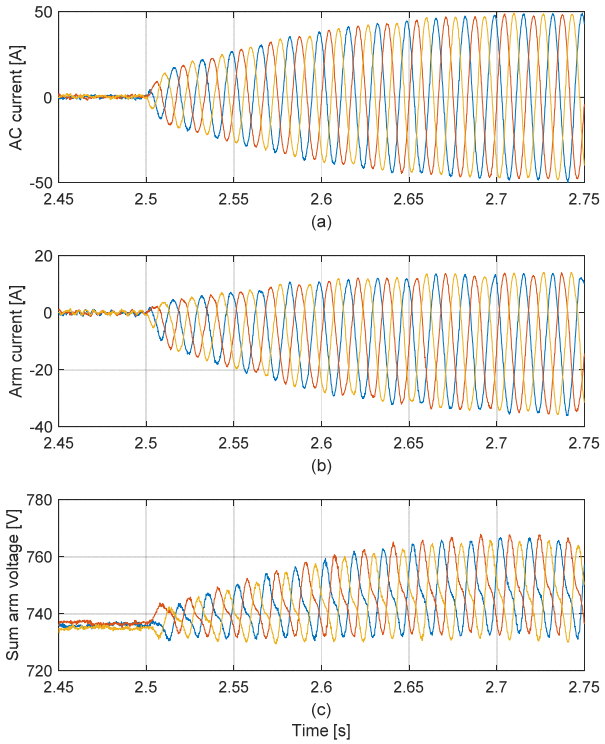

Fig. 9. MMC Converter B (a) AC currents, (b) upper arm currents in each leg, and (c) sum of upper arm voltages in each leg

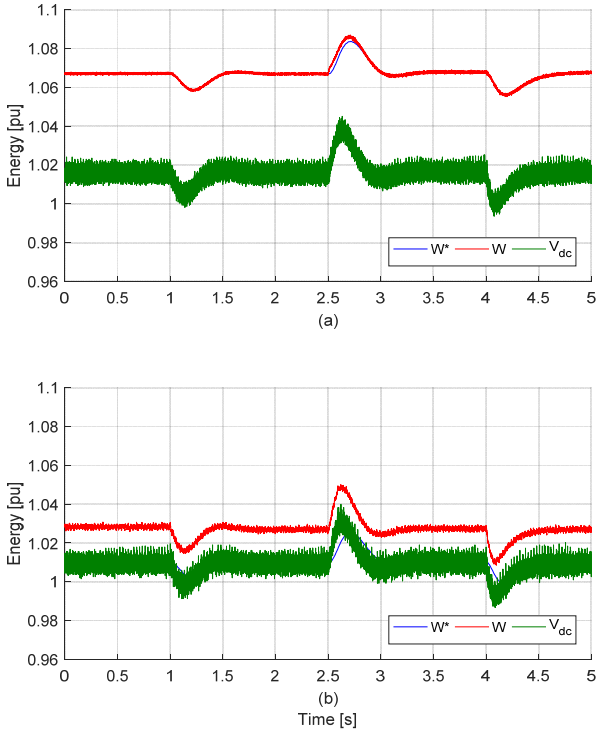

Fig. 10. Reference energy, measured energy, and dc voltage for MMC (a) Converter B, and (b) Converter C

B. Transient response

For further assessing potential interoperability issues, a test was performed to highlight the transient performances of the system in response to a step change in the active power references, as shown in Fig. 8 (a). Initially, all active power controlled converters were operated with zero reference, and the converter acting as a slack bus is operating with low active power to compensate for the system losses. The active power reference in MMC Converter C was changed from 0 to 10 kW at t = 1s. To compensate the power imbalance in the dc grid, the dc-voltage controlled Converter A changes its power flow. The power references in Converter B and Converter D were stepped from 0 to -20 kW and 30 kW at t = 2.5s and t = 4s, respectively. Note that power flowing out of a converter and into an ac grid is defined as positive. The measured powers reach steady state within about 0.5 s after the step of the power setpoint. The dc voltage disturbance caused by change in power flow is effectively rejected by the dc voltage controlling Converter A, as shown in in Fig. 8 (b), achieving smooth and stable operation. It can be noted that the transient response resulting from a change in the power reference for Converter D is different from the response when the power reference is changed for Converter C or D. This is mainly because the power controlled 2L VSC has different parameters and a different tuning of the active power controller than the MMCs.

Fig. 9 shows currents and voltages for Converter B. The transients in ac currents when the power reference of the converter is changed are shown in Fig. 9 (a). The arm currents and sum voltages for the upper arms of each leg/phase are shown in Fig. 9 (b) and (c), respectively. The average value of the arm currents goes below zero as the power reference is negative. The sum of the arm voltages increases as the change of power flow causes the dc voltage to increase during the transient period (in Fig. 8 (b)). The currents and voltages in all phases remain balanced throughout the transient.

In Fig. 10, the total sum energy for Converter B and C MMCs are presented, scaled to per unit quantities by using the dc voltage of each converter as the base value. As mentioned, Converter B has an energy controller that generates a reference for zero sequence current as explained in [27], while Converter C only has circulating current suppression controller according to [26]. In this case, the energy reference for Converter B is set to be proportional to the square of the measured dc voltage. Thus, the sum energy reference follows the dc voltage dynamics, and the total energy stored in the MMC is accurately following this reference. This ensures a higher voltage margin for the control of the ac-side currents. If the energy reference was kept constant, this would also effectively decouple the total sum energy stored in the MMC from the dc-voltage in the multiterminal dc grid. The energy sum in Converter C is, however, following the dc voltage dynamics with only a small margin resulting from the peak value of the internal voltage oscillations of the cell capacitor voltages. The difference in the control strategy for the two MMCs do not have any noticeable influence on the other converters operating in the DC-grid.

C. Operation with grid frequency droop-control

As different power systems are being connected to each other through HVDC links, the frequency reserve needed to stabilize a synchronous system does not need

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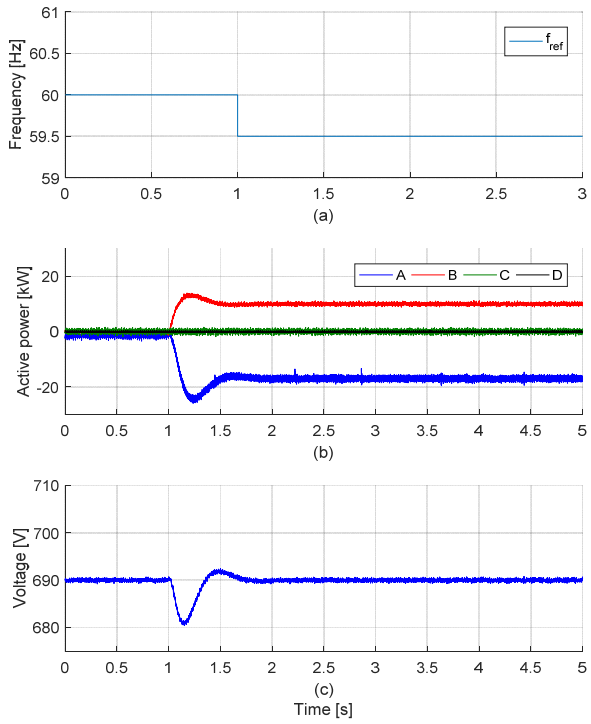

Fig. 11. (a) reference frequency, (b) active power at all converter terminals, and (c) dc grid voltage

to be only provided locally but can also partially supplied by the HVDC connection. Thus, an HVDC system can contribute to the primary frequency regulation by modifying the power flow at the converter terminal based on change in locally measured ac grid frequency. The active power controller of Converter B was modified as shown in Fig. 2 so that the converter participates in frequency control of the connected ac grid.

A frequency disturbance in the emulated ac grid V_{E2} was created by reducing the frequency reference of the grid emulator from 60 Hz to 59.5 Hz at t = 1s, as indicated in Fig. 11(a). This event caused the power flowing through Converter B to change from 0 to 15kW, resulting in increased power flow from the dc grid into the ac grid as shown in Fig. 11(b). To compensate for the change in power flow in the dc grid and the related change in dc voltage, Converter A changes the power flow and regulates dc grid voltage as shown in Fig. 11(b) and (c), respectively.

D. General observations

Considering the presented results, the experimental tests did not reveal any interoperability issues due to the differences in the converters topologies. Moreover, no undesired control interactions between the converters were observed for the simplified control schemes assumed for the different converter terminals. It should be noted that these results were obtained with four converters connected in parallel on the dc-side. This could be considered the potential worst case for direct interaction between the converter topologies since there is no significant impedance between the dc terminals of the different units. However, it should be kept in mind that long HVDC cables or lines can have internal resonance frequencies. Thus, any interoperability issues or stability problems caused by the physical systems in such configurations would more likely result from interactions between a converter and the remaining electrical system than from any interaction caused by differences in topologies.

V. Conclusion

In this paper, the interoperability between converters in a multiterminal configuration has been considered from an empirical perspective based on the experience matured with a reduced-scale four-terminal dc grid with two 2L converters and two MMCs. First, the steady state operation of the dc grid with one 2L converter operating as a slack-bus in dc-voltage control mode has been presented. Then the transient behavior of the system in response to a change in active power flow or to a frequency step in the ac system was investigated. In general, no interoperability issues that could be associated to the differences in the converter topologies have been observed during the tests.

The configuration investigated in the paper included two identical 2L VSCs and two MMCs with different number of levels and inner controls. However, the experimental results do not indicate any noticeable interoperability aspects associated with the topology. The most noticeable differences in the response appeared to be related to the tuning of the voltage and current controller and to the presence of droop functionalities. Indeed, the topological characteristics are essential for the design of the hardware, the development of the internal controllers and all the aspects that are associated to the converter dynamics. However, in a system perspective the differences in the topology are less relevant except for elements like the presence of an output filter or of a bus capacitor. This would seem to justify the studies approaching the interoperability of outer loop control strategies by applying average models and techniques based on linearization for modal analysis.

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