Comparative Analysis of Modulation Techniques for Modular Multilevel Converters in Traction Drives

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***Abstract*—The spreading of electric vehicles led to a renewed interest for innovative traction drives. In this context, an electric traction drive based on a Modular Multilevel Converter and integrating batteries in each module has been recently proposed. This converter concentrates into a single unit, the control of the traction motors, the balancing and energy management of the battery cells and the vehicle recharge functions. By using different modulation techniques it is possible to optimize different aspects like efficiency or THD of output current and voltages. Performance and efficiency in balancing, traction and recharging operations have been analyzed for two modulation techniques: near level modulation and phase disposition PWM. The near level modulation reduces switching losses while the second one better follows voltage references reducing current THD and, consequently, conduction losses. In this paper an innovative modulation technique is proposed and its performance in terms of current THD and global losses are compared with the other two modulation strategies already proposed.**

***Index Terms*—DSCC, Multilevel Converter, Cascaded H-bridge, Modulation Technique, Automotive Converter.**

I. Introduction

In recent years electric vehicles (EVs) are spreading on the market. While hybrid EVs are commercialized since the end of the 90s, only in the last 5 years battery EVs (BEVs) have been really exploited and they are now commercialized by all the major car manufacturers. As a consequence, a great effort has been devoted to study new solutions for motor and traction drives and to improve performances and efficiency of these vehicles [1] [2] [3].

Usually, BEVs are equipped with two or three power converters to accomplish the following main functions:

1) Deliver power to the traction motor;
2) Balance the cells of the battery pack;
3) Recharge the battery pack.

The first function is performed by the traction drive, the second one by the battery management system (BMS) and the third one by the charge unit that only in some configurations is installed on-board. A solution where the three main functions above discussed are integrated in a single modular multilevel converter with batteries embedded at cell level has been proposed in [4]. Balancing capabilities of this converter have been analysed in [5] while the recharge operation has been studied in [6]. The feasibility of this idea has been proven by means of a small prototype [7], while in [8] the balancing techniques have been optimized with attention to the efficiency of the converter. Finally, in [9] the low frequency operation of this converter has been analyzed. However, no analysis specifically oriented to the effect of the modulation techniques has been performed yet. In particular, in all the cited papers a traditional phase disposition multi-carrier PWM (PDPWM) has been considered [10] [11]. In this paper a comparison between PDPWM and nearest level control (NLC) is performed in terms of THD of motor voltage and current and global efficiency of the traction drive. Moreover, a new modulation technique is proposed and compared with the above mentioned. The new modulation technique is ideated starting from the consideration that, for sinusoidal reference, NLC well fits the required voltage around the zero while a worse approximation is obtained near the maximum and minimum values. On the contrary, PWM better approximates the reference but requires a higher number of switching transitions. The proposed technique operates like NLC for all the required output except when the maximum reference voltage for that speed is required since only in this case PWM is applied to one battery module. Thus, the voltage reference is accurately followed reducing the number of required switching operations. In order to compare the three modulation techniques a traction drive is assumed as reference in the paper and results of numerical simulations are reported and commented.

II. Converter Description

A. Topology

The modular multilevel Double Star Chopped Cells (DSCC) whose topology is reported in Fig. 1 is based on a modular multilevel converter (MMC) structure in which capacitors have been substituted with batteries [4]. The analyzed converter has a leg for each phase of the load to be fed. Each leg is composed by an even number of chopper-cells divided equally in upper and lower arms. A coupled inductor is placed in the load point of connection between the two arms to permit power sharing between different legs [12].

In this paper the virtual dc bus voltage is defined as the voltage between positive and negative busbars. The phase voltage of each leg is measured using as reference potential half the virtual dc bus voltage starting from the negative busbar. In Fig. 2 employed conventions are summarized.
The output voltage applied to the load is produced turning on and off upper and lower arm cells and generating references

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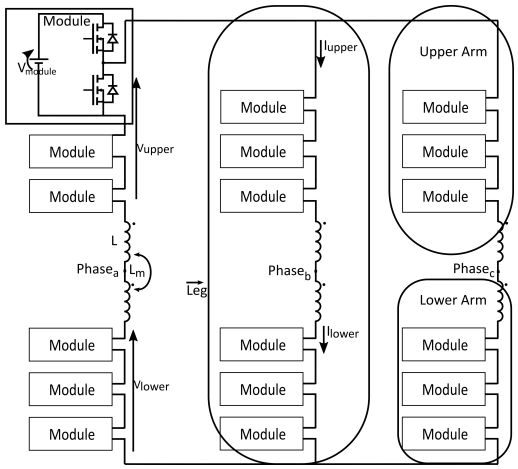

Fig. 1. DSCC converter topology

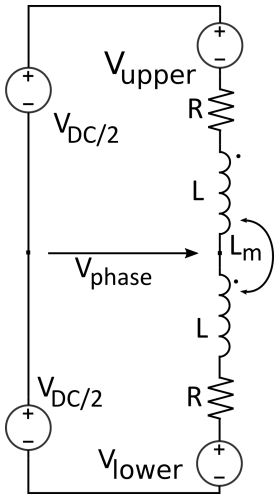

Fig. 2. References convenctions

in order to maintain the required virtual dc bus voltage as constant as possible. Thus, the total number of active modules between upper and lower arms has to be kept constant.

B. Case Study

Since this converter is intended for automotive applications the simulations are performed feeding an asynchronous motor whose parameters are summarized in table I.

The machine is controlled with a V/Hz strategy between 1 and the base frequency of 150 Hz, while above the base frequency the speed is increased at constant voltage. The converter is simulated with 9 modules per arm each of which is composed by a stack of 5 lithium-ion cells with a total nominal voltage of 18.5 V. This configuration allows a theorethical maximum output line voltage of 115 V, high enough to let the selected motor to reach its nominal power. The solid state switches employed for simulations are IRL40SC228 [13], chosen because of their low conduction resistance and their high current rating. Their main parameters are summarized in Table II.

As discussed in the introduction, the balancing algorithm has been already analyzed in previous papers where its effectiveness has been demonstrated. Since this paper focuses on modulation techniques, stacked cells within each modules are assumed to be always equalized at the same state of charge (SoC). Module open circuit voltage (OCV) characteristics have been approximated with a simple linear model (1):

$$V_{module} = 5 \cdot (3 + 1.2 \cdot SoC) \tag{1}$$

where 5 is the number of stacked cells within a module and SoC is the actual state of charge of the module. The chosen SoC for simulations is 0.85 corresponding to a cell voltage equal to 4.02 V. Batteries internal losses and voltage drops due to internal resistance have been neglected because it is not the focus of this study.

C. BMS Capabilities

During converter operation (even with no output phase voltage) it is possible to perform BMS functions to maintain all the modules at the same SoC. The balancing process is composed by three parts [5] [7]:

1) Module Balance
2) Leg Balance
3) Arm Balance

The module balancing process equalizes all the modules within each arm. To perform this task the controller computes the order in which modules have to be activated depending on instantaneous arms current direction and modules $SoCs$. When the current would charge the batteries then the least charged elements are activated first, when the current would discharge the modules then the most charged ones are prioritized.

The second balancing function changes virtual dc_{bus} voltage references for each phase in order to control the dc components of circulating currents and transfers energy from the most charged leg to the least ones. At the end of its operation all the legs will be at the same mean SoC.

The last balancing function is necessary to balance the upper and lower part of each leg. To transfer power between the arms, circulating currents are again employed: controlling the virtual dc bus references it is possible to generate

TABLE I
SIMULATED ASYNCHRONOUS MACHINE PARAMETERS

Parameter	Value
P_n [kW]	50
V_n [V]	108
pole pairs	2
$cos(\phi_n)$	0.88
f_{base} [Hz]	150
η_n	0.87

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TABLE II
SUMMARY OF IRL40SC228 MAIN PARAMETERS

Parameter	Value
U_{d0} [V]	1.2
R_{dson} [mΩ]	0.65
t_{rise} [ns]	210
t_{fall} [ns]	176
t_{don} [ns]	67
Q_{rr} [nC]	45

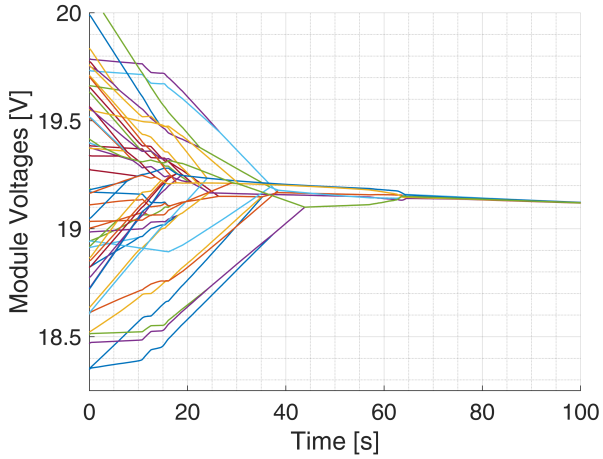

Fig. 3. Module voltages during balancing operations.

alternating circulating currents with the same frequency of the output phase voltage. Modifying the phase of those currents a power flows from upper to lower or from lower to upper arms. Fig. 3 reports a qualitative plot of how cells converge to the same SoC after being initialized with an unbalance level randomly generated between 0.55 and 0.85. The simulations were performed with a 80 kWh battery pack and feeding the motor of table I at 100 Hz with V/Hz control moving a mechanical load with a torque of 106 Nm.

III. MODULATION TECHNIQUES

In this section the three modulation techniques analyzed in the paper are explained in details. The reference signals for the upper and the lower arm of each phase are obtained independently by the modulation technique. With the conventions of Fig. 2 and neglecting voltage drops on inductors and on parasitic resistances, the relations defining the voltage references are (2) and (3):

$$\begin{cases} V_{phase,k} = \frac{1}{2}\left(V_{lower,k} - V_{upper,k}\right); \\ V_{dc,bus,k} = V_{lower,k} + V_{upper,k}; \end{cases} \tag{2}$$

$$\begin{cases} V_{lower,k} = \frac{V_{dc,bus,k}}{2} + V_{phase,k}; \\ V_{upper,k} = \frac{V_{dc,bus,k}}{2} - V_{phase,k}; \end{cases} \tag{3}$$

where $V_{phase,k}$ is the generic phase reference output voltage. $V_{dc,bus,k}$ is the required voltage on the virtual dc bus of that specific phase including voltage variations to perform balancing operations. $V_{lower,k}$ and $V_{upper,k}$ are the references sent respectively to lower and upper arms of the generic k phase. Arm references are sent to the controller which activates the modules according to the modulation technique taking into account the modules priority order generated by the module balance algorithm (II-C). Finally, the three techniques differ each other for how they turn on the components in order to achieve the voltage reference as output.

A. Nearest Level Control

The first analyzed modulation technique is based on nearest level control (NLC) [14]. It is combined with the balancing algorithm and takes into account that battery cells could be at different voltage. For this reason, in each arm, they are counted, following the order given by the balancing algorithm, until the voltage reference given by (3) is overshot. Calling n the number of selected cells, the voltage reference is compared with the voltage resulting from turning on n or $n-1$ cells and the closest to the reference is chosen. Even if the output error is always minimized both on the phase and on the virtual dc bus voltage, voltage discretization of modules causes errors in following the references. This errors have a major impact on the virtual dc bus because they might generate offsets leading to non negligible circulating currents flows between legs. Since the circulating currents are limited only by the arm inductors, this problem is particularly serious at low frequencies; to mitigate their effects suitable controllers should be introduced.

B. All Levels PWM (PDPWM)

This modulation techniques applies PWM on each discretization level of the converter. Voltage references are sent to the controller which performs similar tasks as in III-A but systematically undershoots the references. For both arms the last non activated cell (if available) is selected for PWM. Two signals are then generated following (4):

$$\begin{aligned} pwm_{lower} &= \frac{V_{ref,lower,k} - V_{lower,k}}{V_{cell,lower,k,n}}; \\ pwm_{upper} &= \frac{V_{ref,upper,k} - V_{upper,k}}{V_{cell,upper,k,n}}; \end{aligned} \tag{4}$$

where $V_{cell,lower,k,n}$ and $V_{cell,upper,k,n}$ are the voltages of the cells selected for *PWM*. $V_{ref,lower,k}$ and $V_{ref,upper,k}$ are the references sent respectively to lower and upper arms. $V_{lower,k}$ and $V_{upper,k}$ are the generated lower and upper voltages when the reference is undershot. pwm_{lower} and pwm_{upper} are then compared with a triangular carrier signal bounded between 0 and 1: if pwm is higher than the carrier, the respective module is turned on.

C. Last Level PWM (LLPWM)

The *All levels PWM* (III-B) modulation technique best approximates output voltages but also highly increases the number of commutations performed by the solid state switches. A trade off between output voltages approximation and number of commutations per period can be achieved applying *PWM*

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just on the top and the bottom levels of arm voltages. Top and bottom arms maximum and minimum references are computed using (3) substituting $V_{phase,k}$ with the maximum phase voltage that the converter is supposed to generate. Cells far from boundary references are activated following *NLC* technique. The closest cells to maximum and minimum references are then selected to generate a PWM signal produced as done in III-B. This modulation technique reduces the time window in which PWM is applied thus the overall number of commutations is reduced.

IV. Output Waveform Distortion

In this section all the described modulation techniques will be compared in terms of output voltage and current harmonic distortions for output frequencies between 1 Hz and 450 Hz. The virtual dc_{bus} voltage reference will be fixed at 180.9 V which means that the number of active modules between upper and lower arms will be always 9.

A. NLC

When the nearest level control modulation technique is implemented, depending on the selected dc bus voltage, it is possible that no output waveforms are generated below an output peak voltage reference equal to $V_{module,min}/2$ where $V_{module,min}$ is the minimum voltage of the module of the arm. A higher requested output phase voltage allows to use more of the converter levels with consequent reduction of the output THD as visible in Fig. 4 and Fig. 5 in which voltage and current THDs are reported as a function of output frequency. The peaks visible within the two plots occur when the required output voltage is such that the number of active modules is incremented by one. After each peak in voltage THD there is a decrease as effect of the changes in the turn on time instants of the modules. Triggering instants change because the output required voltage increase with frequency until 150 Hz. In general, as the output required voltage increases, voltage THD tends to decrease because the ratio between peak phase voltage and module voltage gets lowered. As this ratio is reduced, the reference waveform is better approximated. After 150 Hz the reference voltage is constant so the number of active levels remains constant and the voltage THD remains unchanged. Current THD (Fig. 5) has a similar behavior as voltage THD but it is always lower because of the filtering action of the employed inductive load. It is worth noting that both THDs are very high due to the lower number of used modules. In a converter with higher number of modules *NLC* could give better results.

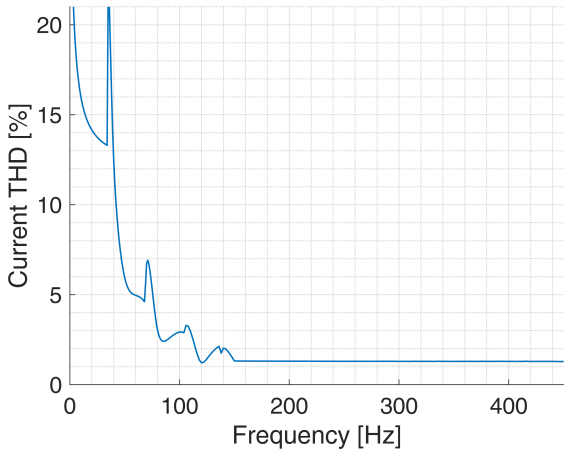

Fig. 5. Nearest level control current THD profile.

B. PDPWM

This proposed modulation technique adds PWM on each discretized output level of nearest level control. Two different maximum carrier frequencies of 15 kHz and 20 kHz have been tested. Synchronous modulation is adopted on the whole output frequency range. In Fig. 6 a detailed plot of the current THDs produced by PWM techniques is reported. As clear from the comparison of Fig. 6 with Fig. 5, both PWM carrier frequencies improve strongly the current harmonic distortion

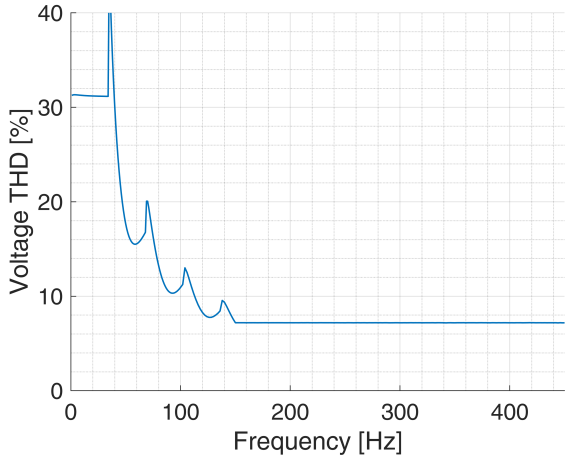

Fig. 4. Nearest level control voltage THD profile.

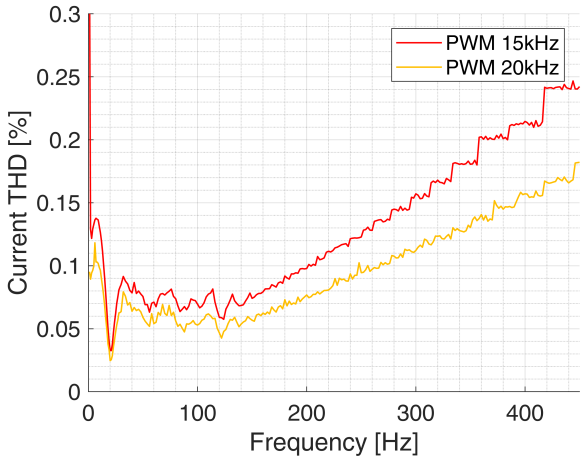

Fig. 6. Comparison between current THDs as a function of output frequency when the implemented modulation technique is PDPWM.

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on the whole frequency range.

Synchronous modulation requires to change the modulation index as the output frequency increases in order to keep constant and multiple of three the ratio between carrier and output reference frequencies; as a consequence, when the output frequency increases, the lowest carrier presents bigger current THD steps in the instants when modulation index changes. This phenomenon is visible in Fig. 7 where the plots of output current THD and of the corresponding modulation index are superimposed.

C. LLPWM

This modulation technique applies to nearest level control PWM just on the last top and bottom levels of the output voltage waveforms. The idea is to minimize the number of commutations keeping as low as possible output current THD. In this case, synchronous PWM with maximum carrier of 20 kHz has been tested. At very low frequencies (thus also very low output voltages) just one level of the converter is active so voltage and current THDs behave exactly as all levels PWM modulation technique (Fig 8 and 9). As the output voltage increases, the next level is triggered; when this happens the output current THD assumes a similar pattern to *NLC* but stays below its highest spikes: this is due to the fact that *LLPWM* corrects voltage discretization error in the most critical points of the generated waveform. From the comparison between voltage THDs (Fig. 8) of all the proposed modulation techniques it is visible that at low frequencies the lowest distortion is achieved with the *NLC* modulation technique. At high output frequencies (and voltages), PWM modulation technique voltage distortions are lower than all the others. However, this increases with the output frequency, while the one of NLC and LLPWM is constant. For this reason, for very high modulating frequencies (or very low carrier frequencies) NLC and LLPWM could behave better than PWM. Applying PWM on top and bottom levels when working at high frequencies results in a voltage distortion oscillating on the same value assumed by *NLC*.

Comparing current THDs reported in Fig. 9, it is clear that the best performance in terms of output current THD is obtained by applying PWM on all levels.

V. Converter Losses

In this section losses within the converter will be analyzed for each modulation technique reported in III. The internal losses of the converter can be divided into conduction and switching losses [15]. Conduction losses arise because switches present a non zero resistance even when in conduction state. Conduction losses also include the energy dissipated from the leg inductors due to their internal resistance assumed to be 0.65 mΩ. Switching losses exist because energy is dissipated every time a switch changes its state. The amount of energy lost for each commutation depends on the switch physical parameters and on voltage and current applied to it. Conduction losses are computed for each time step (Ts) of the simulation with (5).

$$E_{conduction} = R_{dson} \cdot I_{arm}^2 \cdot T_s. \tag{5}$$

Since in normal operation always one component of a module is conducting this equation is computed for each cell of every arm within the converter. Every time one of the modules changes its state current flows also in one of the two internal diodes thus a correction has to be done:

$$E_{diode} = -R_{dson} \cdot I_{arm}^2 \cdot (2t_{rise} + 2t_{fall} + t_{don}) + U_{d0} \cdot I_{arm} \left(\frac{t_{fall}}{2} + \frac{t_{rise}}{2} + t_{don} \right). \tag{6}$$

with t_{don} the time delay of the MOSFET. Note that ohmic losses within diode have been neglected. Total conduction losses are obtained summing together (5) and (6). Switching losses are computed for each module within the converter. Losses for diodes activation and losses inside MOSFET gate circuits have been neglected. Every time a module changes state a MOSFET is turned off and then the other one is turned

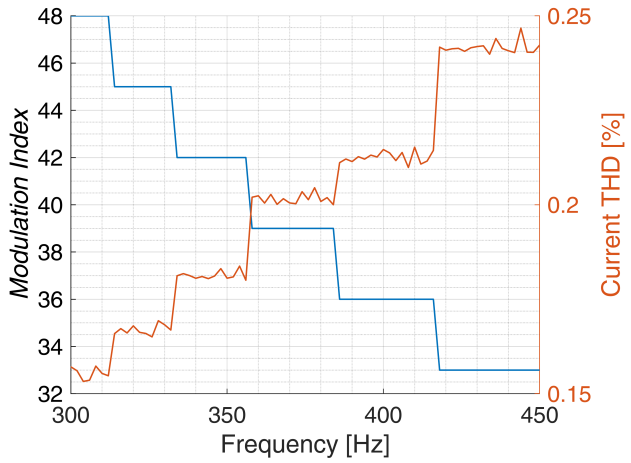

Fig. 7. NLC with 15 kHz PWM on all levels Current THD vs Modulation Index ($F_{carrier}/F_{phase}$).

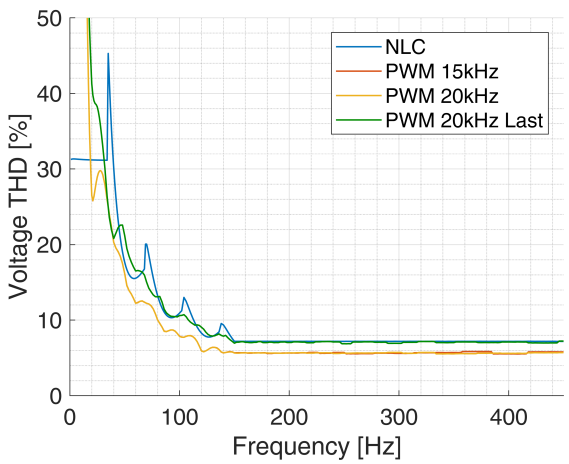

Fig. 8. Voltage THD as a function of the output frequency. Comparison between different modulation techniques.

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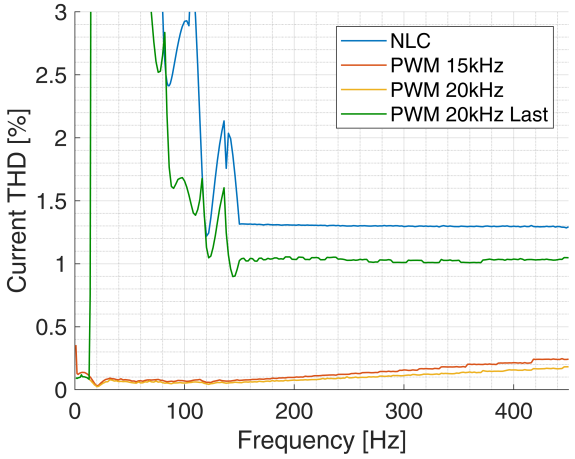

Fig. 9. Current THD as a function of the output frequency. Comparison between different modulation techniques.

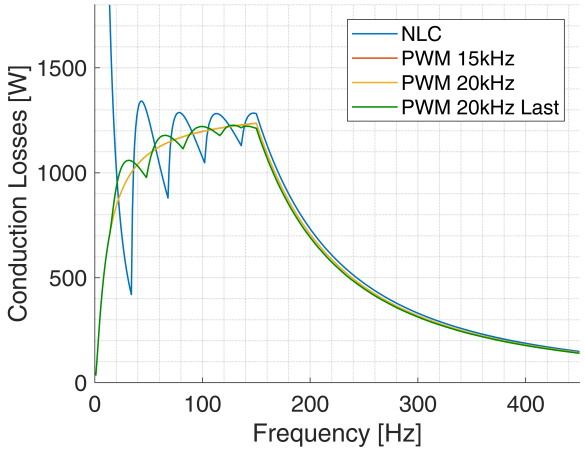

Fig. 10. Comparison of conduction losses within the converter between all the proposed modulation techniques.

on. When the second MOSFET turns on it also turns off its correspondent diode. The switching losses equation is (7).

$$E_{switching} = E_{off,M} + E_{on,M} + E_{off,D} + E_{off,D-M}. \quad (7)$$

with:

$$\begin{aligned} E_{off,M} &= E_{on,M} = V_m \cdot I_m \frac{t_{rise} + t_{fall}}{2}; \\ E_{off,D} &= \frac{1}{4} Q_{rr} \cdot V_m; \\ E_{off,D-M} &= Q_{rr} \cdot V_m; \end{aligned} \quad (8)$$

where V_m is the voltage of the module, I_m is the current flowing within it and Q_{rr} is the reverse recovery charge of the diode. $E_{off,M}$ and $E_{on,M}$ are the energies dissipated to turn off and on MOSFETS, $E_{off,D}$ is the energy lost to turn off the diode and $E_{off,D-M}$ is the additional energy loss within the MOSFET to turn off its corresponding diode.

A. Conduction Losses

In Fig. 10 the conduction losses obtained applying the three modulation techniques are reported, it is possible to see that at low frequencies *NLC* modulation technique presents high conduction losses differently from *PWM* based techniques. This is mainly because at low frequency the impedance of the load is low and the applied voltage of NLC technique overshoots the reference leading to a high current flowing within the load. In the V/Hz control region all the modulation techniques except for PDPWM presents ripples in the losses profile. At high frequency instead all the modulation techniques presents practically the same power dissipation. Fig. 11 reports conduction losses in p.u. It demonstrates that ripples in the middle frequencies of the losses profile are directly related to ripples on the delivered active power since the ratio between internal dissipated power and output active power does not show any oscillation. Ripples on output power are strictly related to modules voltage discretization: as the reference voltage increases there are some values that fall across the limit with the activation of the successive level. In some cases the output is undershooting the reference until the next level is triggered, when this happens the reference is suddenly overshot. Those variations in the output voltage approximations influence the real power delivered to the load. At very low frequency the actual power delivered to the load is quite low. Fig. 10 suggests that *NLC* modulation technique is subjected to very high internal losses at low frequencies. Those losses are produced by two different factors. The main reason is that the *NLC* is programmed to minimize the error on both the virtual dc bus and on the output phase voltage. This means that, depending on the virtual dc bus reference, the output voltage for references below $V_{module}/2$ might be systematically overshot. In this context, voltage overshot at low frequency operation highly increases load currents and increases strongly internal losses. The second phenomenon which leads to higher conduction losses is related to circulating currents which tend to rise more in *NLC* with respect to other modulation techniques when delivering power at low frequencies.

B. Switching Losses

Switching losses depend on switches technology, on the current flowing and on the voltage across them when they are interdicted. Each time a switch changes its own state some energy is lost. The relation of switching losses with the number of commutations appear clearly in Fig. 12 where switching losses are reported in p.u.: at low frequencies (and voltages) all the modulation techniques except for *NLC* shows high p.u. switching losses, this is because in all modulation techniques involving *PWM* a high number of commutations is performed even if the output power is rather low. At such low output voltage references, all modulation techniques which apply *PWM* on last levels act as PDPWM (just one level is being utilized) so their switching losses are identical to the PDPWM modulation technique with the same carrier frequency. If the carrier frequency Fc is much higher than the maximum output frequency (450 Hz) *PWM* techniques perform almost the same

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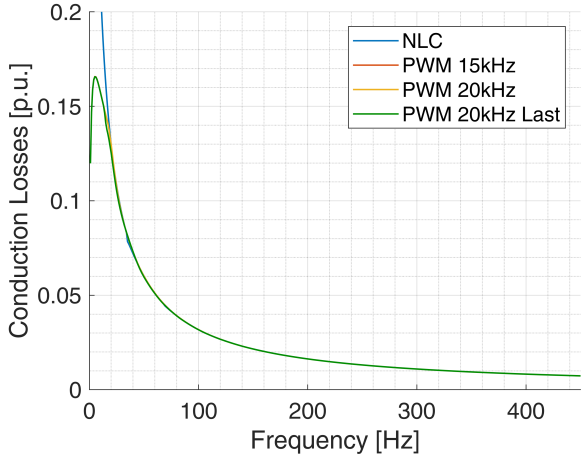

Fig. 11. Comparison of conduction losses within the converter between all the proposed modulation techniques. Results are in p.u. with respect to the active output power.

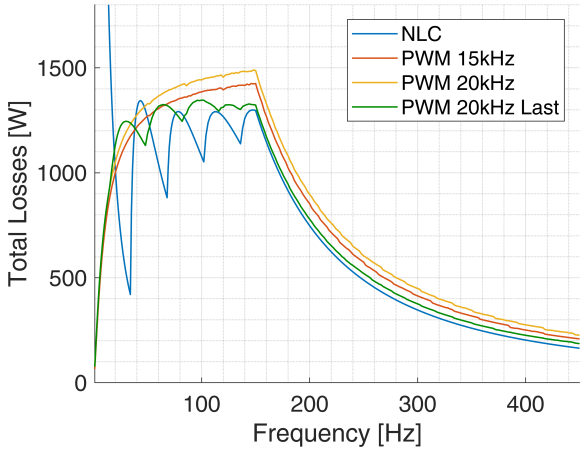

Fig. 13. Comparison of total losses within the converter between all the proposed modulation techniques. Results are expressed in W.

number of commutation across the whole frequency range. At high frequencies it is rather visible the influence of carrier frequency over switching losses: higher carrier frequencies leads to higher switching losses even when applying *PWM* on just the last levels.

NLC modulation technique presents very low switching losses at low frequency: in this modulation technique the number of commutations performed by the switches is directly related to the reference frequency. At low frequencies and voltages very few commutations per second are performed leading to low switching losses.

C. Total Losses

In this subsection both conduction and switching losses are combined together to be analyzed. In Fig. 13 total converter losses are reported for each modulation technique, in Fig. 14 the same results are expressed in p.u. Comparing Fig. 10 with Fig. 13 and Fig. 11 with Fig. 14 it is possible to appreciate the different weights of conduction losses and switching losses: the overall plots pattern is the same but an offset is introduced for modulation techniques involving *PWM*. The magnitude of the offset depends primary on carrier frequency and secondarily on reference frequency (for techniques with *PWM* on just last levels).

Since the difference of total losses between all the modulation techniques remains well below 0.01 p.u. it is possible to claim that switching losses are always much lower than conduction losses. This is mainly because of converter topology since each switch deals with relatively low voltages thus low switching losses arises. The converter structure also needs many semiconductors connected in series so the global internal resistance is rather high with consequent higher conduction losses. In Fig. 14 the internal losses reduction obtained applying NLC

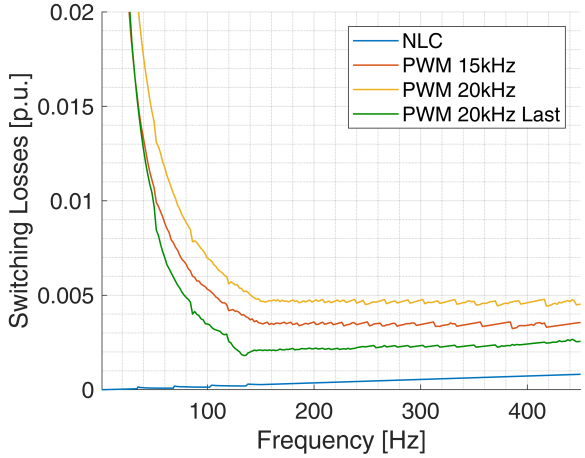

Fig. 12. Comparison of switching losses within the converter between all the proposed modulation techniques. Results are in p.u. with respect to the active output power.

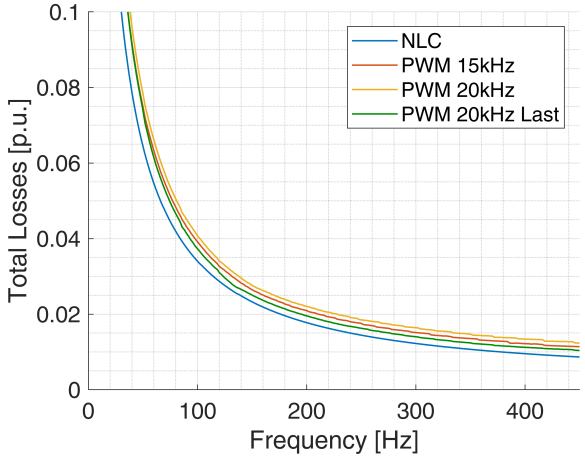

Fig. 14. Comparison of total losses within the converter between all the proposed modulation techniques. Results are in p.u. with respect to the active delivered power.

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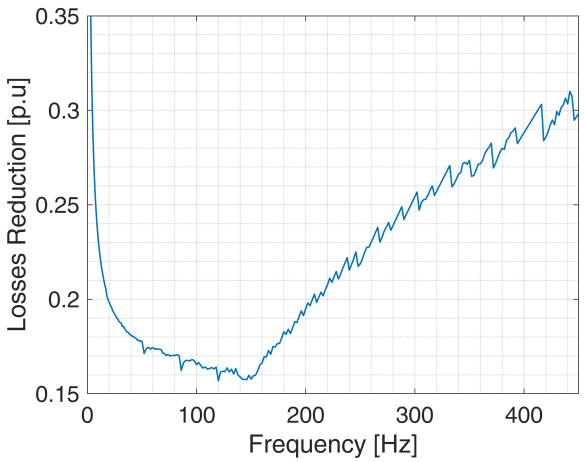

Fig. 15. Losses reduction of NLC over PDPWM modulation technique in p.u. with respect to the delivered active power.

instead of PDPWM modulation technique is computed for each output frequency. In Fig. 15 the losses reduction obtained employing NLC instead of PDPWM is shown for each output frequency. The NLC technique allows a reduction of at least 15% of the losses in comparison with PDPWM for all the output frequencies.

VI. Conclusions

In this paper three possible modulation techniques for *DSCC* were analyzed in terms of harmonic distortion and converter internal losses. The best modulation technique depends on the requirements of the load, it can be chosen to minimize output voltage and current distortion or to minimize both the losses generated within the load and the converter. If the goal is to minimize output current THD, the best modulation technique depends on the output frequency, on the output voltage and on the characteristics of the load itself. At low output voltages, *NLC* modulation technique appeared to introduce non negligible errors on the reference approximation. The reference could be radically overshot or undershot depending on the virtual dc bus voltage reference. This characteristic makes *NLC* unsuitable for the employed V/Hz control at very low voltage levels. If the goal is to minimize losses, NLC is the best solution. The proposed technique implementing PWM only on the last level permits to achieve THDs comparable with traditional PWM but with reduced losses, even if higher than NLC.

Switching between modulations techniques as function of output frequency and output voltage could optimize internal losses maintaining acceptable output current harmonic distortion. The choice of modulation technique could also be done in order to limit current harmonics within modules in order not to stress the batteries and to increase the expected lifetime of the storage system [16].

References

[1] K. Li, A. Bouscayrol, S. Han, and S. Cui, "Comparisons of electric vehicles using modular cascade machines system and classical single drive electric machine," *IEEE Transactions on Vehicular Technology*, vol. PP, no. 99, pp. 1–1, 2017.

[2] S. M. M. Sangdehi, S. Hamidifar, and N. C. Kar, "A novel bidirectional dc/ac stacked matrix converter design for electrified vehicle applications," *IEEE Transactions on Vehicular Technology*, vol. 63, no. 7, pp. 3038–3050, Sept 2014.

[3] J. Wang, X. Yuan, and K. Atallah, "Design optimization of a surface-mounted permanent-magnet motor with concentrated windings for electric vehicle applications," *IEEE Transactions on Vehicular Technology*, vol. 62, no. 3, pp. 1053–1064, March 2013.

[4] S. D'Arco, L. Piegari, and P. Tricoli, "A modular converter with embedded battery cell balancing for electric vehicles," in *2012 Electrical Systems for Aircraft, Railway and Ship Propulsion*, Oct 2012, pp. 1–6.

[5] ——, "Power and balancing control considerations on modular multilevel converters for battery electric vehicles," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, Sept 2013, pp. 1–9.

[6] S. D'Arco, L. Piegari, M. S. Quraan, and P. Tricoli, "Battery charging for electric vehicles with modular multilevel traction drives," in *7th IET International Conference on Power Electronics, Machines and Drives (PEMD 2014)*, April 2014, pp. 1–6.

[7] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 507–517, Jan 2016.

[8] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2041–2051, March 2017.

[9] S. D'Arco, M. Quraan, P. Tricoli, and L. Piegari, "Low frequency operation of modular multilevel converters with embedded battery cells for traction drives," in *2016 International Symposium on Power Electronics, Electrical Drives, Automation and Motion (SPEEDAM)*, June 2016, pp. 1375–1382.

[10] B. P. McGrath and D. G. Holmes, "Multicarrier pwm strategies for multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 858–867, Aug 2002.

[11] M. S. Rajan and R. Seyezhai, "Comparative study of multicarrier pwm techniques for a modular multilevel inverter."

[12] Y. Okazaki, W. Kawamura, M. Hagiwara, H. Akagi, T. Ishida, M. Tsukakoshi, and R. Nakamura, "Experimental comparisons between modular multilevel dscc inverters and tsbc converters for medium-voltage motor drives," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1805–1817, March 2017.

[13] *HEXFET Power MOSFET IRL40SC228*, International Rectifier, 05 2017.

[14] M. Moranchel, E. J. Bueno, F. J. Rodriguez, and I. Sanz, "Implementation of nearest level modulation for modular multilevel converter," in *2015 IEEE 6th International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2015, pp. 1–5.

[15] D. Graovac, M. Prschel, and A. Kiep, "Mosfet power losses calculation using the data-sheet parameters," Infineon Tecnologies AG, pp. 1–22, 7 2006.

[16] K. Uddin, A. D. Moore, A. Barai, and J. Marco, "The effects of high frequency current ripple on electric vehicle battery performance," *Applied Energy*, vol. 178, no. Supplement C, pp. 142 – 154, 2016. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S030626191630808X

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