3D Integration Technology: Status and Application Development

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***Abstract*—As predicted by the ITRS roadmap, semiconductor industry development dominated by shrinking transistor gate dimensions alone will not be able to overcome the performance and cost problems of future IC fabrication. Today 3D integration based on through silicon vias (TSV) is a well-accepted approach to overcome the performance bottleneck and simultaneously shrink the form factor. Several full 3D process flows have been demonstrated, however there are still no microelectronic products based on 3D TSV technologies in the market - except CMOS image sensors. 3D chip stacking of memory and logic devices without TSVs is already widely introduced in the market. Applying TSV technology for memory on logic will increase the performance of these advanced products and simultaneously shrink the form factor. In addition to the enabling of further improvement of transistor integration densities, 3D integration is a key technology for integration of heterogeneous technologies. Miniaturized MEMS/IC products represent a typical example for such heterogeneous systems demanding for smart system integration rather than extremely high transistor integration densities. The European 3D technology platform that has been established within the EC funded e-CUBES project is focusing on the requirements coming from heterogeneous systems. The selected 3D integration technologies are optimized concerning the availability of devices (packaged dies, bare dies or wafers) and the requirements of performance and form factor. There are specific technology requirements for the integration of MEMS/NEMS devices which differ from 3D integrated ICs (3D-IC). While 3D-ICs typically show a need for high interconnect densities and conductivities, TSV technologies for the integration of MEMS to ICs may result in lower electrical performance but have to fulfill other requirements, e. g. mechanical stability issues. 3D integration of multiple MEMS/IC stacks was successfully demonstrated for the fabrication of miniaturized sensor systems (e-CUBES), as for automotive, health & fitness and aeronautic applications.**

I. INTRODUCTION

Performance and productivity of microelectronics have increased continuously over more than four decades due to the enormous advances in lithography and device technology. However, today it has become questionable if the "traditional" device shrinking development alone will be able to overcome the performance and cost problems of future IC fabrication, e.g. caused by interconnect delay and latency issues. The ITRS roadmap predicts 3D integration as a key technology to solve this so-called "wiring crisis" [1]. The corresponding solution – 3D integrated circuits (3D-IC) - will most probably be based on through silicon via (TSV) technology.

World-wide several companies and research institutes have demonstrated 3D integration processes [2]. Even though there are still no commercial 3D-IC applications in the market, it has become apparent that there is a strong demand for such future applications including memories and processors.

In addition to the enabling of further improvement of transistor integration densities ("More Moore"), 3D integration is a well-accepted approach for so-called "More than Moore" applications with their essential need for integration of heterogeneous technologies.

II. APPLICATION DEVELOPMENT

Which microelectronic products based on TSV technologies are at present actually in the market? CMOS image sensors (CIS) using a "via last" approach with via diameters of about 50 µm and similar silicon thicknesses have been already introduced in the market mainly driven by form factor. Actually today´s only commercial stacked TSV applications are not 3D-IC structures, but instead use backside vias. In Europe STMicroelectronics developed a 2M pixel mobile-phone camera module VD6725 which is fabricated using TSV. The CMOS image sensor products are being fabricated in their Crolles facility [3]. Also other major CIS manufacturers, as Aptina, Samsung, Toshiba and ZyCube announced to use backside TSV processes for their future products.

A strong demand for TSV technology is predicted in numerous publications and as well by many independent

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market reports (e.g. [4]). Thus clearly, future applications include memories and processors (see Fig. 1): 3D stacking of DRAM and NAND memories by applying TSV technology is in development and has been reported to be technically viable by e. g. Samsung, Elpida and Micron. Subsequently the stacking of Flash memories is expected to be introduced. The evolution of the corresponding fabrication technologies will result in combined DRAM/Flash products with TSV diameters of < 5 µm in ultrathin silicon of less than 20 µm. Chip-on-Chip (CoC) stacking of memory and logic devices without TSVs is already widely introduced in the market. Applying TSV technology for memory on logic will increase the performance of these advanced products and simultaneously shrink the form factor. Toshiba simulated a 16-core processor to quantify the impact of 3D integration (TSV) to CMOS technology (32nm node). In 2009 Samsung published the realization of an 8Gigabit DDR3 DRAM memory by 3D stacking using TSV technology [5]. The 3D architecture with one master and three slave chips enables I/O data rates of 1600 Mb/s. Elpida Memory has prototyped as well an 8Gigabit TSV DRAM and announced to schedule the fabrication of a 16 Gigabit product.

While in summary it shows up that the benefits of 3D TSV technology are widely accepted, the real initiation of commercial 3D-IC products is not expected before 2012. Apparently the high performance needs can not be met by current 3D TSV technologies with sufficient low production costs.

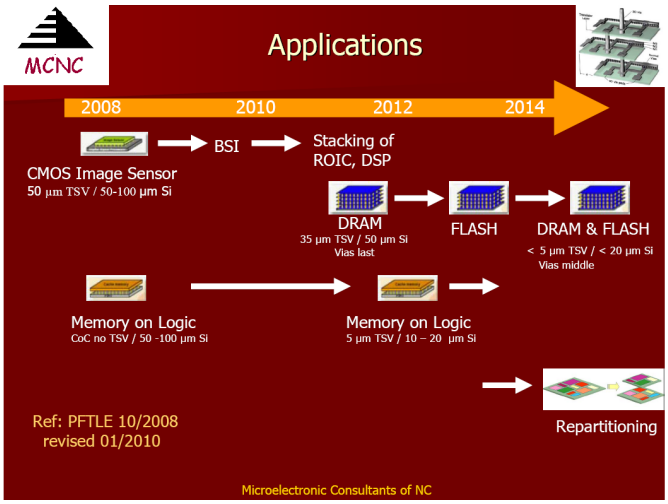

Figure 1. Roadmap of applications based on 3D integration (courtesy of Philip Garrou, MCNC, revised 2010).

The ultimate goal of 3D integration is repartitioning of ICs (right in Fig.1) and eventually a brain-like 3D architecture e.g. for processors. Clearly, both scenarios will not lead to products in the near future. Besides such high performance applications, 3D integration is recognized as a key technology for heterogeneous products, demanding for smart system integration rather than extreme high interconnect densities.

While the majority of the activities in Asia and in North America are targeting "More Moore" applications, the European industry will certainly benefit - from its strong background in microsystems technologies - of focusing on "More than Moore" products with their need of heterogeneous system integration: heterogeneous combination of components to integrate higher levels of intelligence into multifunctional microsystems including multisensing, processing, wireless and wired communication, and/or actuation capabilities. 3D integration is a very promising cost-effective approach for the realization of such heterogeneous systems.

III. STATUS OF 3D TECHNOLOGIES

3D integration is defined as fabrication of stacked and vertically interconnected device layers. The large spectrum of corresponding technologies can be reasonably classified mainly in the following main categories:

1) Stacking of packages (or substrates)
2) Stacking of embedded dies (without TSVs)
3) 3D TSV technology

According to the recently published interconnect chapter of the ITRS roadmap [1] category 1) is termed as 3D System-in-Package (3D-SIP) and 2) as 3D Wafer-Level Packaging (3D-WLP), indicating that the latter is mainly based on wafer-level processes for cost-efficient fabrication. The 3D TSV technologies can be distinguished in

a) 3D integrated circuits (3D-IC)
b) 3D system-on-chip (3D-SOC)

corresponding to basically different interconnect scenarios: 3D-ICs with sophisticated 3D architecture realized by 3D integration of transistor layers at local interconnect levels (very high TSV densities) and on the other hand 3D-SOCs where devices are stacked and interconnected at a global level with much lower TSV densities.

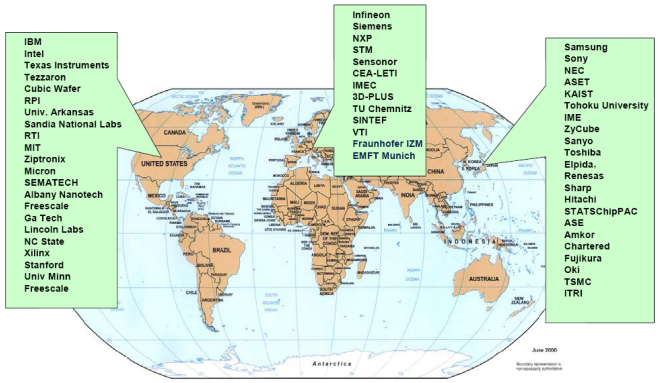

Figure 2. A sampling of global activities in 3D integration.

All over the world many companies and research organizations have demonstrated full 3D integration processes and numerous demonstration vehicles have been developed in particular for TSV technology. Fig. 2 shows a map of some of the global activity in 3D integration. An overview of the state-of-the-art on the corresponding technology developments is described in [2]. Furthermore technology suppliers as ZyCube, Intel, Samsung and IBM are currently optimizing the manufacturability and reliability of their 3D fabrication processes. One of the recent progresses is pointed out as representative for the corresponding efforts: Tezzaron´s "SuperVia" technology, initially a post backend-of-line process with Cu-Cu bonding [2] was abandoned due to failures of the used copper TSVs (ca. 5 µm diameter). In consequence they changed their process now to tungsten filled "SuperContacts" with 1.2 µm diameter [6].

What are the criteria for the technology choice? Naturally cost will always be a main criterion for large volume 3D integrated products (see Fig. 3). Besides form factor improvement, the key driver for TSV technology is performance enhancement. On the other hand, TSV technology has the potential to be less costly than the state-of-the-art for mixed technologies products – monolithically integrated planar SOCs.

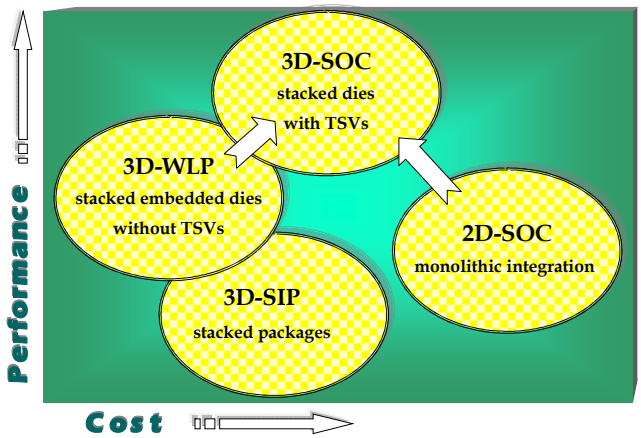

Figure 3. Qualitative comparison of different system integration technologies regarding performance and cost (as well in competition to monolithic SOCs)

The European 3D technology platform that has been established within the EC funded e-CUBES project [IST-026461] is focusing on the requirements coming from heterogeneous systems. Corresponding technologies were successfully developed in all relevant categories of 3D heterogeneous integration:

1) 3D System-on-Chip (3D-SOC)
2) 3D Wafer-Level Packaging (3D-WLP)
3) 3D System-in-Package (3D-SIP)

The 3D integration technologies which form part of the established e-CUBES platform were reported and described in detail including key characteristics, critical dimensions, electrical parameters and adaptability to new applications [7].

The main objective was to provide 3D integration technologies which on the one hand increase the performance sufficiently and at the same time allow for cost-efficient fabrication in order to achieve products with a large market potential: 3D-SOC based on bonding and vertical inter-chip wiring of stacked thinned device substrates using freely positioned (area) through silicon vias (TSVs), 3D-WLP of embedded devices by wafer-level packaging (without TSVs) and 3D-SIP of packaged devices (without TSVs). Suitable technologies in all these three main areas of interest for heterogeneous system integration were developed building the established European technology platform (see Table 1). The 3D technologies are selected and optimized concerning the availability of devices (packaged dies, bare dies or wafers) and the requirements of performance and form factor (see Fig. 4). Processes and key characteristics of these technologies are described in the following sections.

TABLE 1: The European 3D Technology Platform (e-CUBES)

Technology	**e-CUBES Partner**
3D-SOC	
Through Silicon Via (TSV) Technology (ICV-SLID)	Fraunhofer EMFT (formerly IZM-M)
Hollow Via & Gold Stud Bump Bonding (HoViGo)	SINTEF
3D-WLP	
Thin Chip Integration (TCI / UTCS)	IMEC and Fraunhofer IZM & EMFT
Via Belt Technology (Chip-in-Polymer and µInsert)	CEA-Leti
3D-SIP	
High Performance Package-in-Package Technology (HiPPiP)	3D-PLUS
Wirefree Die-on-Die Technology (WDoD)	3D-PLUS
Submicron Wire Anisotropic Conductive Film Assembly (SW-ACF)	Tyndall

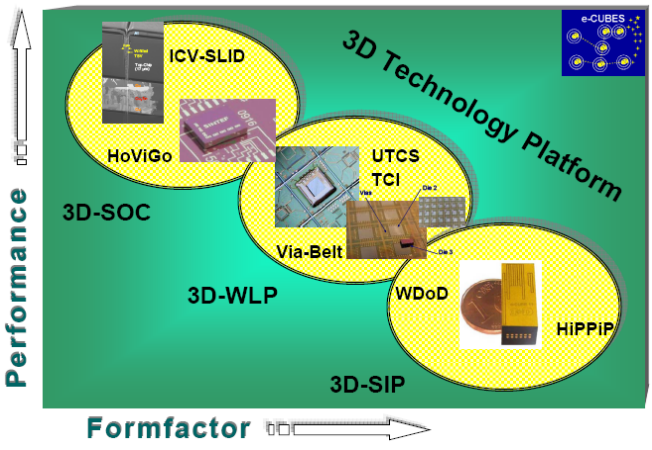

Figure 4. The European 3D Technology Platform

3D SYSTEM-ON-CHIP (3D-SOC)

Through Silicon Via Technology ICV-SLID:

The fabrication of heterogeneous products is in general based on integration of fully-processed devices which do not show identical chip areas. In consequence post backend-of-line (BEOL) processes optimized for chip-to-wafer stacking are needed. Targeting on products with high-performance and small form factor requirements, a post BEOL 3D-SOC technology based on TSVs and stacking of devices by intermetallic compound bonding (solid-liquid interdiffusion – SLID) has been developed and evaluated. The chip-to-wafer stacking process is optimized for 3D integration of known good dies. The through silicon vias are fabricated on completely processed bare device wafers. High aspect ratio TSVs through all BEOL layers and typically 10 – 50 µm deep further into the Si substrate are isolated with a highly conformal O_3/TEOS oxide and filled with tungsten or copper CVD. The thinned top chips are connected to the bottom device wafer by the SLID metal system (Cu, Cu_3Sn, Cu). The Cu/Sn metallization for the SLID interconnect is realized using through-mask electroplating. The copper and tin thicknesses are selected according to the temperature profile during bonding with respect to the topography of the devices. During bonding at temperatures < 270°C the deposited Sn is completely transformed into Cu_3Sn intermetallic compound. This ε-phase is thermodynamically stable with a melting point above 600 °C. Using appropriate film thicknesses, the tin is consumed and the solidification is completed within a few minutes, leaving only unconsumed copper on both sides. The TSVs are interconnected by Al wiring to the metallization of the top device and by the SLID metal system to the metallization of the bottom device. The vertical interconnect resistances including SLID contact are approx. 0.4 Ohm for 3 x 10 µm² vias with 60 µm depth. The minimal pitch achieved for TSVs is typically 10 µm. For chip stacking with high-resolution alignment a minimum SLID pad size of 5 x 5 µm² is required. Depending on the alignment accuracy, the pitch of the complete vertical interconnects (TSV and SLID) is 10^4 - 10^5 cm^{-2}. A pitch reduction down to 3 µm is feasible and enables interconnect densities of 10^6 cm^{-2}.

A schematic of the 3D stacking concept exemplifying the modular chip-to-wafer principle of the ICV-SLID technology is shown in Fig. 5, left and the cross section of a 3D integrated test chip with W-filled TSVs and Cu/Sn SLID bond in Fig. 5, right.

The post-BEOL TSV technology applied for 3D stacking of a state-of-the-art industrial ASIC (7-level metallization) is shown in Fig. 6. The cross section shows the status of the 3D integration before the stack formation using SLID or microbump interconnects. The TSV formation is completely finished including thinning of the die down to a thickness of about 60 µm, processing the metal redistribution and deposition of passivation layers on the bottomside. After via opening the functionality test of the TSVs can be performed. Mean values of the DC-resistance of 3.7 Ohm have been measured for this W-filled daisy chain with 8 single TSV structures connected in series. The ASIC was prepared for stacking by electro-chemical deposition (ECD) of a Cu-layer with a thickness of 5 µm (top right of Fig. 6). In this case the die was glued onto a temporary silicon handle wafer.

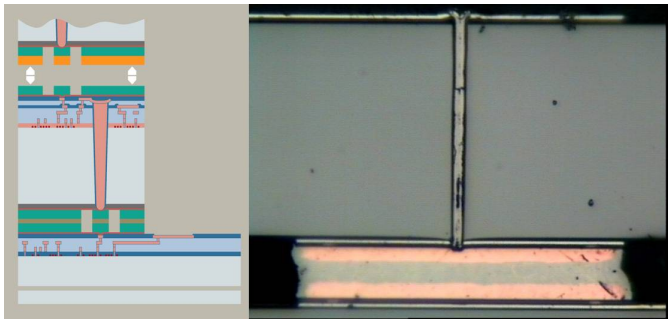

Figure 5. ICV-SLID technology
Source: Fraunhofer EMFT (formerly IZM-M)

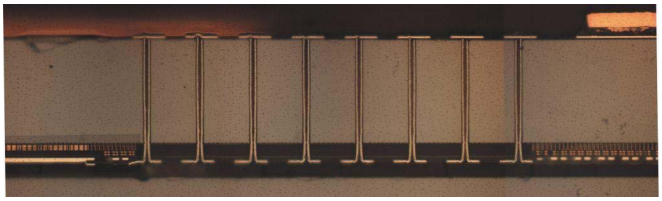

Figure 6. Post-BEOL TSV Technology
Source: Fraunhofer EMFT (formerly IZM-M)

For the application of heterogeneous system integration, in the majority of cases the components are available as fully fabricated devices only. In consequence ready-processed and thinned devices with different backend-of-line compositions (metals/dielectrics compound on thin silicon) have to be stacked. The enabling processes show up as especially sophisticated when studying the production requests (e.g. TSV formation on completely processed device wafers with complex BEOL layer structures). The basic conditions for the application of intermetallic compound bonding have to be considered carefully. Two of the critical topics are the topography of the devices to be stacked and the possibility of getting high mechanical stress built into the final 3D-IC stacks due to the TSV formation and/or the bonding process. Corresponding process optimization was required to overcome these limiting conditions. The optimized ICV-SLID technology was successfully applied for the fabrication of Infineon´s TPMS wireless sensor node [8]. The key element of the TPMS, a 3D-IC / MEMS stack, consists of a microcontroller, an RF transceiver, a bulk acoustic resonator and a pressure sensor from Sensonor and was processed in combination with SINTEF´s MEMS-specific 3D integration technology (see Fig. 7).

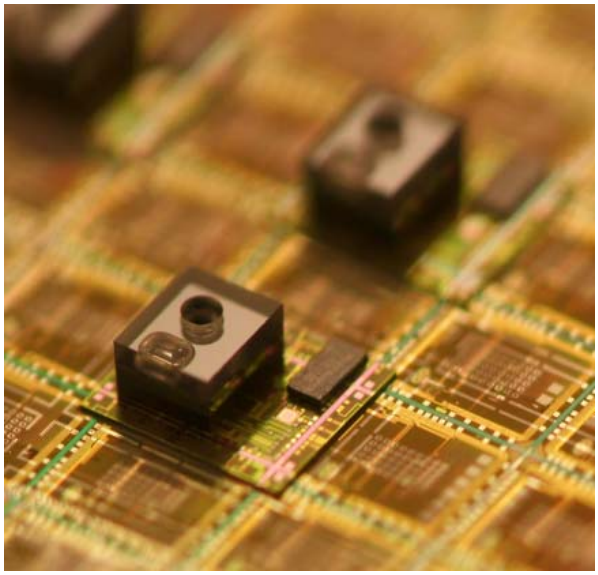

Figure 7. 3D integrated MEMS/IC systems for Infineon´s TPMS wireless sensor nodes (e-CUBES) [8]

The requirements for TSVs are different regarding 3D integration of 3D-ICs and MEMS/IC stacks, respectively. While 3D-ICs typically show a need for high interconnect densities and conductivities, TSVs for the integration of MEMS to ICs have in most cases no such need for very high performance interconnects. Rather, there is a strong requirement for very deep TSVs because the device substrates typically cannot be extremely thinned without violating the mechanical stability of the device or without breaking fragile mechanical structures. Fig. 8 shows a qualitative comparison of selected TSV processes for IC and MEMS applications, regarding achievable substrate thicknesses and pitches.

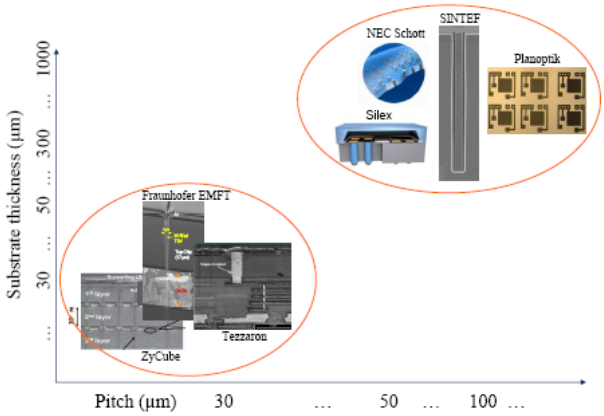

Figure 8. Qualitative comparison of selected TSV technologies for IC and MEMS applications

3D WAFER-LEVEL PACKAGING (3D-WLP)

Thin Chip Integration:

The embedding of 20 - 40µm thin dies into a BCB - copper multilayer thin film build-up on wafer level is the key technology of this 3D-WLP approach. A reliable thinning process on wafer level as well as adapted handling steps of the thinned dies are the basic requirements for the TCI technology (also called UTCS – Ultra Thin Chip Stacking). The photo-structurable BCB polymer material acts as a glue layer as well as interdielectric layer and combines the advantages of a low k dielectric material and a good planarization behavior. Electroplated Cu tracks are used for the electrical routing between embedded dies, wafer substrate and top metallization. For a successful implementation of the TCI technology the embedded chips have to be smaller than the base chip (heterogeneous integration). The TCI technology enables the shortest interconnections between embedded die and substrate chip. In addition to the realization of impedance defined interconnection lines this technology is well adapted for high frequency applications since it allows chip to substrate interconnections exhibiting extremely low parasitic capacitance and inductance together with very small bond pad pitches of future CMOS technologies. The final pad metal layer (Cu-Ni-Au) on top of the stack allows the connection to a PCB as well as mounting flip chip components or SMD components on top of the 3D stack. Fig. 9 shows a correspondingly fabricated 3D integrated chip stack.

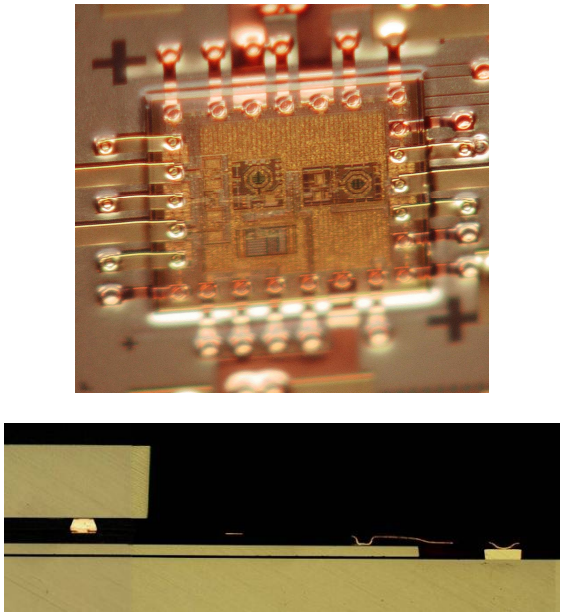

Figure 9. top: view of embedded and interconnected thin radio chip; bottom: TCI – cross section of the 3-chip-stack [7]

The thin chip integration technology was used for the realization of the 3D stack of a wireless activity monitor prototype. In cooperation between Philips Applied Research, IMEC, Fraunhofer IZM and the University of Uppsala a silicon substrate with integrated µ-Processor and a 17 GHz transmitter chip was designed [7]. The wireless sensor node consists of a 3D silicon substrate which contains the thinned active chips in a BCB-Cu multilayer stack, an antenna coupling structure that interfaces to a patch antenna on the back of the substrate and SMDs including a 3D accelerometer on top. This silicon substrate is soldered to a PCB which also carries the power management electronics, a battery and a coil for wireless charging on the backside. The linear-polarized patch antenna, glued on the backside of the 3D silicon stack is fed by a 50Ω microstrip line using aperture-coupling through an H-shaped slot in the ground plane of the 3D silicon stack. After housing, the wireless activity monitor sensor node has a size of only 20 x 11.4 x 7.4 mm³.

The active components, an MSP 430 µ-processor from TI and a 17GHz transmitter chip designed by Philips, were thinned to a thickness of 20 µm at the Fraunhofer IZM-M in Munich. These dies were glued onto a silicon substrate which already contains an electroplated ground metal layer, thin film resistors (NiCr and TaN) and Cu interconnects to the substrate. Using the above mentioned BCB-copper multilayer technology a 3D integrated system with a size of 8x18 mm² was manufactured on wafer level. The main features of this integrated 3D stack for the wireless sensor node are:

- Embedded MSP430 µ-processor and 17GHz transmitter chip (both 20µm thickness)
- 7GHz oscillator flip chip
- SMD crystal on top of embedded µ-processor
- Integrated passives: NiCr or TaN thin film resistors; Cu-BCB-Cu capacitors; a 7 GHz Balun
- Aperture-coupled antenna through an H-shaped slot
- 0201 SMDs and 3D accelerometer SMDs assembled on integrated Si substrate

The integrated 3D Si substrate after SMD assembly is shown in Fig. 10. The soldering of the integrated silicon substrate to the PCB as well as the housing of the whole sensor node was done at Philips Applied Technologies in Eindhoven. The functionality of the thinned active dies as well as the whole sensor node was successfully demonstrated.

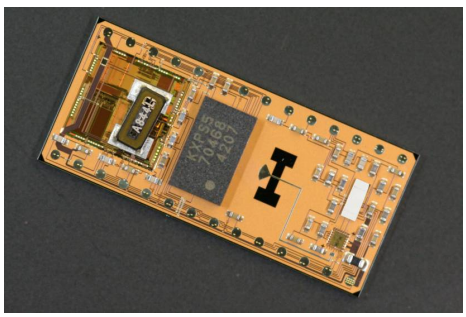

Figure 10. 3D integrated TCI substrate for wireless sensor node fabricated at Fraunhofer IZM for Philips´ Health and Fitness Demonstrator (e-CUBES) [7]

3D SYSTEM-IN-PACKAGE (3D-SIP)

High Performance Package-in-Package (HiPPiP):

The main steps of the HiPPiP process are the placement of plastic packages on an adhesive foil, then the overmoulding with epoxy resin. After the curing of the resin a thinning of active and back-side is performed permitting to reduce the thickness from 1.2 mm to 0.4mm. Then, redistribution layers are processed in order to build a fan-out from the sections of the gold wires of the packages and finally different levels are stacked and vertical interconnection is performed according standard 3D-PLUS patented process.

The advantages of this technology are the possibility of integration of almost any plastic components or passive ceramic components or bare dies of different dimensions and technologies and also integration of components which have been fully tested and burn-in. Test of each Known Good rebuilt Wafer (KGRW) is performed before stacking permitting to reach a good final yield. The manufacturing is adapted to low volume and low cost thanks to simple manufacturing steps.

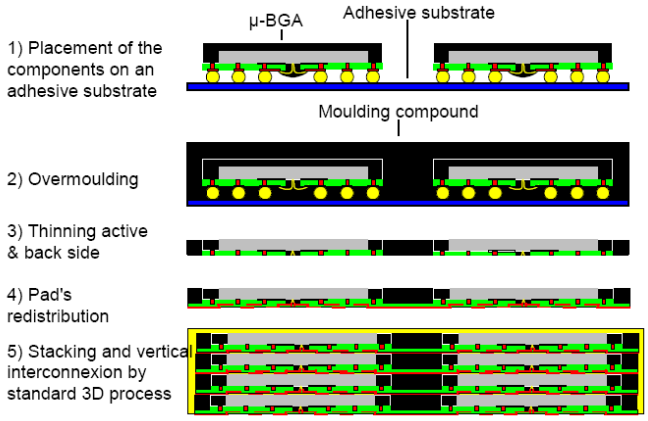

Figure 11. Description of the main process steps of HiPPiP technology [7]

The HiPPiP technology of 3D-PLUS was applied for the manufacturing of Thales aeronautical e-CUBES demonstrator where the availability of bare dies was limited. A corresponding module of the safety and security monitoring system for aeroplanes is shown in Fig. 12. The use of the HiPPiP technology resulted in a total thickness of 3 mm.

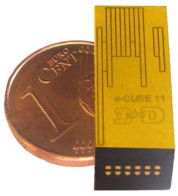

Figure 12. 3D-integrated MEMS/IC system fabricated at 3D-PLUS for Thales´aeromautical demonstrator (e-CUBES) [7]

IV. 3D INTEGRATION OF MEMS

Initially deep reactive ion etching (DRIE) of silicon was developed for micromachining of micro-electromechanical systems (MEMS), but today it has become an essential process step required for realizing TSVs, whether it is in ICs or in MEMS. The fact that the electrical components of MEMS usually are encapsulated into a sealed cavity naturally leads to an interest in TSV solutions. As opposed to IC manufacturers, MEMS manufacturers are used to implement custom process solutions for different type of devices. This is one of the reasons why MEMS will be amongst the first applications that bring 3D technology into volume production. Miniaturization demands for microsystems are the main driving force behind the interest in 3D stacking of MEMS and IC, as most MEMS devices are dependent on a control or readout IC.

TSV FOR MEMS

Glass wafer suppliers like PlanOptik [10] and NEC Schott [11] now offer glass substrates with hermetically sealed TSVs, which can be used for encapsulating MEMS devices. However in some cases a silicon cap wafer will be preferred or it will be preferable to have the TSVs in the silicon device wafer. Due to restrictions on wafer thinning for bulk MEMS devices, TSVs for MEMS will typically have very high aspect ratios, even if the TSV pitch is significantly larger than for thinned ICs. In most cases TSVs for MEMS are realized using a via-first approach, meaning that the vias are etched and filled prior to fabricating the actual devices. This allows the use of high temperature process steps which are capable of filling the high aspect ratio vias. Typically thermal oxide or TEOS provides the isolation for the TSVs and doped polysilicon is used as the conductor material. Alternatively, the silicon bulk material itself can be used as a TSV by isolating a silicon area with a surrounding oxide filled trench [12].

At SINTEF TSV technology for MEMS devices is being developed based on silicon DRIE of high aspect ratio vias, thermal oxide and polysilicon doped by phosphorus deposition. Depending on the required pitch and hermeticity, the TSVs can be either hollow (open) or filled. Hollow vias in 300 µm thick silicon wafers were successfully demonstrated in the European project e-CUBES [13]. In the ENIAC JU project JEMSiP-3D, filled polysilicon TSVs with high aspect ratio and low resistance are being developed. In an initial experiment, filled TSVs were successfully fabricated in 300 µm thick bulk silicon wafers. TSVs that could have a minimum pitch of 50 µm had a resistance of 3.2 Ω/via, whereas the resistance was only 1.2 Ω/via for a minimum pitch of 75 µm (Table 2). In many cases, silicon-on-insulator (SOI) wafers are used as device wafers for MEMS. Therefore, further work planned within JEMSiP-3D includes the demonstration of filled polysilicon TSVs through SOI wafers. DRIE of TSV structures through SOI wafers with 20 µm device layer, 0.5 µm buried oxide (BOX) and 350 µm handle wafer thickness was already developed successfully (Fig. 13).

TABLE 2: Electrical results for filled polysilicon TSVs fabricated through 300 µm bulk silicon wafers. Source : SINTEF

Via name	Minimum pitch	TSV resistance	Std dev
U3_7	50 µm	3,2 Ω	0,3 Ω
U5_7	65 µm	1,8 Ω	0,2 Ω
U7_7	75 µm	1,2 Ω	0,1 Ω

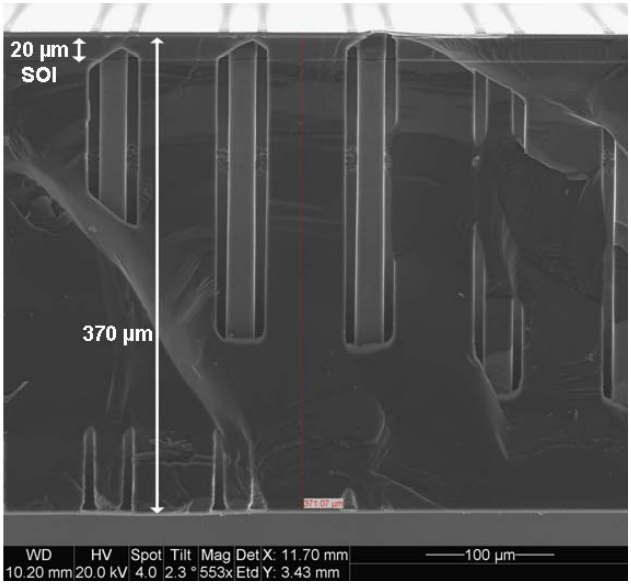

Figure 13. SEM cross-section of DRIE etched TSV structures through an SOI wafer with 20 µm device layer, 0.5 µm BOX and 350 µm handle wafer. Source : SINTEF

3D STACKING OF MEMS AND IC

In most cases the solutions being proposed for 3D stacking of ICs are based on solder bumps. The bonding can be done either chip-to-wafer or wafer-to-wafer.

In the e-CUBES project SINTEF demonstrated chip-to-wafer bonding of two different MEMS devices that were placed side by side onto a 3D stack consisting of two ASICs [13]. This was done using gold stud bump bonding (SBB). In JEMSiP-3D, SINTEF is developing a low-temperature wafer-level bonding method based on benzocyclobutene (BCB) containing gold coated polymer spheres, which forms an anisotropic conductive adhesive. Initial results are very promising. As opposed to bonding methods based on solder bumps, the use of SBB or BCB with metal coated polymer spheres does not involve wet processing steps like electroplating or wet etching, which could be problematic for e.g. MEMS devices with inlets. The stud bumps or BCB layer only need to be applied on one of the surfaces to be bonded, which could be the MEMS side without inlet or the IC. Both bonding methods also have the additional advantage of not requiring any photolithography steps or under bump metallization.

V. CONCLUSIONS

3D integration technology is today well positioned to become a paradigm shift for semiconductor industry. However there are still no microelectronic products based on 3D TSV technologies in the market – except CMOS image sensors. All over the world many companies and research organizations have demonstrated full 3D integration processes. A large percentage of the process flows that are demonstrated early on in a technological evolution are feasible but often not commercially viable. Besides the performance requirements, mainly the manufacturability and reliability of 3D fabrication processes are the basic requirements and will determine the choice of the technology. The benefits of 3D TSV technology are widely accepted but the real initiation of commercial 3D-IC products is not expected before 2012. Apparently the high performance needs can not be met by current 3D TSV technologies with sufficient low production costs and the ultimate goal of 3D integration – repartitioning of ICs – will become a reality only in a more distant future.

Besides such high performance applications ("More Moore"), 3D integration is recognized as a key technology for heterogeneous products, demanding for smart system integration rather than extreme high interconnect densities. The European industry, with its strong background in microsystems technologies, would certainly benefit of focusing on "More than Moore" products with their need of heterogeneous system integration. The fabrication of such heterogeneous products has to deal with the following basic challenging conditions: the components to be integrated are in general fully-processed devices, they do not show identical chip areas and they are not necessarily fabricated with very high wafer yield. In consequence post backend-of-line 3D integration technologies optimized for chip-to-wafer stacking of known-good-dies are needed. The requirements for TSVs are different regarding 3D integration of 3D-ICs and MEMS/IC stacks, respectively. While 3D-ICs typically need high vertical interconnect densities and conductivities, 3D integration of MEMS to ICs has a strong requirement for formation of very deep TSVs.

The European 3D technology platform that has been established within the European e-CUBES project is focusing on the requirements coming from heterogeneous systems. 3D integration technologies in three main categories – 3D-SOC, 3D-WLP and 3D-SIP – have been developed and optimized concerning the availability of devices and the performance and form factor requirements of miniaturized micro/nano-systems. Based on this comprehensive 3D technology platform further developments are focusing on the robustness of the fabrication processes and especially on reliability issues of advanced 3D integrated heterogeneous systems for future applications.

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