3D Interconnect Technologies for Advanced MEMS/NEMS Applications

Nicolas Lietaer[a], Maaike M.V. Taklo[a], Kari Schjølberg-Henriksen[a], and Peter Ramm[b]

[a] SINTEF, Department for Microsystems and Nanotechnology, Oslo, Norway
[b] Fraunhofer Institute for Reliability and Microintegration, Munich, Germany

3D integration and wafer level packaging (WLP) with through-silicon vias offer benefits like reduced footprint and improved performance. CMOS imaging sensors is one of the first successful introductions of a product with TSVs on the market, and 3D integrated memory stacks are expected to follow soon. Also sensor and actuator systems based on micro- and nano-electromechanical systems (MEMS/NEMS) will greatly benefit from WLP and 3D integration of the transducers and their readout and controller ICs. Ultimately, heterogeneous integration of different device technologies will allow the fabrication of MEMS/IC and NEMS/IC products with new and improved functionalities. For this to become a reality, cost-effective and reliable 3D integration technologies need to be developed. This paper gives an overview and reports on the current status of 3D interconnect technologies that will enable 3D integration for advanced MEMS/NEMS applications.

Introduction

In the multi-chip module technology that became available in the early 1990s, several ICs are mounted side by side into a single ceramic package. Next, came the so-called System in a Package (SiP) technology in which ICs are stacked vertically, which reduces the footprint of a package dramatically. However, in a SiP system, there is no direct electrical interconnection between the different ICs. Instead, wire bonding is typically used to connect every IC individually to a common substrate. In recent years, a new technology referred to as 3D integration has been emerging, in which ICs are stacked vertically with direct electrical interconnects between each IC. The two key process technologies required for 3D integration are the fabrication of through silicon/substrate vias (TSVs) and chip-to-wafer or wafer-to-wafer bonding. The bonding provides a mechanical as well as an electrical interconnect between the different chips in the IC stack, while the TSVs provide the electrical interconnects through the chips themselves. Provided that potential yield and reliability issues are addressed, 3D integration offers the benefits of device miniaturization, improved performance, and reduced costs.

Another key advantage of 3D integration is the potential for increased functionality. The progress of advanced smart systems relies on the ability to tightly integrate different types of technologies and devices. While Moore's law is all about scaling of traditional ICs and memory chips, functional diversification also called "*More than Moore*" requires the integration of ICs with different types of semiconductor devices like passives, sensors, actuators, bio and fluidic chips (Figure 1). Such heterogeneous 3D integration will start a whole new area for micro- and nanoelectronics with a tremendous potential for new applications. One of the key market drivers for 3D integration of MEMS devices with ICs

is portable consumer electronics. Today's cell phones, PDAs and game controllers have functionality based on MEMS devices. MEMS based 3-axis accelerometers are for instance used as motion sensors for the newest game controllers (e.g. Nintendo Wii) or for drop detection in laptops and PDAs. Cell phones also offer increasing functionality based on MEMS devices, like silicon microphones, accelerometers, micro autofocus and zoom, etc. Since MEMS devices usually depend on a separate controller or readout IC, 3D integration of MEMS and IC becomes a very desirable technology. Essential requirements for portable consumer electronics are small size, low power and low cost, all of which are potential key advantages of 3D integration. The application of nanotechnology to MEMS sensors will also allow further improvements in functionality and performance of ambient intelligence systems aimed at multiple product areas as medical, automotive and aeronautic. Such heterogeneous NEMS/IC products will also greatly benefit from cost-effective and reliable 3D integration technologies.

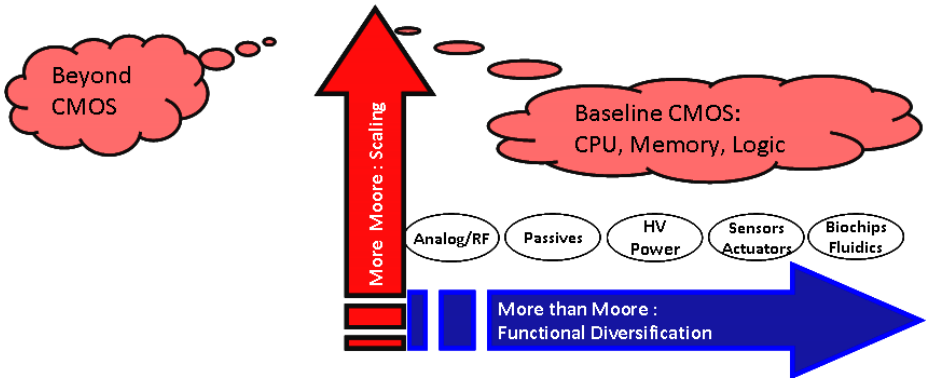

Figure 1. Moore's law scaling alone cannot maintain the progress of smart systems. Functional diversification ("*More than Moore*") requires heterogeneous integration of different types of semiconductor devices.

Technologies

Specific challenges for MEMS/NEMS

Whereas there is a certain consensus about the main approach for fabrication of 3D integrated IC or memory stacks, this is much less the case when it comes to the integration of MEMS/NEMS devices with ICs. There are a number of specific challenges to be addressed when developing 3D technologies for MEMS and NEMS devices. MEMS structures rely on a certain mass, volume or thickness for their strength, stability and reliability. As a consequence, silicon substrates for MEMS devices can normally not be thinned to 50 µm or less, as is done for realizing TSVs in ICs. With a typical substrate thickness of 300 µm or more, specific solutions need to be found for realizing the TSVs and a trade-off needs to be made between substrate thickness and minimum pitch. Many MEMS devices are fabricated on silicon-on-insulator (SOI) substrates, which also complicates the fabrication of TSVs. Anodic bonding of glass to silicon substrates is commonly used for hermetic sealing of MEMS devices. For realizing TSVs in glass wafers completely new solutions are needed, some of which are already commercially available. Depending on the application, TSVs will be needed through the silicon device wafer, or through the MEMS cap wafer which can be either silicon or glass. In the latter case, an interconnect solution is also needed to connect the TSVs in the cap wafer to the

devices on the device wafer. The presence of inlets or released structures in MEMS make the use of wet processing steps problematic, and the high topography and fragility of the structures is also a challenge. The presence of organic coatings, functional materials and nano-materials impose significant temperature limitations for the 3D integration.

TSVs for MEMS/NEMS

Fabrication of vertical TSVs in silicon substrates relies on deep reactive ion etching (DRIE) of holes, followed by the filling of the holes with an isolator and a conductive material. Although holes with very high aspect ratios can be etched by DRIE, there is a trade-off to be made between the minimum size of the holes and their depth. Typically, ICs have many I/Os and therefore require TSVs with very fine pitch. This is made possible by thinning the silicon substrates to 50 μm or less, which reduces the aspect ratio for the DRIE process. Since MEMS devices cannot be thinned, the minimum achievable pitch is necessarily larger than what can be realized for ICs. However, as MEMS devices normally only have a limited number of I/Os, they usually do not need a pitch as fine as what is required for ICs.

Hymite. The HyCap® technology of Hymite is an early example of the fabrication of TSVs through SOI wafers (1). Wet anisotropic etching (KOH) is used to etch a large cavity in the backside of the wafer, down to the buried oxide (BOX) layer. Then another short anisotropic wet etching is done from the front side. After etching the BOX oxide, small via holes exist and TSVs can be made there. A thermal oxide is grown to isolate the vias and finally the vias are hermetically sealed by electroplating Au. The slope created by the wet anisotropic etching allows the use of 3D lithography techniques to pattern the Au layer on both sides of the wafer. The HyCap® technology is particularly suitable for making TSVs through cap wafers for MEMS, but the use of wet anisotropic etching as opposed to DRIE results in a larger footprint.

Silex. Based on their "Through Silicon Insulator" technology, Silex offers vertical TSVs with a sub-50 μm pitch, in silicon wafers with a thickness from 300 to 600 μm (2). As opposed to etching a hole that is subsequently filled with a conductive material, their approach is to etch an isolation trench that forms a closed loop in a low-resistivity silicon wafer. The trench is subsequently filled with silicon dioxide, thereby isolating a silicon plug. The TSVs can be realized prior to any other processing on the wafer since the vias can withstand high-temperature post-processing, even at very high temperatures. This technology can be used to fabricate TSVs in a MEMS device wafer as well as in silicon cap wafers. A drawback of using the silicon bulk material as the conductor for the TSV is that low-resistivity wafers need to be used in order to obtain a reasonable resistance, which could be a problem e.g. for RF MEMS. However, the development of a metal via process has been announced.

SINTEF. Hollow and filled polysilicon TSVs for MEMS and interposers are being demonstrated by SINTEF. DRIE is used to etch vertical holes with different shapes and dimensions through 300 μm silicon wafers, followed by thermal oxidation, low pressure chemical vapor deposition of polysilicon and gas phase phosphorus doping of the polysilicon (3,4). Depending on the size of the holes and the amount of polysilicon that is deposited, either only the sidewalls of the holes are being covered with polysilicon ("hollow vias") or the holes are completely filled. Whereas conventional resist spinning

can be used to pattern the filled via holes, the hollow vias are being patterned using a dry-film laminated photoresist. The minimum pitch that can be achieved is of the order of 50 µm for the filled TSVs and 100 µm for the hollow TSVs. Since the vias only consist of silicon, silicon oxide and polysilicon, they can withstand high temperature post processing. The development of polysilicon TSVs in SOI wafers is ongoing, as is the demonstration of hollow vias in silicon wafers with a thickness of up to 1000 µm. Figure 2 shows the pitch versus substrate thickness for the TSV technology platform that is being established at SINTEF.

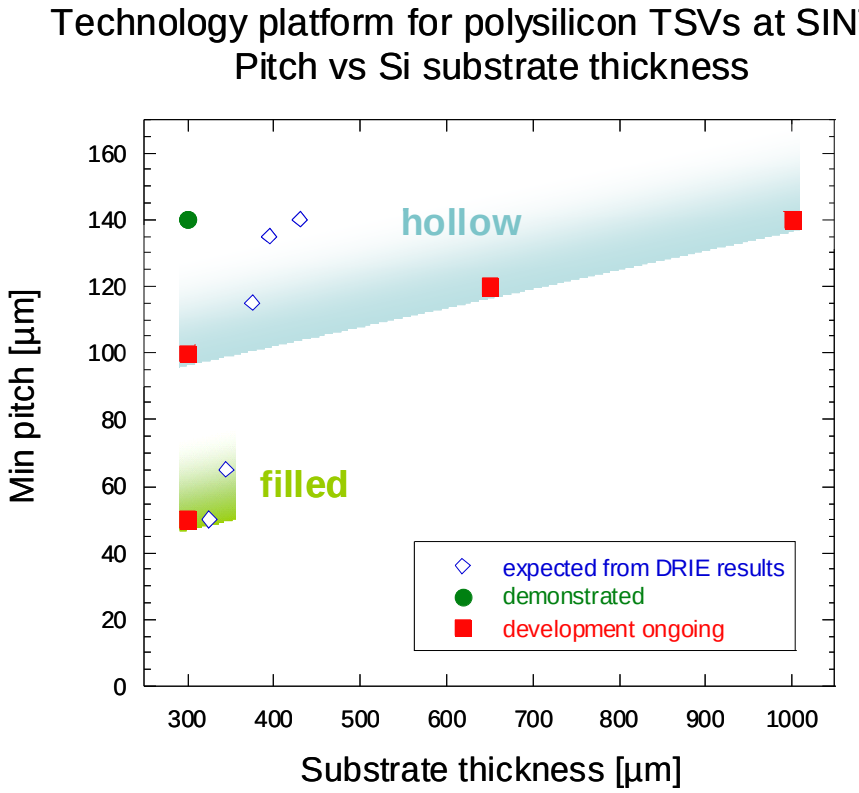

Figure 2. SINTEF technology platform for filled and hollow polysilicon TSVs in bulk silicon wafers and SOI wafers.

Planoptik. A completely different approach is being proposed by Planoptik, which is a market leader for the production of glass wafers. In addition to the conventional glass wafers, Planoptik also offers silicon-glass compound wafers, which consist partly of glass areas and partly of silicon areas (5). Their patented technology allows to freely decide where there should be glass and where there should be silicon. A silicon area surrounded by glass can serve as a hermetically sealed TSV through the wafer. The wafer can either consist mostly of glass, which allows to bond it anodically to the MEMS device wafer, or alternatively, it can exist mostly of silicon, with only isolating glass rings to define the TSVs. As is the case for the technology proposed by Silex, low-resistivity silicon wafers need to be used in order to obtain a low enough via resistance. An advantage of having glass wafers with TSVs as the MEMS cap wafer is that the transparent glass allows visual inspection of the MEMS structures even after the devices have been sealed.

NEC Schott. Through their HermeS™ technology, NEC Schott also offers glass wafers with hermetic TSVs, but their vias are filled with tungsten, which gives a much lower resistance (6). The tungsten as well as the borosilicate glass that is used has a coefficient of thermal expansion that is relatively close to that of silicon, which helps to ensure a good reliability. The vias have a fixed diameter, and a minimum via pitch of 300 µm has been reported for 500 to 600 µm thick wafers. A process for making vias with 200 µm pitch is under development.

Bonding of MEMS/NEMS and IC

The bonding method used for stacking devices with TSVs needs to provide a mechanical as well as an electrical interconnect. Many selection criteria can be used to choose the bonding technology, such as required minimum pitch, alignment accuracy, number of I/Os, stand-off height, hermeticity, reliability and cost.

It is important to make the right choice between chip-to-wafer bonding and wafer-to-wafer bonding. Wafer-to-wafer bonding allows a better alignment accuracy and smaller pitch. It also has the potential of being more cost-effective than chip-to-wafer bonding, although this will probably only be true when stacking devices with high yield and similar footprint. Whereas wafer-to-wafer bonding might be the preferred approach for making stacks of multiple ICs or memory chips, this will most often not be the case for stacking MEMS and IC. Indeed, the die sizes of the MEMS and the IC will most often differ, and MEMS devices often have a significantly lower yield than ICs. The difference in die size is not a problem for chip-to-wafer bonding, and all dice can be tested prior to bonding, such that only stacks of known good dice are formed. Also, today most MEMS devices are fabricated on smaller wafer sizes than the ICs, thereby making it impossible to use wafer-to-wafer bonding.

Many different technologies can be considered for realizing the electrical and mechanical interconnect between MEMS and IC. TABLE 1 gives an overview of possible technologies with an estimated value for the minimum pitch and minimum stand-off height that they can achieve. Some of these technologies are well established whereas others are still under development.

In order to fit a 3D stack in a standard package with a height of 1.4 or 1.2 mm, a bonding technology with low stand-off height is desired. This is particularly the case for 3D integration of MEMS and IC, where the MEMS device itself typically has a thickness of 0.8 to 1 mm. Because of their relatively large minimum stand-off height and pitch, conventional solder balls and jetted microbumps will not be discussed in this paper.

TABLE 1. Estimated minimum pitch and stand-off height for different bump/bonding technologies. Stand-off height is defined as the distance between the metal pads of the stacked devices.

Technology	Minimum pitch	Minimum stand-off height
Conventional solder balls (solder paste screen printing)	150 µm	80 µm
Jetted microbumps	80 µm	60 µm
Au stud bumps	70 µm	10 µm
Plated solder bumps	25 µm	25 µm
CuSn SLID	10 µm	10 µm
Anisotropic conductive adhesive	40 µm	3 µm
Metal thermocompression	25 µm	0 µm

Au stud bumps. A very promising bonding technology for MEMS devices is Au stud bump bonding (7). The stud bumps can be placed directly on the metal bond pads, without the need for any extra passivation or under bump metallization layers. This means that there is no need for any wet processing that could otherwise be problematic for MEMS devices with inlets and released structures. As the placement of the bumps is a serial process, this technology will be most cost-effective for devices with a relatively low number of I/Os, which is the case for most MEMS devices. The minimum pitch that can be achieved for Au stud bumps is estimated at 70 µm, with a minimum stand-off height of about 10 µm. The use of chip-to-wafer Au stud bump bonding for 3D integration of MEMS and IC was demonstrated successfully within the e-CUBES project (3).

Plated solder microbumps. Also demonstrated within the e-CUBES project was the successful use of SnAg plated microbumps (8) for chip-to-wafer bonding of two ICs. The same technology could also be used to stack a MEMS and an IC, although the inlets and released structures might need protection during some of the process steps like the electroplating. This could for instance be done by using a laminated dry-film photoresist. It is estimated that the minimum pitch achievable with plated solder microbumps is of the order of 25 µm, as is the minimum stand-off height (9). Extensive tests done for SnAg microbumps revealed an excellent reliability of this bonding technology (10).

Solid-Liquid Interdiffusion (SLID). Another very promising technology that might be used for bonding of MEMS and IC is Cu/Sn SLID (11,12). During the soldering step at 325 ºC, a Cu_3Sn phase is formed, which is thermodynamically stable up to its melting point which is as high as 670 ºC. This interesting property allows many layers to be bonded on top of each other without degradation of the previous bonds. It is estimated that SLID technology can be used for chip-to-wafer bonding with a minimum pitch and minimum stand-off height of about 10 µm. The achievable pitch is only limited by the alignment accuracy.

Anisotropic conductive adhesive (ACA). A very different approach being investigated for bonding of MEMS and IC is the use of ACA (13,14), which today is mainly used in the flat panel display industry. ACA is a film-like adhesive containing conductive metal spheres or metal coated polymer spheres. The interconnect is formed by trapping the conductive particles between two corresponding conductive pads. The stand-off height is extremely small since it is determined by the diameter of the metal spheres, which is typically 3 to 5 µm. The minimum pitch for ACA is estimated to be about 40 µm. Compared to many other technologies, ACA might be a very simple and low cost bonding solution. Only 150 to 200 ºC is required to cure the ACA, which makes it a low-temperature bonding method compatible with CMOS devices. A further evolution of this technology is to embed nanowires in a polymer or dielectric film (15), which should allow a significant reduction of the minimum pitch.

Metal thermocompression. Thermocompression bonding of metals like Cu, Au and Al can be done at temperatures of 350 to 400 ºC (16), which is just within the temperature limit for post-processing of CMOS ICs. Given a certain temperature, pressure and time, recrystallization of the metal areas will occur, thereby creating a strong bond. Tezzaron for instance uses Cu-Cu thermocompression for 3D integration of ICs and memory chips (17). For their chip-to-wafer bonding a minimum pitch of 25 µm has been published.

Also for bonding of MEMS and IC thermocompression might be suitable. For this bonding method the metal pads of the devices are pressed directly against each other without the need for any intermediate bumps or layers. This means that the height of the stack is minimized.

Technology Demonstrators

e-CUBES miniaturized Tire Pressure Monitoring System (TPMS). One of the demonstrators that was fabricated as part of the European project e-CUBES (18) was a 3D integrated TPMS (4,19,20). It was composed from two ASICs and two MEMS devices (Figure 3). Tungsten-filled TSVs were made through one of the ASICs, which was thinned down to 60 µm. The thinned ASIC was then bonded, chip-to-wafer, to the other ASIC using SnAg microbumps and underfiller. Both MEMS devices were subsequently bonded on top of the double ASIC stack using Au stud bump bonding. One of the MEMS devices was a pressure sensor consisting of a glass-silicon-glass stack. In order to lead the electrical signal from the silicon device wafer in the middle of the stack to the surface of the glass cap wafer, glass wafers with Si TSVs from Planoptik were used.

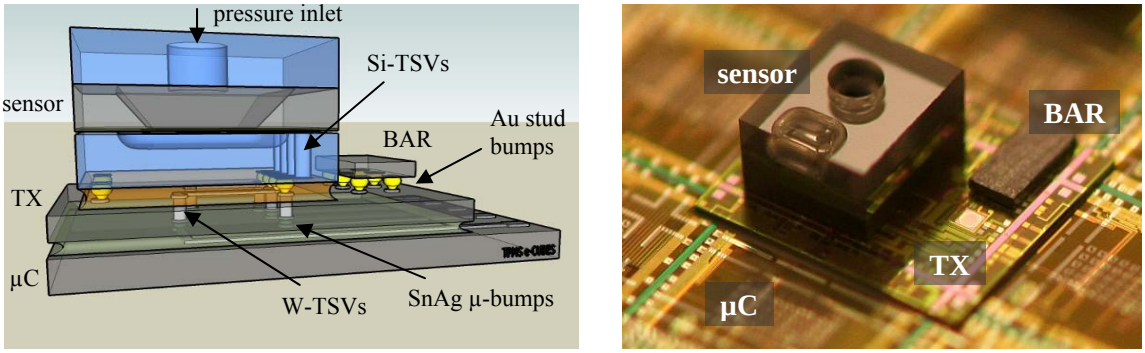

Figure 3. Illustration of the e-CUBES 3D integrated TPMS demonstrator (left) and image of the actual demonstrator before final dicing (right). The pressure sensor and bulk-acoustic resonator (BAR) are both MEMS devices whereas the transceiver (TX) and micro-controller (µC) are ASICs.

European project DAVID. Another European project that looked into 3D integration of MEMS and IC is DAVID (21). In this project, the proposed concept is that the thinned ASIC with TSVs also serves as a cap wafer for the surface micromachined MEMS (22), thereby significantly reducing the total stack height (Figure 4). A potential problem that was addressed is the outgassing from the CMOS IC which could degrade the long-term vacuum level. This was solved by integrating a getter film in the MEMS cavity. Au-Sn bonding is used for the mechanical, hermetic and electrical joining of both devices. Both chip-to-wafer and wafer-to-wafer approaches were investigated. For the chip-to-wafer approach, singulated MEMS dice were bonded onto a full ASIC wafer.

VTI technologies Chip-on-MEMS. In the Chip-on-MEMS technology from VTI (23) a thinned ASIC die is flip-chipped to a MEMS wafer, using small solder bumps. Only known good ASICs are mounted onto known good MEMS devices. For the final mounting of the stack, large solder balls with a size of several hundreds of micrometer are placed on the MEMS die, next to the thinned ASIC. With this concept, no TSVs are required through the ASIC, but TSVs are needed through the MEMS cap wafer. The total

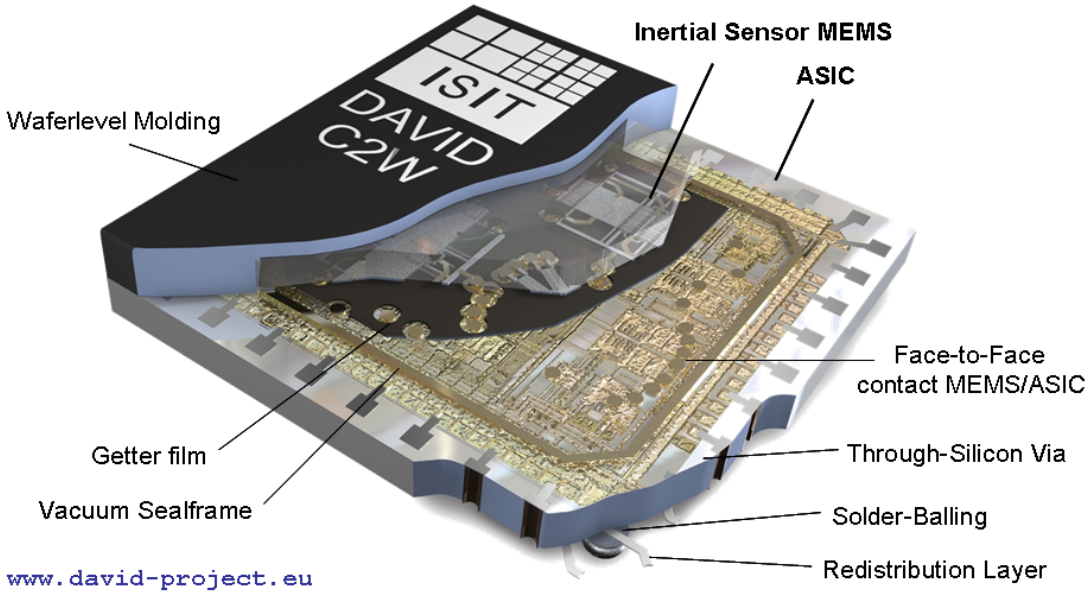

Figure 4. Illustration from the European project DAVID, showing a 3D integrated MEMS die and CMOS IC with TSVs and getter film.

height of the MEMS-IC stack is kept below 1 mm. As a further evolution of the technology, VTI has also announced a research program aimed at stacking multiple ASICs on top of the MEMS. In order to achieve this, all ASICs will be thinned down to about 20 μm, presumably with TSVs.

Summary

There is an emerging market for 3D integration of MEMS/NEMS and IC, with portable consumer electronics as one of the main market drivers. A number of challenges need to be addressed for the fabrication of TSVs through MEMS and NEMS structures, but solutions are being developed and demonstrated. Metal bonding technologies developed for packaging and 3D integration of conventional ICs will also be applicable for 3D integration of MEMS/NEMS and IC. Today, the differences in die size, wafer size and yield make chip-to-wafer bonding the preferred approach for stacking of MEMS/NEMS and IC.

Acknowledgments

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