ETCHING BURIED OXIDE AT THE BOTTOM OF HIGH ASPECT RATIO STRUCTURES

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***Abstract* — Plasma based dry etching is a key process widely used in micro-fabrication today. In this article, we look at the challenges involved in the anisotropic etching of buried SiO_2 layers at the bottom of high aspect ratio structures on SOI wafers. We present our etch results that show the limitations of using a process with radio frequency (RF) substrate bias. This is followed by results obtained with a newly developed dielectric etch process based on a pulsed low frequency (LF) bias which makes it possible to etch through even relatively thick buried oxide layers. Finally we present an application in which this newly developed process was used.**

Keywords: **Plasma etching, DRIE, Dielectric charging, SOI, Notching, High Aspect Ratio**

I - Introduction

High aspect ratio structures in silicon play an important role in many MEMS devices and are also finding a growing number of applications in other semiconductor devices. Dry anisotropic etching using high density plasmas is a key technology that is widely used for etching high aspect ratio structures in silicon. However there are several well-known phenomena that lead to non-uniformities in etch rates during deep silicon etching such as the aspect ratio dependence of the etch rate (ARDE), and loading effects (both micro-loading and macro-loading). To overcome these non-uniformities, silicon-on-insulator (SOI) substrates are often employed for fabrication of MEMS devices in order to ensure a uniform etch depth for all structures, by using the buried oxide (BOX) as an etch stop layer.

When etching high aspect ratio structures and stopping on the BOX layer, a well-known phenomenon that occurs is notching. Notching is the lateral etching of the sidewalls of the silicon structures, in the region near the interface between the silicon device layer and the BOX layer as shown in figure 1. When the BOX layer gets exposed to the plasma, it gets charged by the positive ions flux that is directed towards the substrate. Due to the charging of the BOX layer, the ion trajectories are distorted causing ions to be deflected towards the sidewalls of the etched structure [1]. This leads to undesirable lateral etching of the structures in the silicon device layer which could cause problems in the subsequent fabrication steps or hamper the performance of the devices.

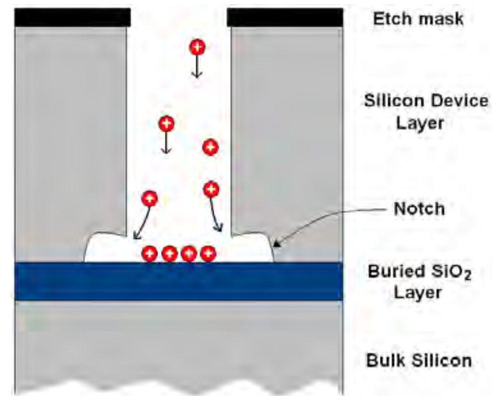

Figure 1*: Notching phenomenon resulting from the charge buildup on the buried oxide layer*

A similar notching phenomenon results when one attempts to etch through the BOX layer at the bottom of high aspect ratio structures. An additional challenge when etching buried SiO_2 in such structures is the fact that the etching of SiO_2 layers in general requires a relatively high amount of energetic ion bombardment [2]. Due to the charge buildup on the BOX layer and consequent ion deflection, the amount of energetic ion bombardment at the bottom of high aspect ratio structures is considerably reduced as compared to the top surface of the wafer, which results in a significantly lower etch rate.

In this article we report the results of our experiments to find a solution to etching through the BOX layer at the bottom of high aspect ratio structures. We then present an application where this etch process has been used successfully to fabricate MEMS devices with through silicon vias (TSVs) in the SOI substrates.

II - Experimental Setup

All experiments reported here were performed on an Alcatel AMS200 SE I-Productivity etch tool. This is a so-called downstream etch tool which is built to run a switched etch process such as the BOSCH deep reactive ion etch (DRIE) process [3]. However, it is also possible to run continuous etch processes such as dielectric etch or isotropic silicon etch, making it a very versatile tool for micro-fabrication. Figure 2 is a simplified functional illustration of the tool. The upper portion of the tool is a high density inductively coupled plasma (ICP) source. It consists of a ceramic cylinder into which various process gases (typically SF_6, C_4F_8 and O_2) are introduced. RF power from a generator is applied to a coil antenna wound around the ceramic cylinder to create a plasma. A diffusion chamber lies below the plasma

source. It is here that various ions and radicals from the plasma react with the substrate to be processed.

The substrate is electrostatically clamped onto the substrate holder. The temperature of the substrate holder is regulated by a system consisting of an external chiller unit and resistive heaters. Thermal conductivity between the substrate and the substrate holder is achieved by a flow of Helium gas between the back-surface of the substrate and the substrate holder, which is used to regulate the substrate temperature during processing.

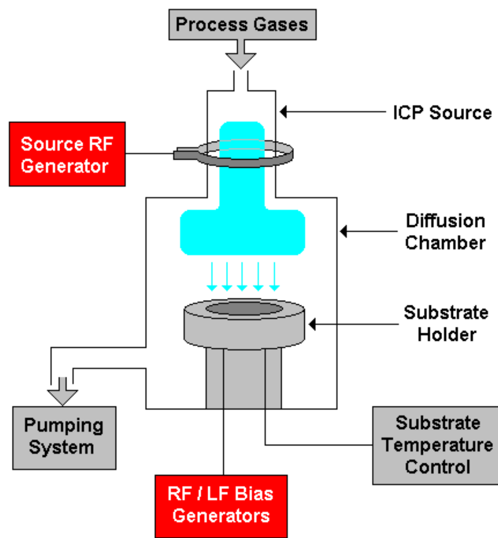

Figure 2: *Simplified functional illustration of the plasma etch tool used in the experiments*

To accelerate ionic species from the plasma sheath towards the wafer it is possible to apply an electrical bias on the substrate to be etched. In this way, the energy of ionic species arriving at the substrate is controlled independently of their flux. The biasing can be achieved either by applying RF power (13.56 MHz) or LF power (100 KHz to 460 KHz) from independent substrate bias generators. If LF bias is used, it is also possible to pulse the bias “ON” and “OFF” or between a High and Low value.

The substrates used in these experiments were all 100 mm diameter SOI wafers with a nominal thickness of 340 µm. Two types of wafers were used: The first type had a 43 µm thick device layer and a 0.5 µm thick BOX layer and the second type had a 40 µm thick device layer and 2 µm thick BOX layer. An aluminium layer (0.7 µm thick) was patterned and used as the hard-mask for dry etching. On all the wafers test structures in the form of trenches with a width of approximately 7 µm and a length of 70 µm were etched down to the BOX layer using the BOSCH process. The trenches had an aspect ratio of approximately 5:1. The goal of the experiments was to develop an etch process to etch through the BOX layer at the bottom of the trenches while keeping the etch-profile as straight as possible.

III - Results

A. Etch results on wafers with a 0.5µm BOX layer

In the first set of experiments the SOI wafers had a 43 µm thick device layer and a 0.5 µm thick BOX layer. After the trenches were etched in the silicon device layer, a standard dielectric etch recipe (Recipe RF1) which uses RF substrate bias was used as a starting point for the BOX etch. Process parameter details of this recipe are mentioned in Table 1. An etch time of 5 minutes was used, which would be sufficient to etch more than 2 µm SiO_2 on the top surface of the wafer.

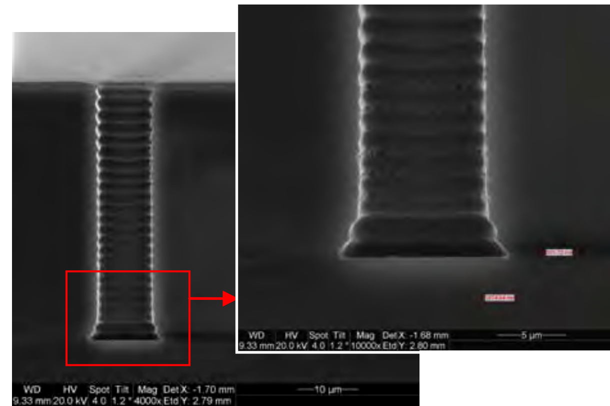

Figure 3*: Etch results obtained with a standard dielectric etch process (Recipe RF1) on a SOI wafer with 0.5µm thick BOX.*

Figure 3 shows SEM cross-sections of the etch result. It appears that virtually no buried oxide was etched. We also see a considerable amount of notching at the bottom of the device layer (> 1.8 µm on each side). We know that the notching resulting from the device layer etch (BOSCH process) was less than 0.7 µm. Thus during the BOX etch, the width of the notch increased by more than 1 µm.

In an attempt to increase the energy of the ions arriving at the BOX layer, a new recipe was developed (Recipe RF2) with double the applied RF substrate bias power, half the process pressure and half the C_4F_8 gas flow as compared to Recipe RF1.

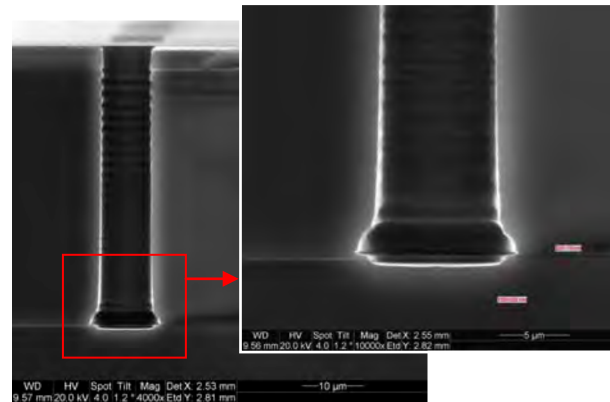

Figure 4*: Etch results obtained with Recipe RF2 on a SOI wafer with 0.5µm thick BOX.*

Figure 4 shows the etch result for Recipe RF2 with an etch time of 8 minutes. It is clear that significantly increasing the ion energy made it possible to etch through the BOX layer. Notching is still a problem, even though it is slightly reduced (to about 1.6 µm on each side).

B. Etch results on wafers with a 2µm BOX layer

In the next set of experiments the SOI wafers had a 40 µm thick device layer and a 2 µm thick BOX layer. At first we attempted to etch through the BOX layer using Recipe RF2 that was successfully used to etch a 0.5 µm BOX layer. However in this case, even after a relatively long etch time of 14 minutes, very little of the BOX layer was etched. Figure 5 shows SEM images of the etch result. Near the bottom corners of the trenches only about 170 nm of the BOX layer was etched while at the centre of the trenches no BOX was etched at all. In fact in the centre of the trenches we observe a build up of polymer residues on top of the BOX layer. We also see a very significant amount of notching (> 3.6 µm on each side) which was unacceptable for our application.

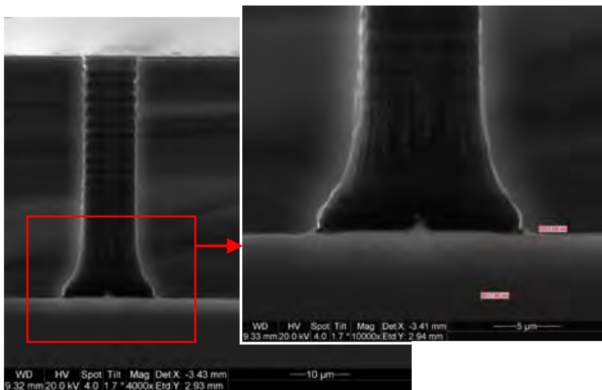

Figure 5: *Etch results obtained with Recipe RF2 on a SOI wafer with 2µm thick BOX.*

Another limitation that became apparent was that due to the high energy ion bombardment onto the wafer, the aluminium hard-mask eroded rapidly. As only about 150 nm of the aluminium mask was left, it was difficult to increase the etch time further.

As it became clear that a RF substrate biasing scheme had its limitations, we experimented and developed a new etch process (Recipe LF1) based on a pulsed LF substrate biasing scheme instead of RF biasing. Figure 6 shows the etch results obtained after 35 minutes of etching with this process. It is evident that pulsed LF biasing made it possible to etch through the 2 µm thick BOX layer. The amount of notching is also very little (< 0.7 µm on each side). In fact keeping in mind that we already had up to 0.7 µm of notching after the device layer etch itself, the increase in notching due to this BOX layer etch is insignificant. In addition, only approximately 270 nm of the aluminium mask was consumed.

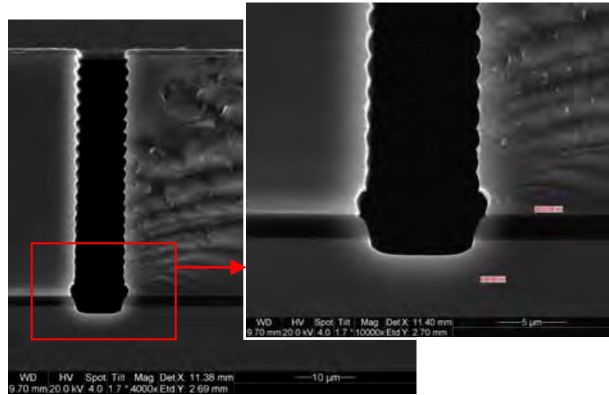

Figure 6: *Etch results obtained with Recipe LF1 on a SOI wafer with 2µm thick BOX.*

More detailed process parameters for each etch recipe are given in Table 1.

Parameter	Recipe RF1	Recipe RF2	Recipe LF1
Source power	2800 W	2800 W	2800 W
C_4F_8 gas flow	50 sccm	25 sccm	25 sccm
Pressure	0.6 Pa	0.3 Pa	0.3 Pa
Substrate-holder temperature	20 °C	20 °C	20 °C
Substrate bias power	100 W (RF 13.56 MHz)	200 W (RF 13.56 MHz)	100 W (LF 200 KHz, pulsed)

Table 1: *Process parameter details of the etch recipes*

Table 2 gives a summary of various etch rates measured for each process. Although for these experiments an aluminium hard mask was used, the etch rate of a commonly used positive photoresist (HiPR 6512) was also measured for all the etch processes in order to give an idea about the selectivity of a photoresist mask.

Parameter	Recipe RF1	Recipe RF2	Recipe LF1
Avg. etch rate of top surface SiO_2 (nm/min)	456	609	202
Avg. etch rate of 0.5 µm BOX layer (nm/min)	~0	~167	~120
Avg. etch rate of 2.0 µm BOX layer (nm/min)	~0	~0	~105
Avg. photoresist etch rate (nm/min)	310	526	115
Avg. aluminium etch rate (nm/min)	12.3	38.9	7.8

Table 2: *Summary of etch rates for all etch processes*

IV - Discussion

The experimental results show that the use of a RF substrate bias leads to charging of the BOX layer, causing ion trajectories inside the trenches to diverge towards the sidewalls of the trenches. This results in lateral etching of the silicon device layer leading to notch formation. Another consequence of the charging is that it reduces the ion bombardment onto the BOX layer which significantly reduces the etch rate.

Although pulsed LF biasing has been used to limit notching in deep silicon etching [4,5], to our knowledge its use in etching of the BOX layer has not been reported in literature until now. The use of a pulsed LF bias addresses the root cause of the problem which is the charging of the BOX layer. The 'ON' time of the pulses provide enough ion energy to etch the BOX layer while the built-up charge gets enough time to discharge during the 'OFF' time of the pulses

V - Application

Fragile MEMS structures are usually protected from the environment by bonding a capping wafer to the device wafer. As opposed to using lateral interconnects at the interface between the cap wafer and the device wafer, the use of vertical TSVs significantly simplifies the mounting of the components and it also results in the smallest geometry. Figure 7 shows a schematic cross-section of a MEMS accelerometer that was fabricated as part of the European ENIAC Joint Undertaking project JEMSIP-3D. The newly developed pulsed LF bias etching process made it possible to successfully fabricate TSVs through the SOI wafer.

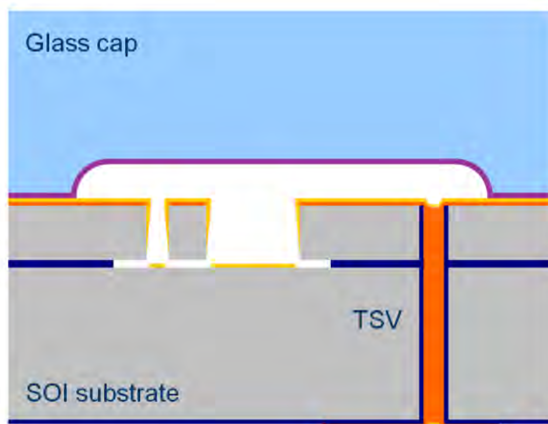

Figure 7: *A schematic crosss-section of a MEMS accelerometer with TSV through the SOI wafer.*

Using a via-first approach, TSVs were first created on the SOI wafers followed by the fabrication of the MEMS devices. Plasma etching was extensively used for fabricating both the TSVs and the MEMS structures. For creating the TSVs, three consecutive anisotropic etch steps were performed using an aluminium hard-mask. First the silicon device layer was etched using the BOSCH DRIE process, followed by dry etching of the 2 µm BOX layer using the LF bias etch process. This enabled us to minimize the notching at the bottom of the device layer which would have led to void formation in the vias at a later stage in the processing. Finally, another multi-step BOSCH DRIE process was used to etch through the silicon handle wafer. The vias were then isolated with thermal oxide and made conductive by filling them with heavily doped polysilicon. More details regarding the fabrication process of the TSVs and MEMS devices are available in another article [6].

VI - Conclusion

In this article, we have looked at the challenges involved in the anisotropic etching of buried SiO_2 layers at the bottom of high aspect ratio structures. We have shown that for this purpose a dielectric etch process using RF bias has significant limitations: very low etch rate, notching issue, and low selectivity to the etch mask. The root cause of the problem is the charging of the BOX layer which causes ion trajectories to diverge towards the sidewalls of the high aspect ratio structures. We have successfully developed a new dielectric etch process using pulsed LF bias which addresses the problem and makes it possible to etch through even relatively thick buried oxide layers. This new process has been applied successfully for the fabrication of through silicon vias in a MEMS application.

Acknowledgements

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