TSV development for miniaturized MEMS acceleration switch

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Abstract

This poster presents a new concept for fabricating a MEMS acceleration switch with through silicon vias (TSVs) through the SOI (silicon on insulator) device wafer. Results of the short-loop experiments conducted in order to develop the most critical process steps are shown. The use of TSVs significantly simplifies the mounting of the MEMS devices and it results in the smallest footprint.

Concept

If subjected to a sufficient acceleration, the released silicon structure will move in the lateral direction and make contact with the sidewall of a neighbouring structure, thereby opening or closing a circuit.

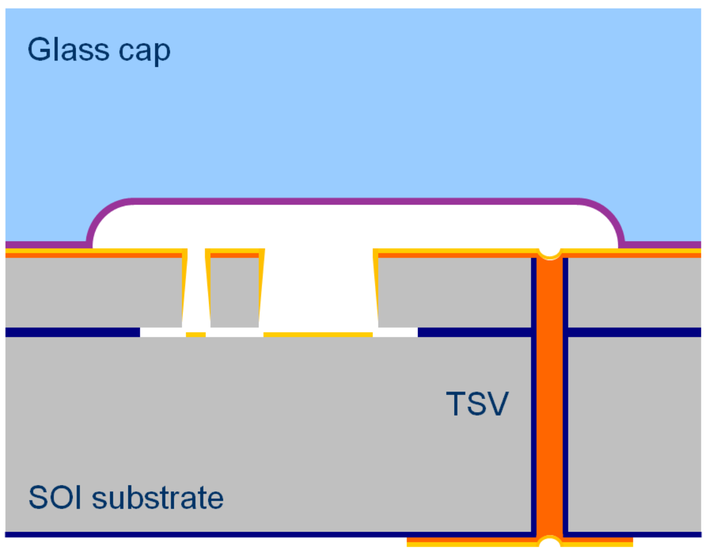

Fig. 1 : Schematic cross-section of the MEMS acceleration switch with TSV.

Process sequence

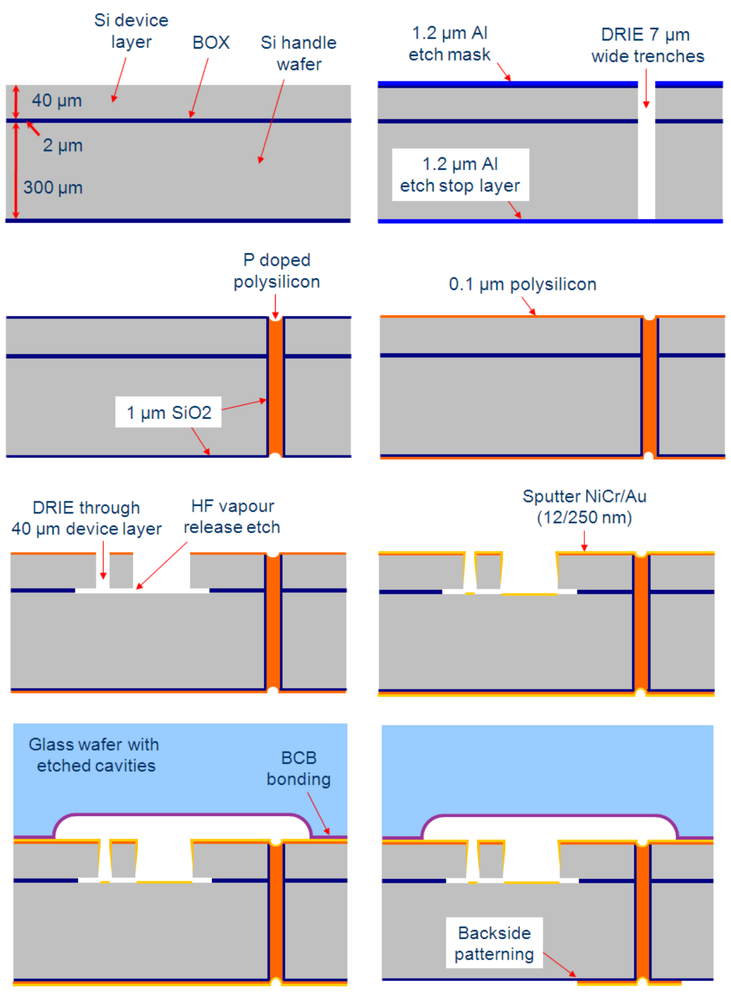

Fig. 2 : Proposed process sequence for the miniaturized acceleration switch.

TSV etching

Deep reactive ion etching (DRIE) is used to etch 7 x 70 µm trenches consecutively through the 40 µm silicon device layer, 2 µm buried oxide (BOX) and 300 µm silicon handle wafer. This results in an aspect ratio close to 50:1. The etch tool that is used is an Alcatel AMS200SE I-Productivity silicon etcher.

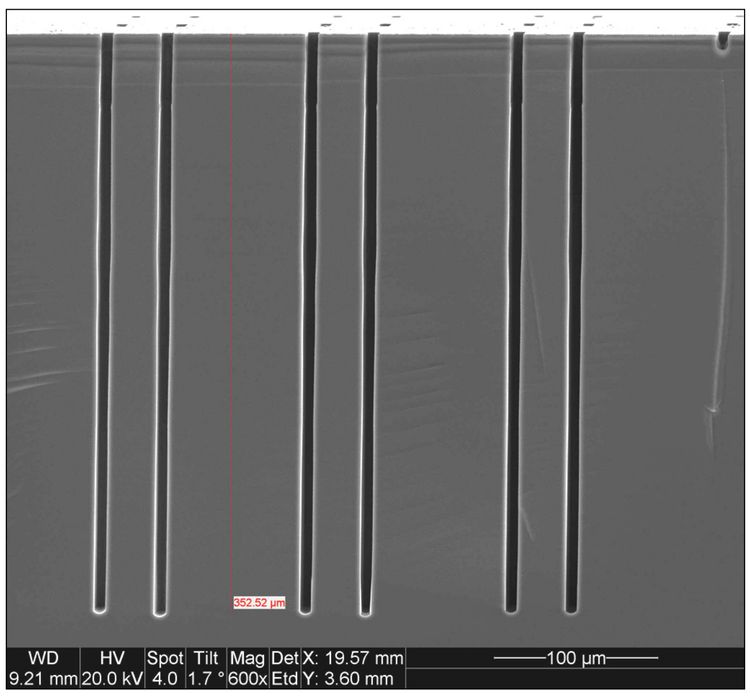

Fig. 3 : SEM cross-section of a bulk silicon test wafer after performing the device layer DRIE followed by the handle wafer DRIE.

A major challenge is the etching of the 2 µm thick BOX layer at the bottom of trenches that are 40 µm deep and only 7 µm wide. A new etch recipe was succesfully developed for this purpose.

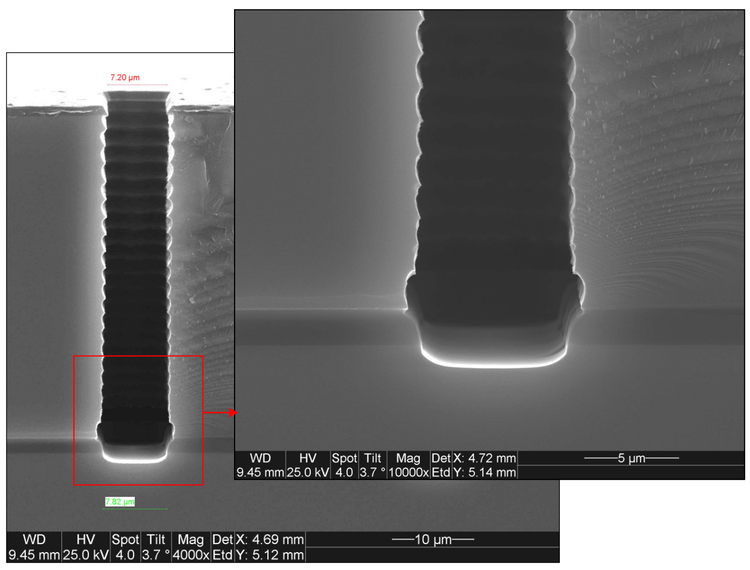

Fig. 4 : SEM cross-section of an SOI wafer after etching 7 x 70 µm trenches through the 40 µm silicon device layer and 2 µm BOX.

Acknowledgment

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TSV filling, etchback and metallisation

TSVs with a width of 7 µm were etched through 300 µm thick silicon wafers (aspect ratio 42:1). The vias were isolated from the bulk silicon by thermal oxide and filled with phosphorus doped polysilicon.

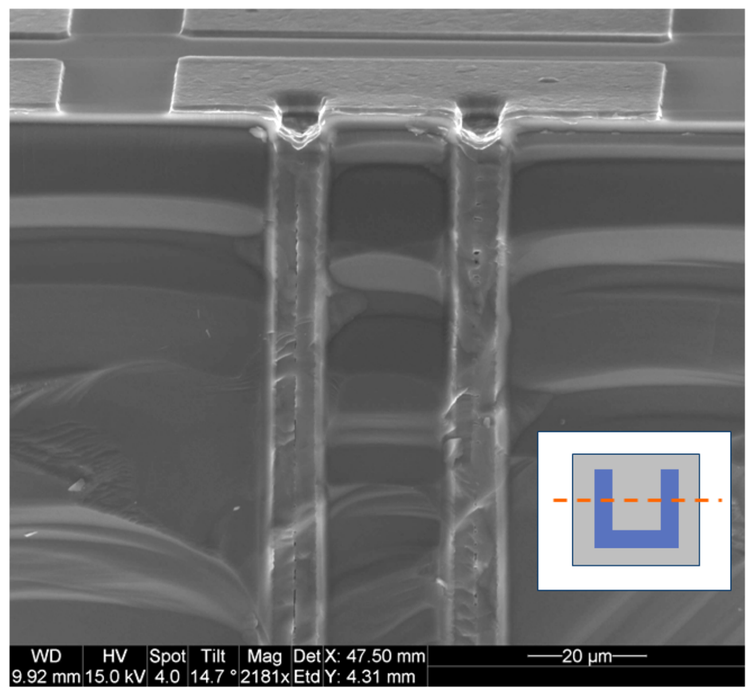

Fig. 5 : SEM cross-section of a U-shaped TSV structure after patterning of the metallization.

Following etchback of the polysilicon, metal deposition and patterning, the TSVs showed excellent electrical results and high yield.

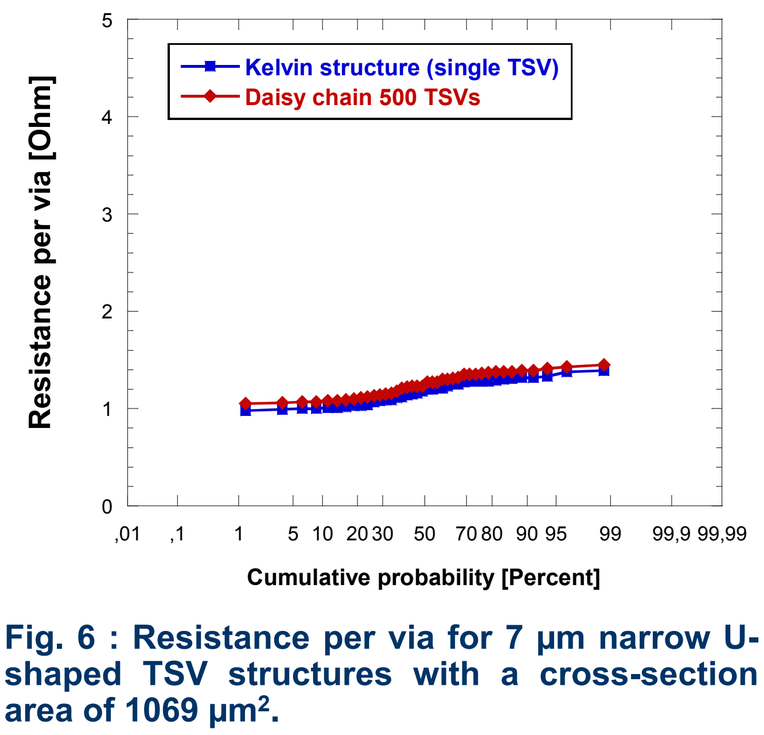

Fig. 6 : Resistance per via for 7 µm narrow U-shaped TSV structures with a cross-section area of 1069 µm².

Conclusions

A novel concept is proposed for fabricating a miniaturized acceleration switch. The most critical process steps for realizing TSVs through the MEMS device wafers were successfully developed. Processing of a complete demonstrator as shown in Fig. 1 is ongoing.

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