

Acoustic/Electronic stack design, interconnect, and assembly Techniques available and under development

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under support-no. IST-026461 e-CUBES

Maaikje M. V. Taklo : SINTEF, Norway

MI-lab Work-shop on future ultrasound probe
technology

Trondheim, March 26. 2009

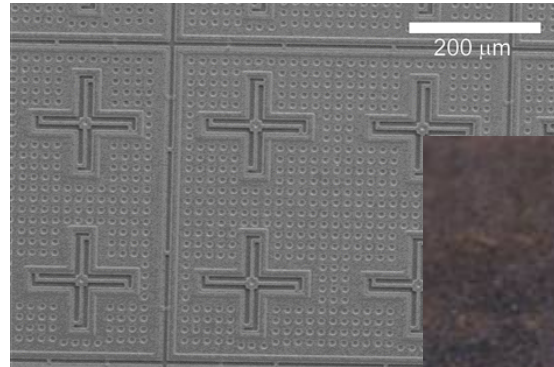
Outline

- 3D integration of MEMS/IC
- Solutions for through silicon vias
- Solutions for interconnects
- Examples of applied technologies
- Coming project
- Summary

MEMS: Micro electromechanical systems

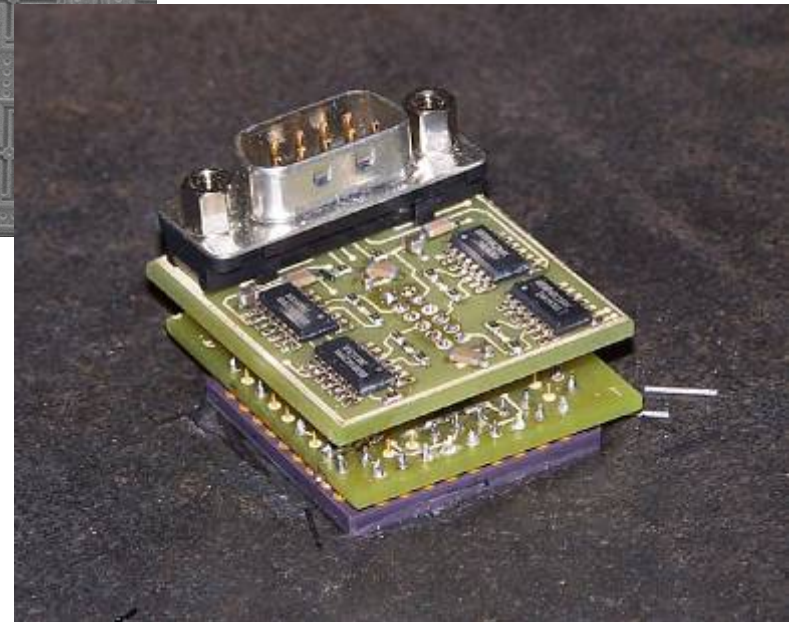
■ Enables

- Sensors
- Actuators
 - cMUT: Both



■ Demands

- “Window” to the environment
- ASICs for calibration and control
 - cMUT: Logic and memory



Source:
www.ece.cmu.edu/~dwg/research/ae.html

Existing packaging solutions

Analog Devices Inc,
ADXL330

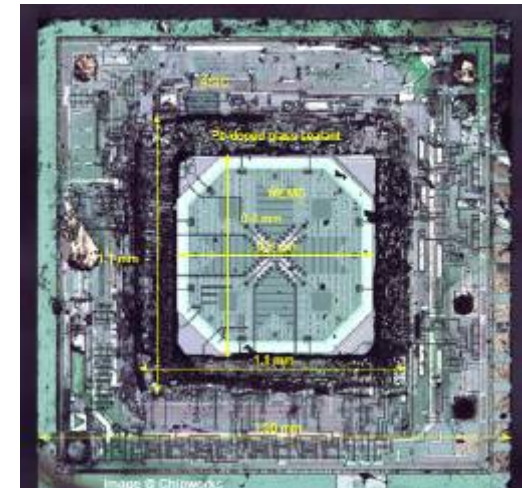
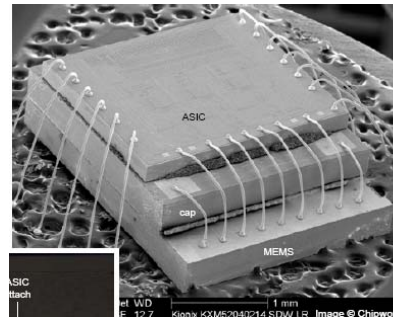
Market driver examples

- Nintendo Wii
- Mobile phones

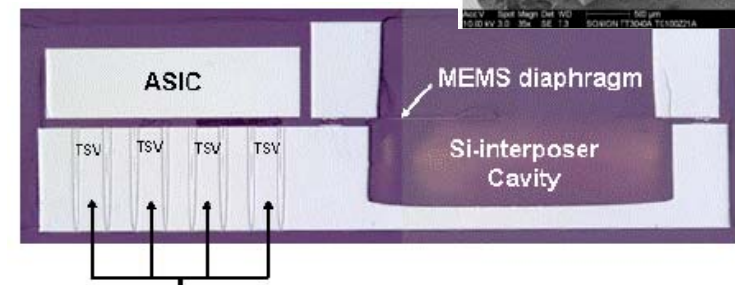
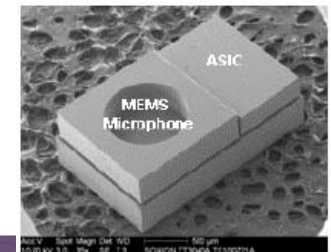
The progress

- Side by side, wire bonded
- 3D stacked with wire bonds
- Integrated in-plane
- Interposer with through silicon vias (TSVs)
- Wafer level packaging...

Kionix, KXPB5

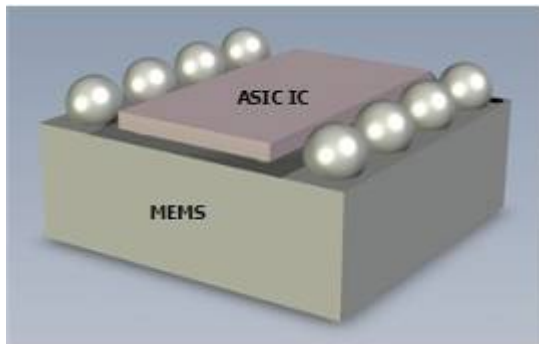


Source: CHIPWORKS



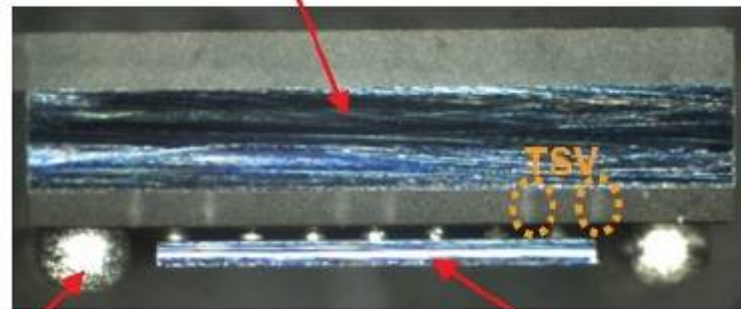
Wafer level packaging (WLP)

- No wire bonds
 - Through Silicon Vias (TSVs) required
 - Interconnects defined on wafer level
- Ready for surface mounting after final dicing



Source: VTI

Hermetically sealed MEMS Sensing element



Solder bumps for interconnection

Signal conditioning ASIC

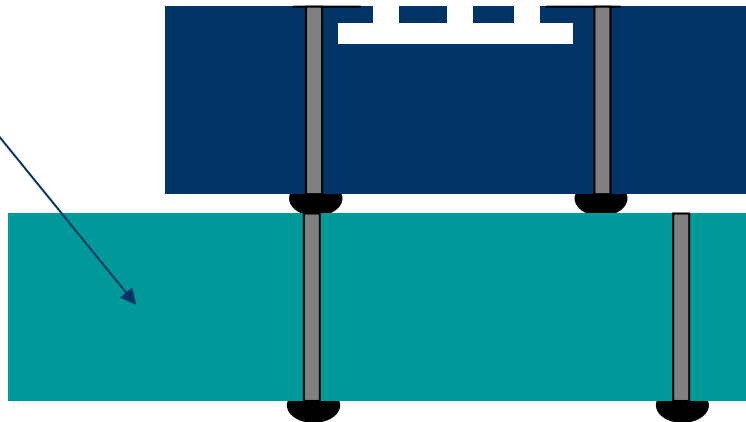
cMUTS: MEMS wafer TSVs / interposer

Surface
micromachining
or based on
bonding



Interposer

RDL



TSV technology choice

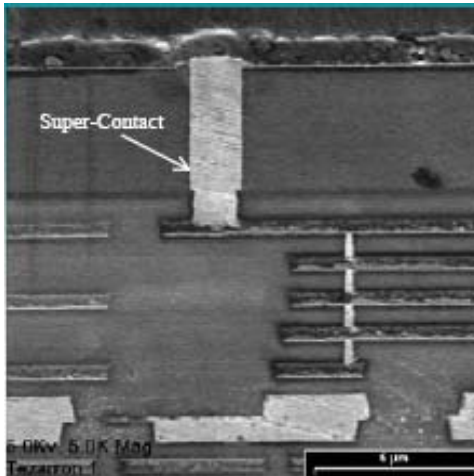
Pitch: 25 μm

Wafer thickness: 30-100 μm

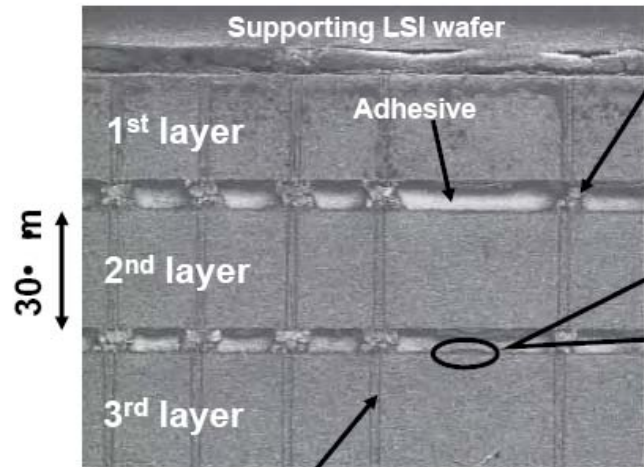
Aspect ratio: 10-20

TSVs

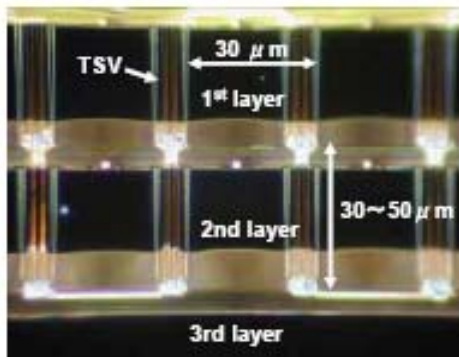
Pitch <math><50 \mu\text{m}</math>, wafers <math><100 \mu\text{m}</math> (ICs)



Source: Tezaron



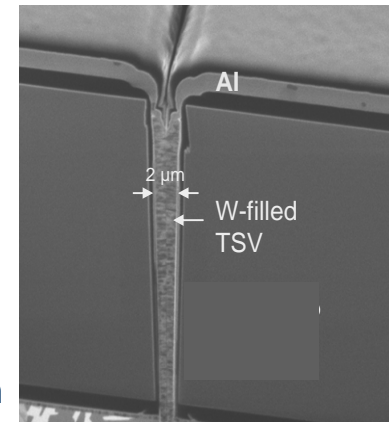
Source: ZyCube



Source: Honda

Poly Si, W, Cu,
conductive paste

Source:
Fraunhofer
IZM-Munich



Definitions of TSVs

- Front-end-of-line (FEOL)
 - Before IC wiring
- Back-end-of-line (BEOL)
 - During IC wiring in IC foundry
- Post-BEOL
 - Following complete IC fabrication
- Vias First
 - Made before wafer bonding
- Vias Last
 - Made after wafer bonding and thinning



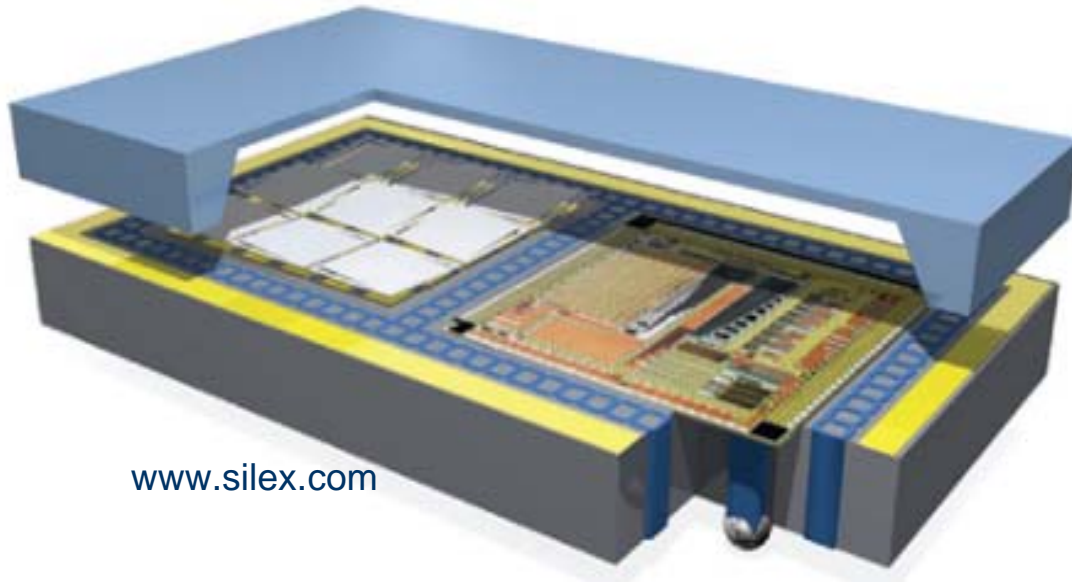
Source: Fraunhofer IZM

Handbook of 3D Integration (Garrou, Bower and Ramm)

TSVs

Pitch $>50 \mu\text{m}$, wafers $>100 \mu\text{m}$ (MEMS)

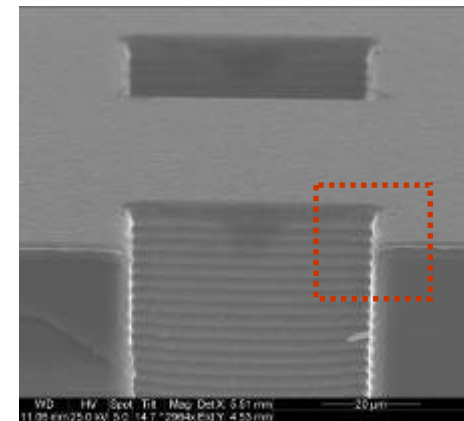
Si pins in Si



www.silex.com

Poly Si

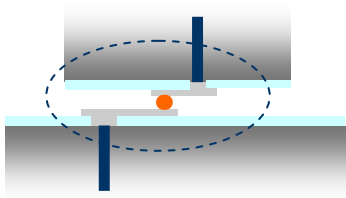
Hollow vias in Si



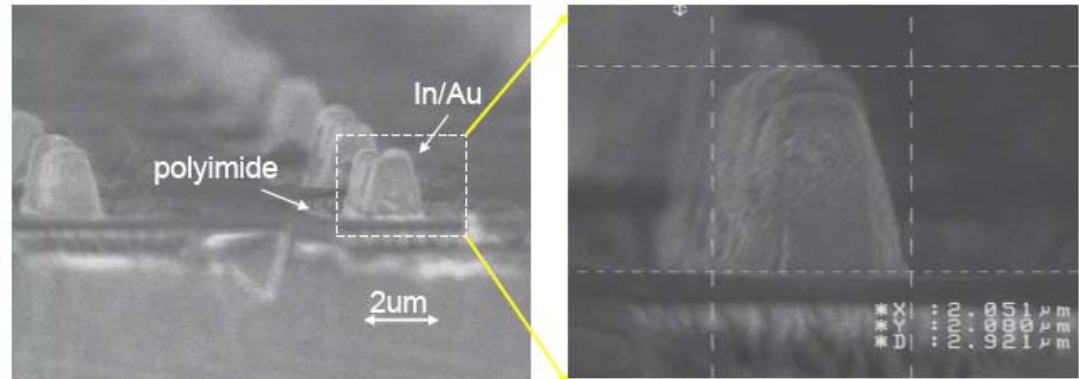
Source: SINTEF

Interconnects

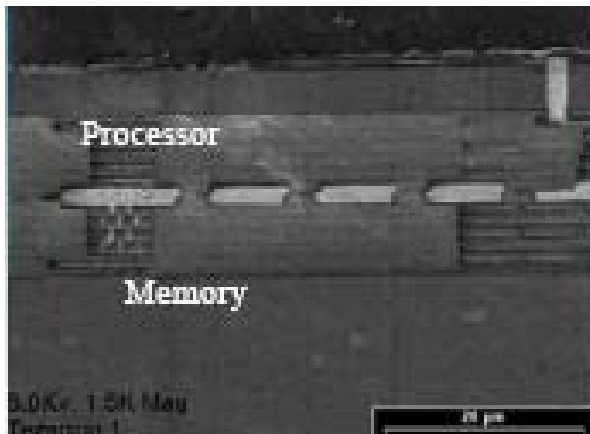
Pitch <math>< 50 \mu\text{m}</math>, stand-off height $\sim 5 \mu\text{m}</math>$



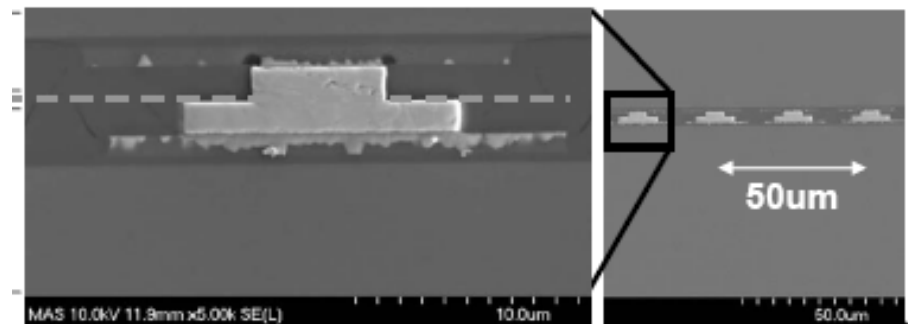
In/Au, Cu, Ni



Source: ZyCube



Source: Tezzaron

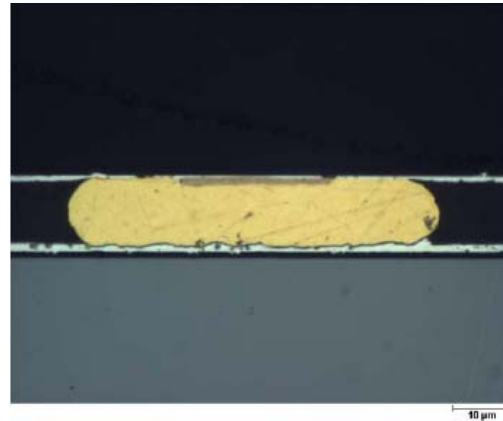


Source: Ziptronix

Interconnects

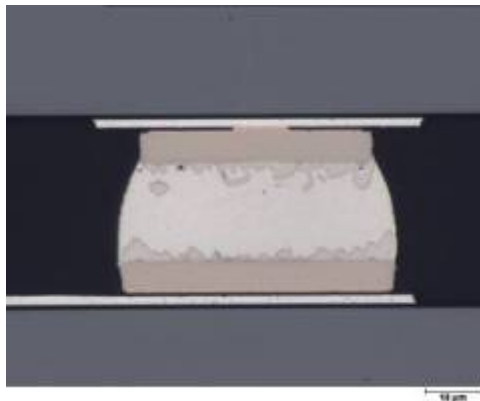
Pitch $>50 \mu\text{m}$, stand-off height $\sim 10\text{-}20 \mu\text{m}$

Au stud bump
bonding (SBB)



Source:
SINTEF/Datacon

SnAg/AuSn microbumps

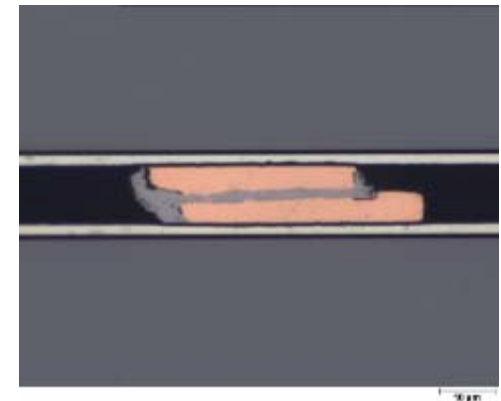


Source: SINTEF/Fraunhofer
IZM-Berlin

Au, Cu/Sn, SnAg,
AuSn

Source:
SINTEF/
Fraunhofer
IZM-Munich

Cu/Sn SLID



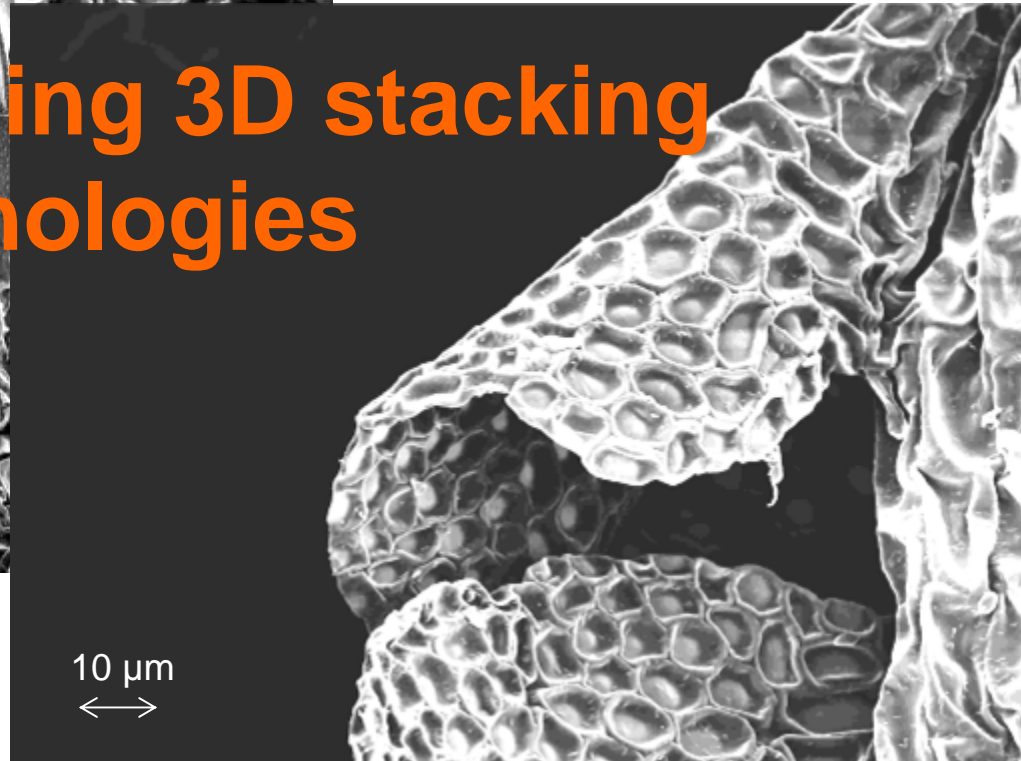
Lesson learned from nature about 3D stacking

Moss, flexible by thinning

Examples using 3D stacking technologies



High aspect ratio pillars on a leaf



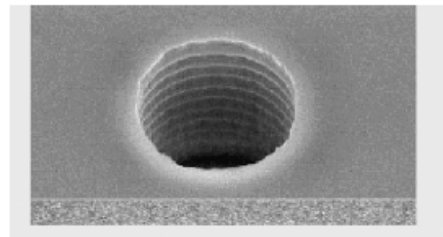
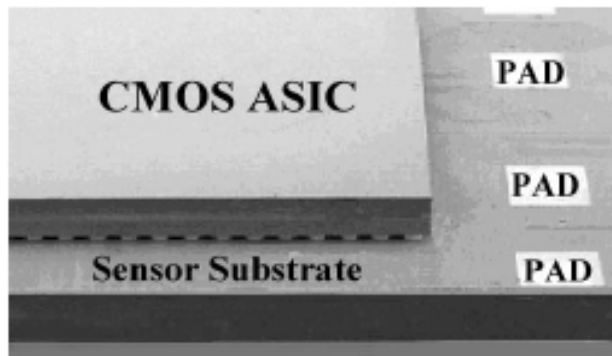
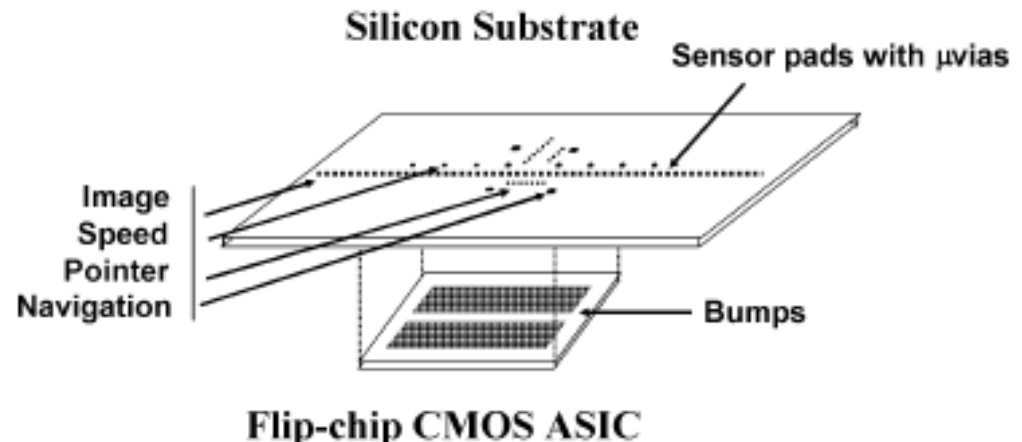
Source: MEMS-Point, Thomas Brunswiler

3D integrated planar silicon sensor



■ Fingerprint sensor

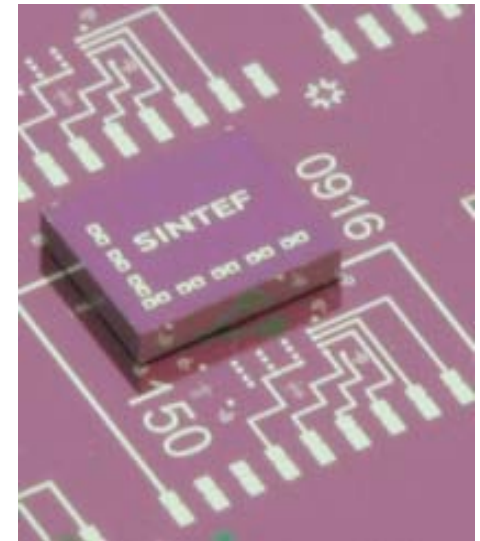
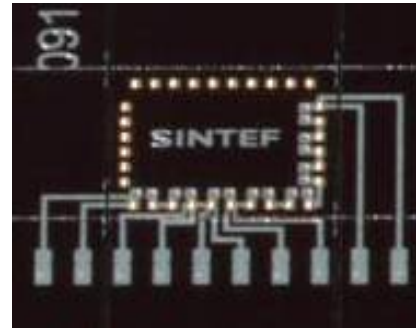
- Navigation and pointer detection
- TSVs through sensor
 - Pitch 50 μm
 - 20 μm wide
- Bumps for interconnect
 - Routed out



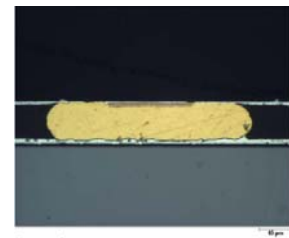
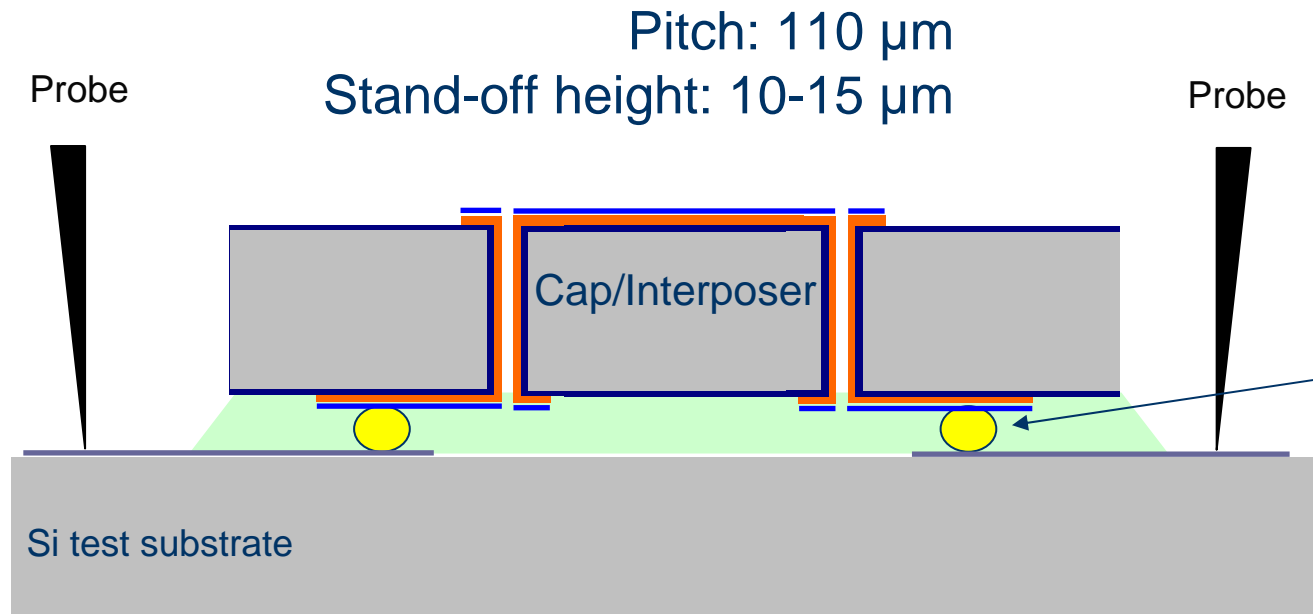
O. Vermesan et al, IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, December (2003) / www.idex.no

Technology demonstrator

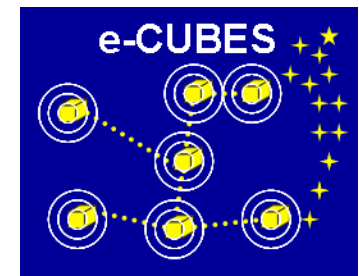
- Hollow vias with gold stud bumps (HoViGo)
 - High yield
 - Good reliability



Source: SINTEF

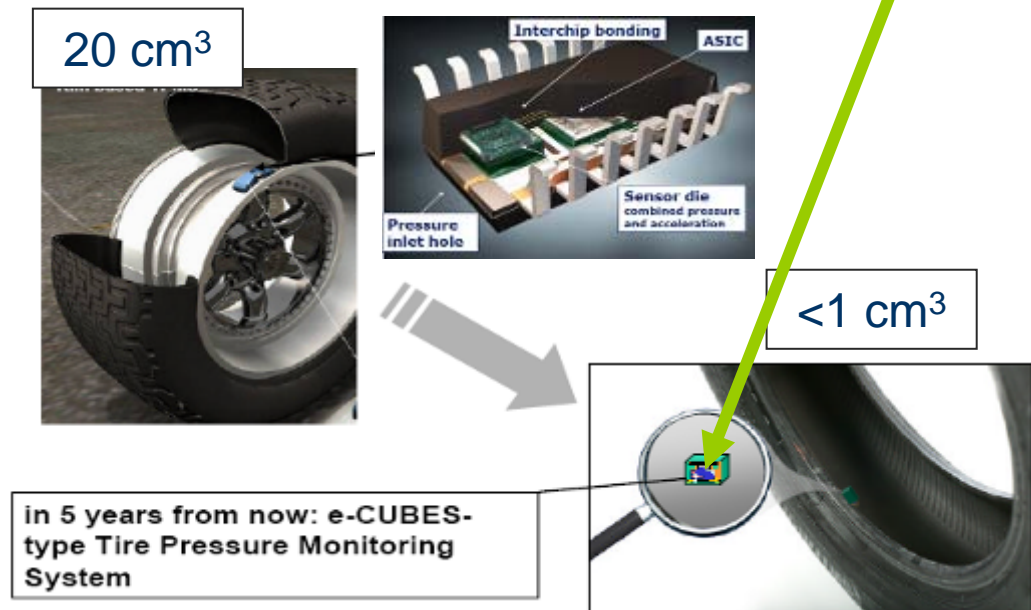


e-CUBES TPMS demonstrator



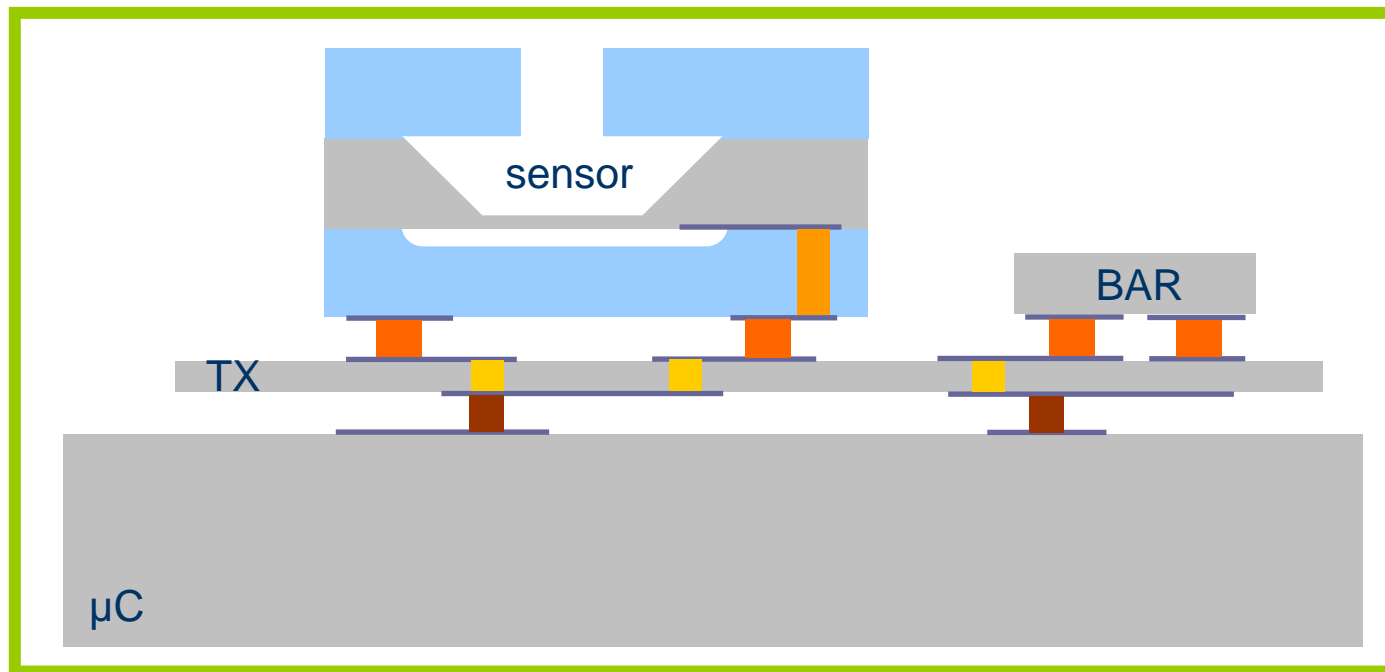
- Develop wireless sensor networks with miniaturized sensor nodes
- 3 demonstrators
 - Health and fitness
 - Aeronautics and space

- Automotive
 - Tire Pressure Monitoring System (TPMS)



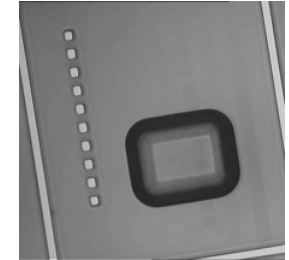
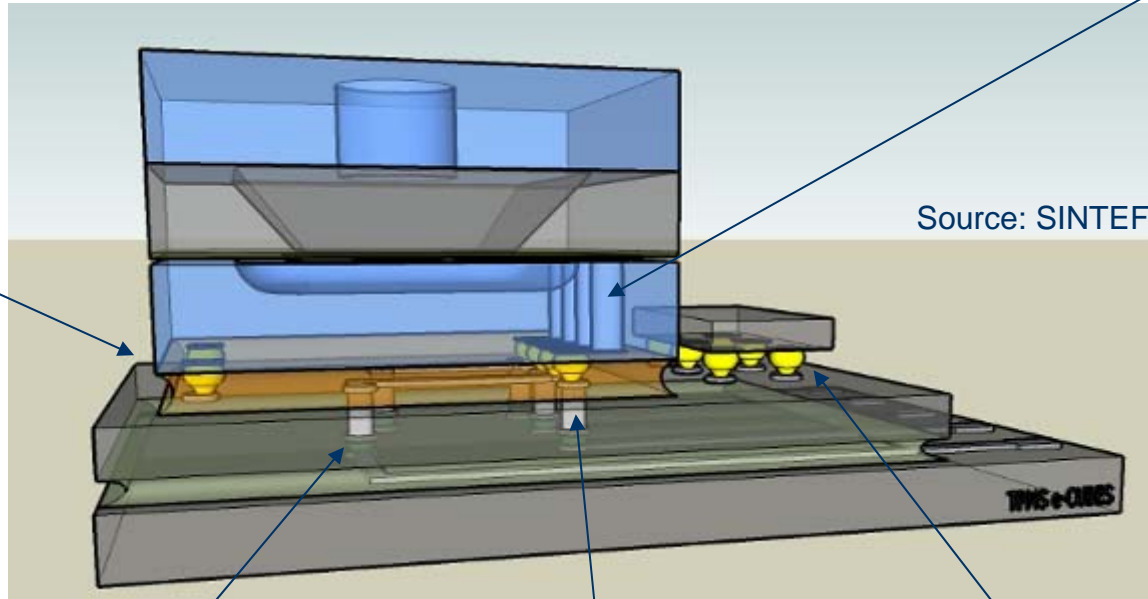
TPMS building blocks

- μ -controller ASIC (μ C) : 4.3 x 3.8 mm²
- Transceiver ASIC (TX): 3.8 x 3.3 mm²
- MEMS pressure sensor: 1.8 x 2.1 mm²
- MEMS bulk acoustic resonator (BAR): 0.8 x 1.3 mm²
 - Antenna, battery, outer package



Technology choices

Silicon-glass compound wafer with TSVs
(alternative : hollow TSVs)

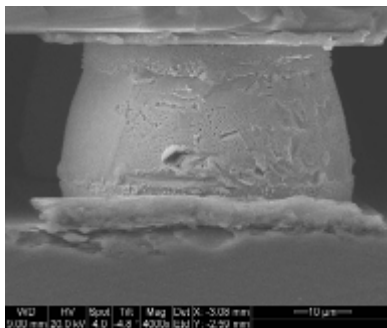


Source:
SINTEF/
SensoNor/
PlanOptik

Au stud bumps with adhesive
(alternative :
SLID)

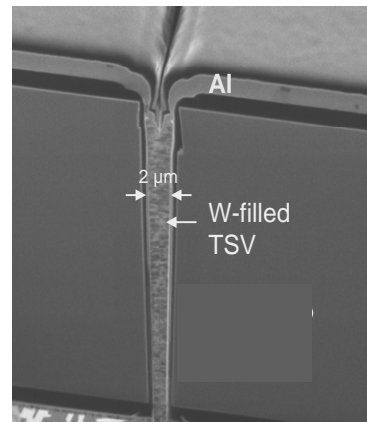
Source: SINTEF

SnAg microbumps
and underfiller



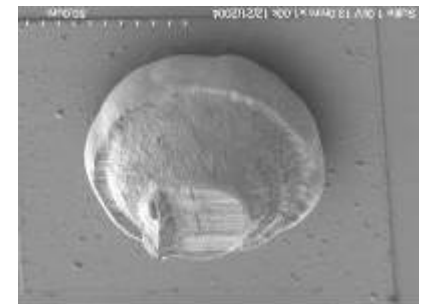
Source: SINTEF/
FhG IZM- Berlin

TSV with W



Source:
Fraunhofer
IZM-Munich

Au stud bumps only
(alternative : SLID)

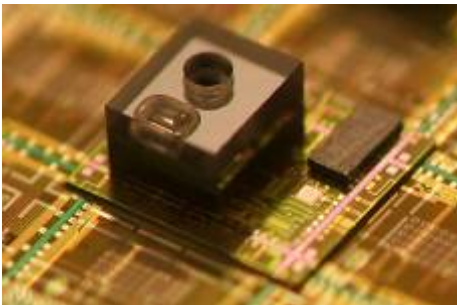


Source: Kulicke & Soffa

TPMS demonstrator results

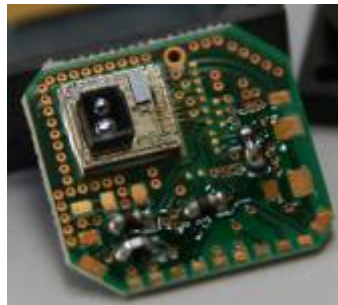
- Successful measurements on PCB level
 - Communication with TX
 - Communication with μC
 - BAR is running at correct frequency
- Sensor performance to be measured soon

MEMS / TX / μC 3D stack



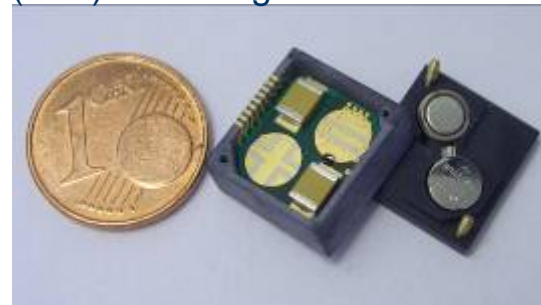
Source : SINTEF

Micro-PCB



Source : Infineon Technologies

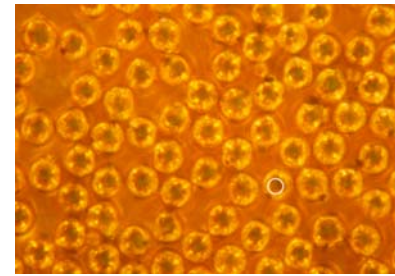
Molded Interconnect Device (MID) with integrated antenna



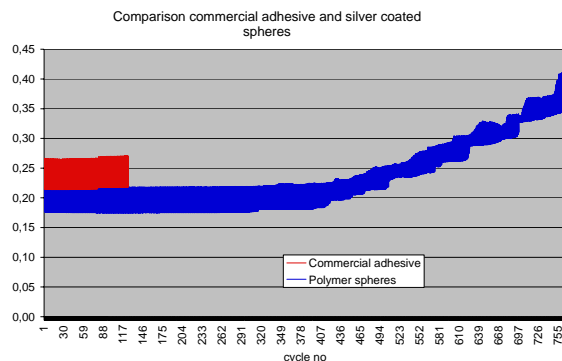
Miniaturized TPMS ~ 1 cm³



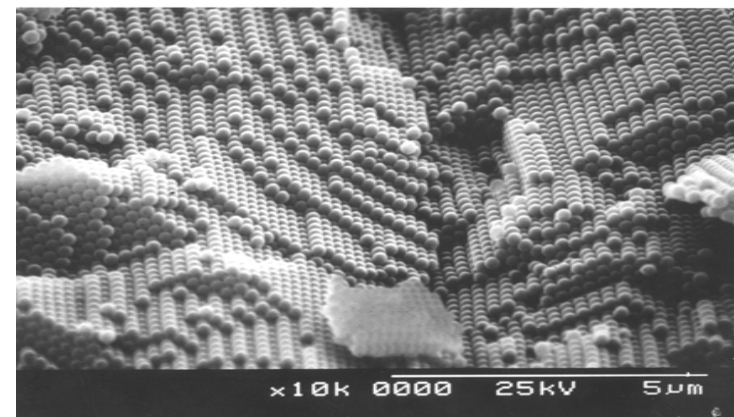
ReMi (KMB, BIA)



- Fine Pitch Interconnect of Microelectronics and Microsystems for use in Rough Environments
- 3 case studies
 - New or significantly improved devices for challenging environment applications
- SINTEF, VUC, FFI
- 6 Norwegian companies



Metal coated polymer spheres (ICA/ACA/ACF)

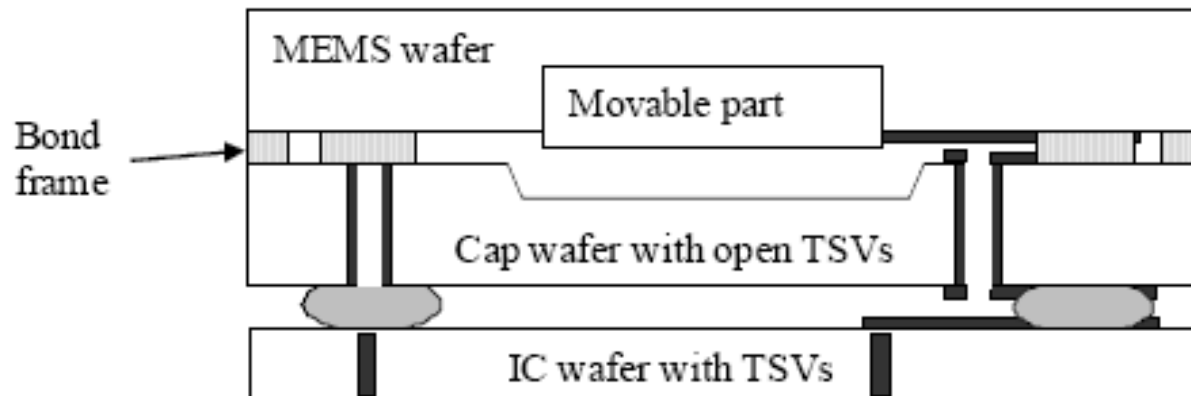


Source: Conpart

Coming:

JEMSiP 3D

- ENIAC
- SUB-PROGRAMME 8
 - Equipment & Materials for Nanoelectronics
- 20 partners
 - SUSS, FCI, FhG, LETI, Infineon, ALES, ASM...etc
- Kick-off: 2009-04-07



Summary

- A number of 3D stacking technologies are emerging
- Technology choice depends on required
 - Pitch
 - Aspect ratio
 - Stand-off height
 - Number of I/O counts
 - Compatibility of wafer/processes
- Research has come quite far, large activity
 - www.3dic-conf.org
- Industry coming
 - Optical devices
 - MEMS

Acknowledgements

- Colleagues of the e-CUBES project, especially
 - Werner Weber, Thomas Herndl and Josef Prainsack, Infineon Technologies
 - Timo Seppänen, Infineon Technologies SensoNor
 - Peter Ramm, Josef Weber and Lars Nebrich, Fraunhofer IZM-Munich
 - Jürgen Wolf and Matthias Klein, Fraunhofer IZM-Berlin
 - Nicolas Lietaer, Thor Bakke, Hannah Rosquist, Kari Schjøelberg-Henriksen ..., SINTEF
- Vincent McTaggart, Kulicke and Soffa Industrial (KNS)
 - For providing the bumping service
- Gerhard Hillmann, Datacon Technology GmbH
 - For providing the chip to wafer bonding service and process development

