2nd run of full 3-D detectors at SINTEF

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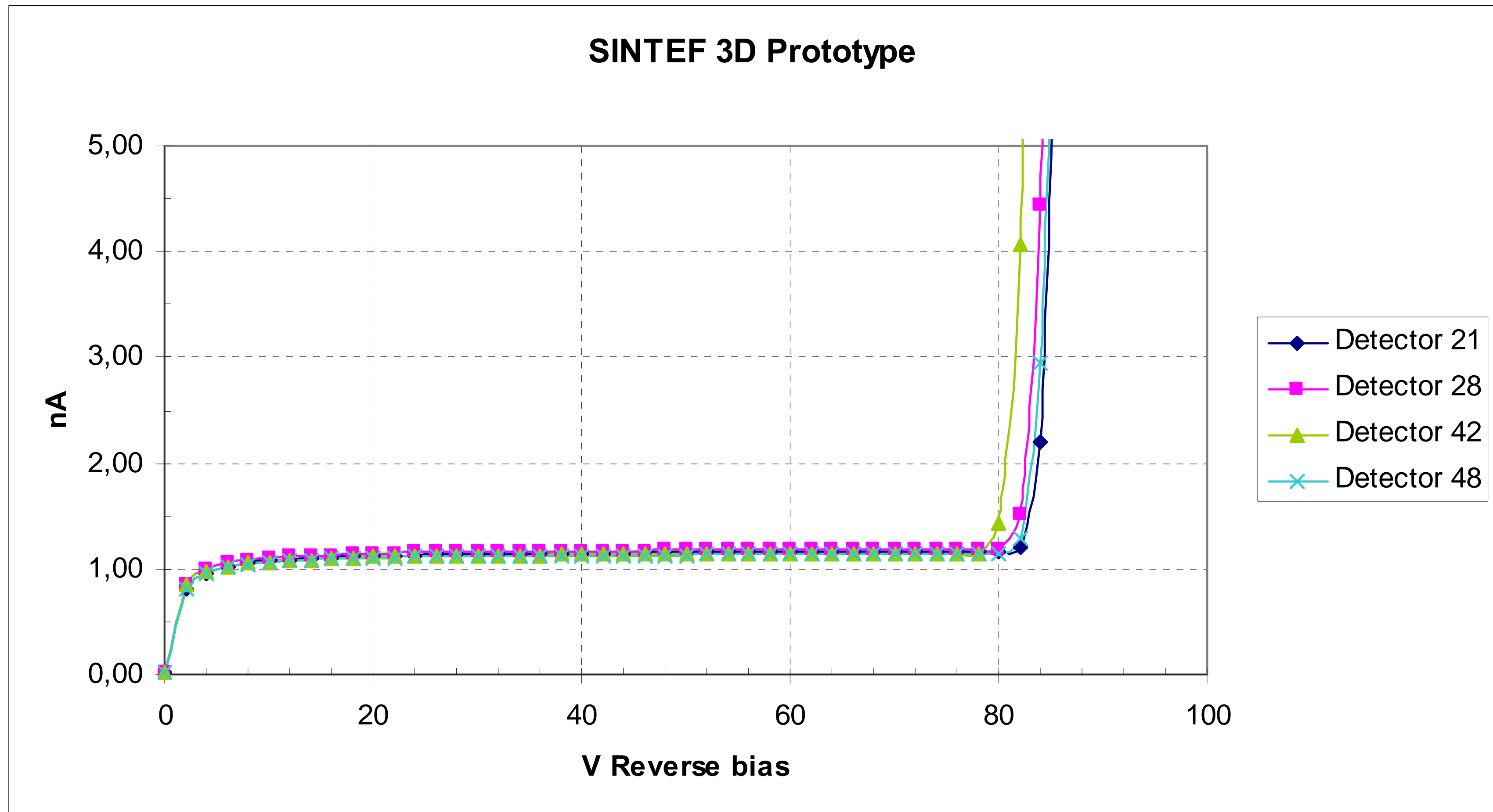
Summary of first run

- First wafer run:
  - Prototype run completed in May 2008. ATLAS pixel layout designed by Chris Kenney
  - 25 wafers, high resistivity n-type substrates
  - Low yield due to wafer breakage caused by high induced stress
  - Measurements at wafer level showed acceptable diode characteristics and high inter-pixel resistance
- Limitations at SINTEF
  - Polysilicon filling have to be performed at Stanford. SINTEF LPCVD is restricted to deposition of ≤ 1μm
- Problems after 3D-stacking
  - 10 chips bump-bonded to ATLAS FE - I3 chip
  - Highly increased leakage current after bump-bonding on most chips.
  - Problems connected with wafer dicing of n-readout devices with p- active edge made on n-type wafers. 2nd run on p-type wafers

ALTAS 4E chip – average pixel leakage current

calculated from measurement of total leakage current – 2700 pixels

4 different chips



Inter pixel / strip resistance

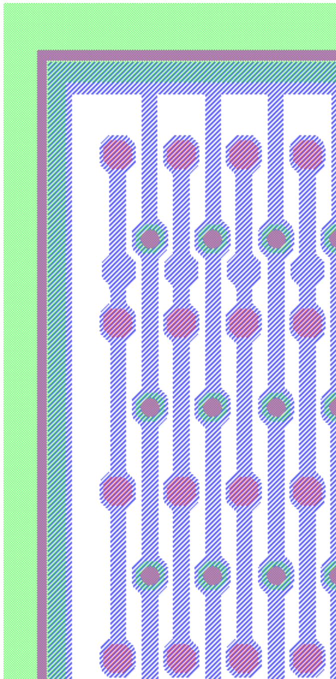
Measured between two neighbouring pixels of n-electrodes when biased at 60 V

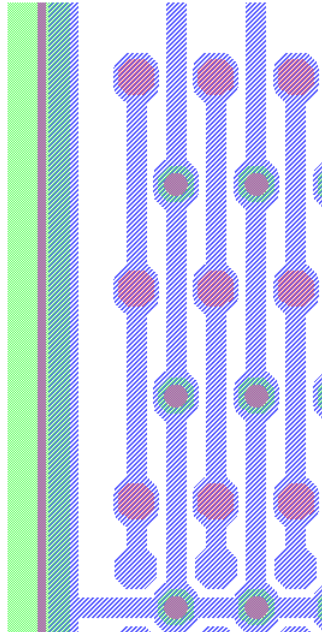
4E structures:
100-300 MΩ

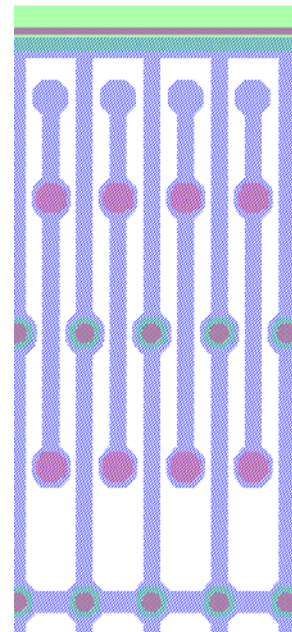
3E structures:
300-500 MΩ

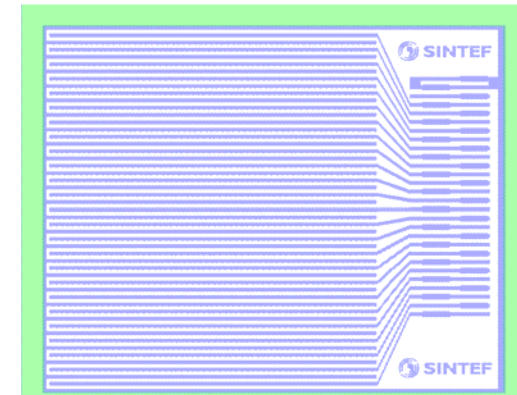
2E structures:
600-800 MΩ

Baby strip:
6.0 - 6.5 GΩ



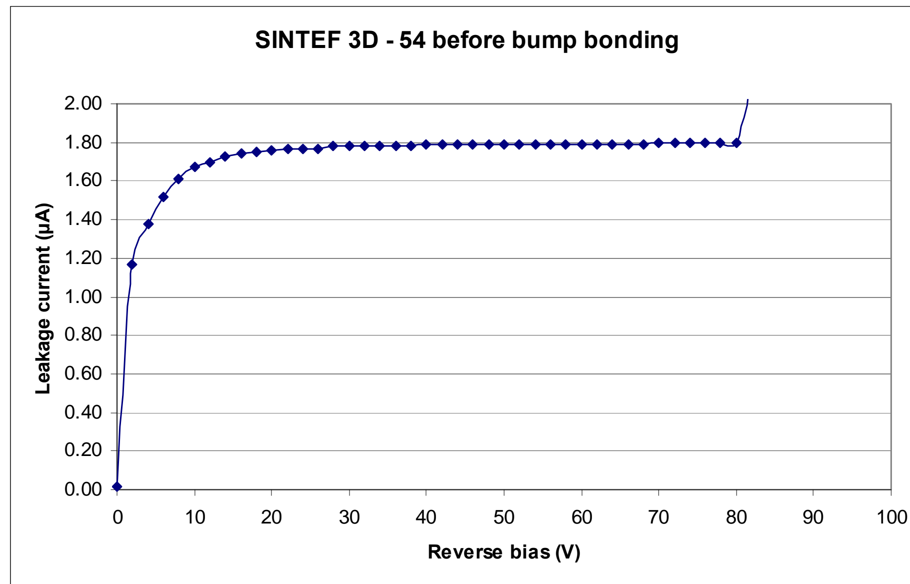


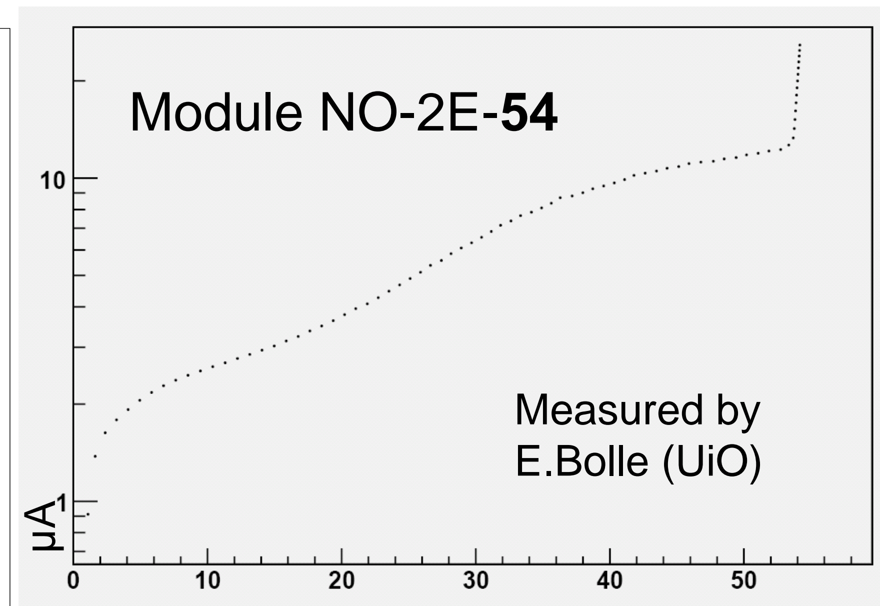




IV measurements before / after bump-bonding

- Characteristic changed after bump-bonding
- Increase of leakage current
- High operational voltage close to breakdown voltage required to achieve low noise close, while depletion voltage measured at wafer level is normal
- Modules suffer from irreversible damage after typically one day of operation



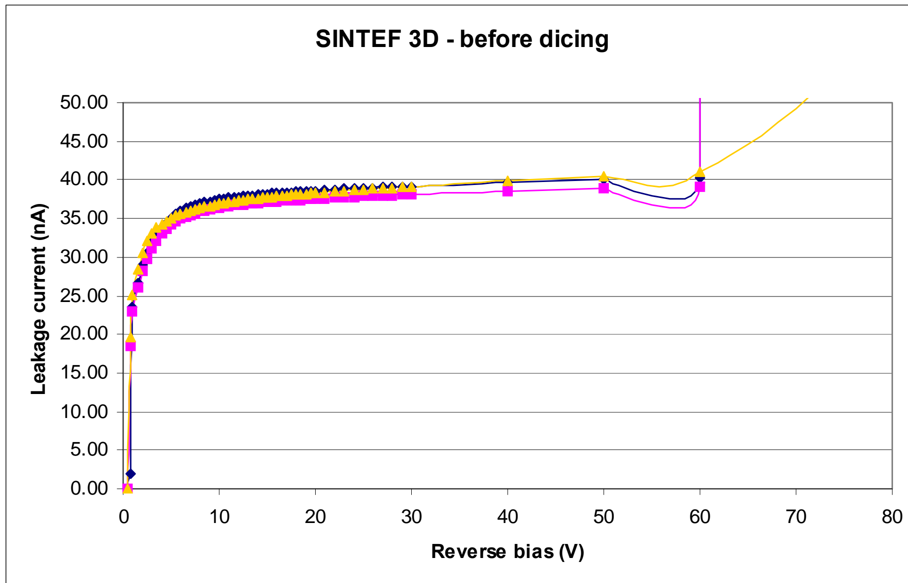


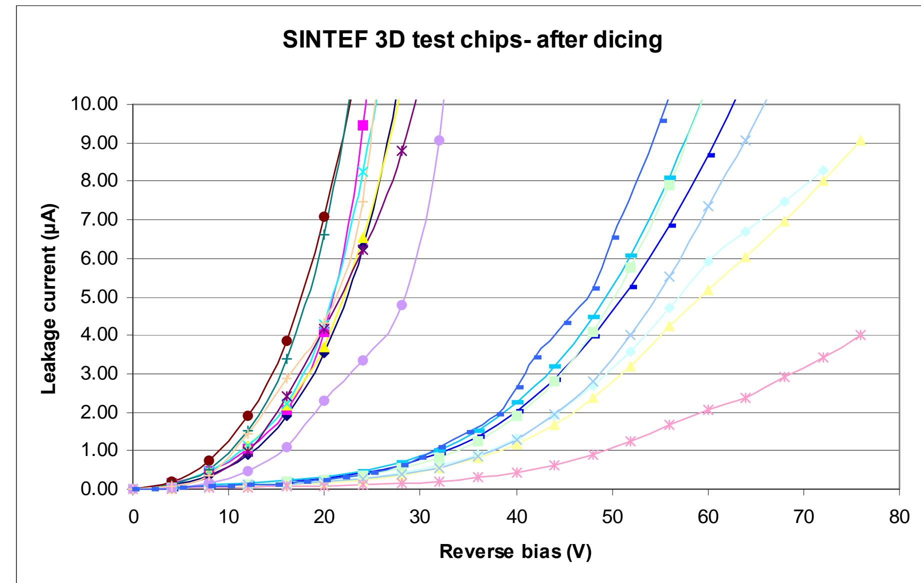
Total dark current on 4E chip with 2700 pixels at wafer/chip level

Total dark current on same chip measured after bump-bonding

IV measurements before / after dicing

- IV measurements on pixels test structures
- Short distance from active edge to saw line





Total dark current on pixel test structures at wafer level before dicing

Total dark current on same chips measured after dicing. Highly increased leakage

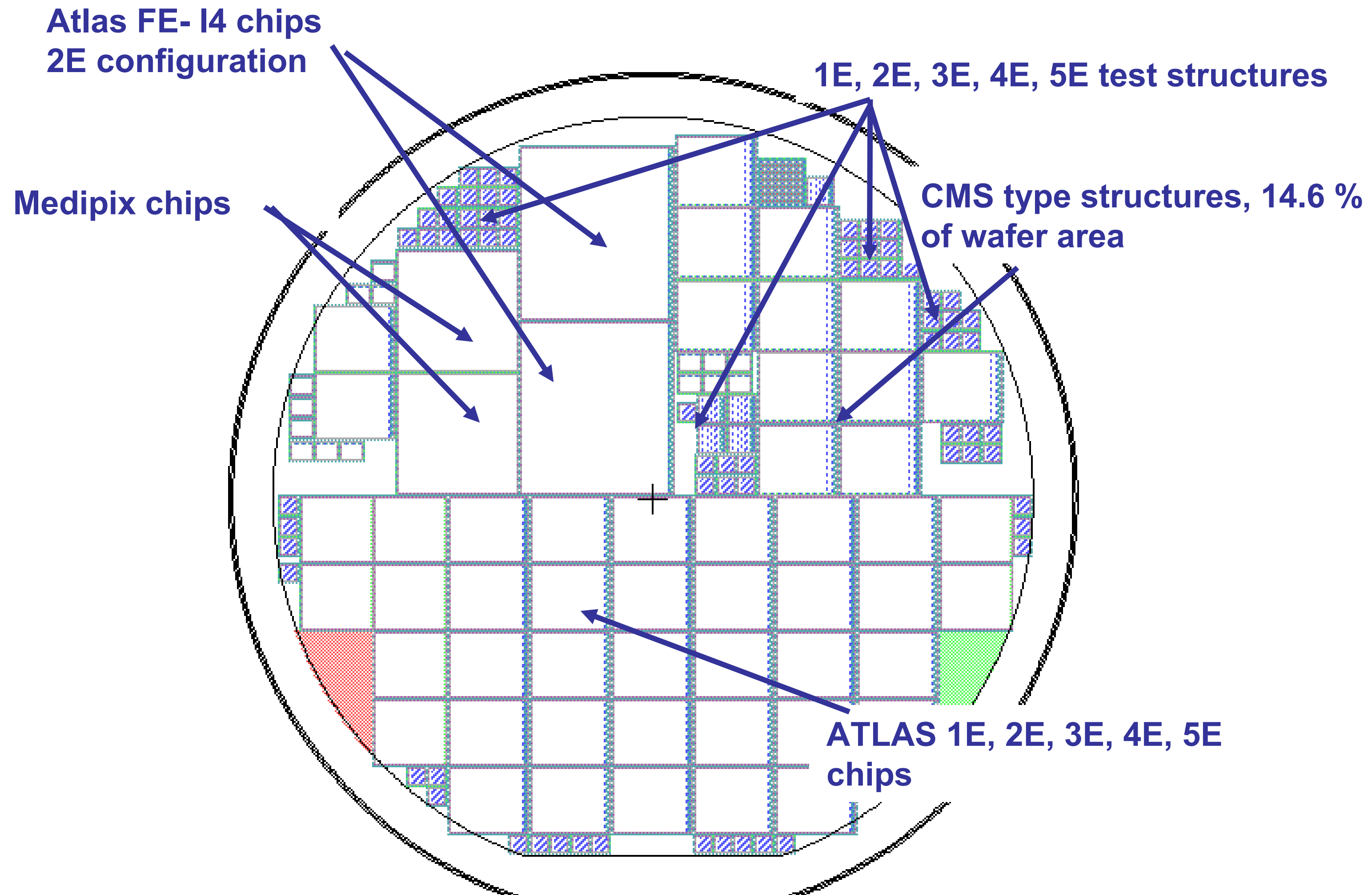
Second 3D-run at SINTEF
n- readout devices on p-wafers.

Wafer specifications

4 – inch ≥ 10000 Ωcm	Depl. Voltage		
200 µm, 17 pcs	4E	3E	2E
285 µm, 6 pcs	≤ 4.4 V	≤ 11 V	≤ 32 V

1. Based on experiences from first run focus on:
   - Improve wafer stress, bow and topography to improve lithography and reduce breakage
2. New AMS 200 ISPEEDER "IPROD" used for DRIE etching
3. Mask design includes ATLAS, CMS and Medipix type devices.

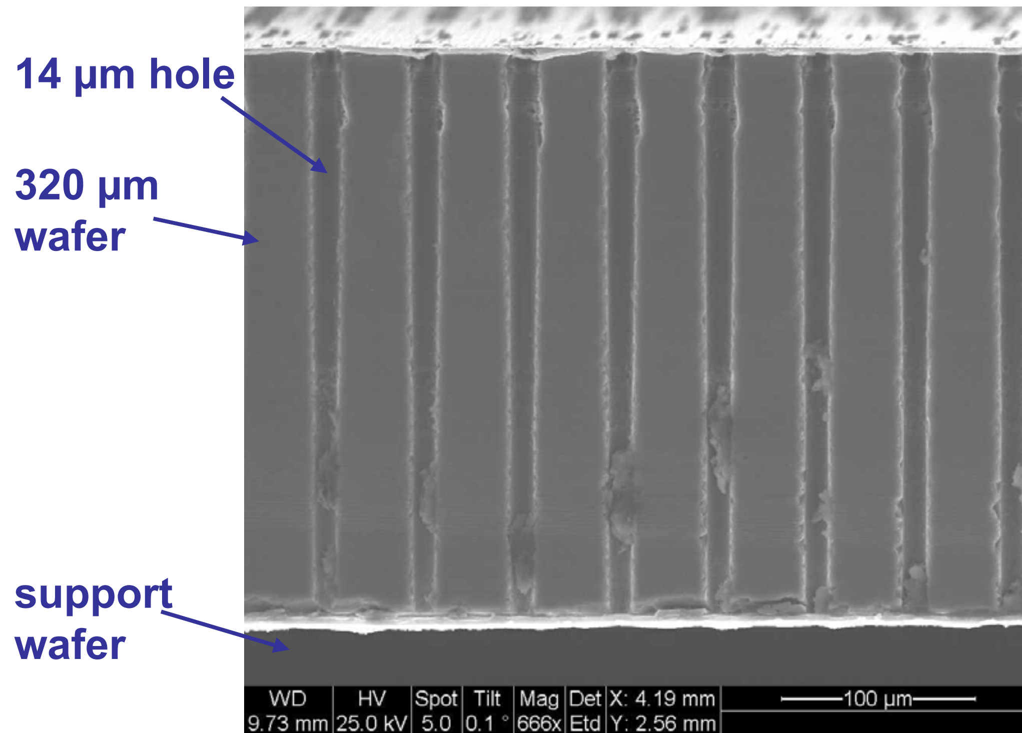
MASK LAYOUT FOR 2nd RUN

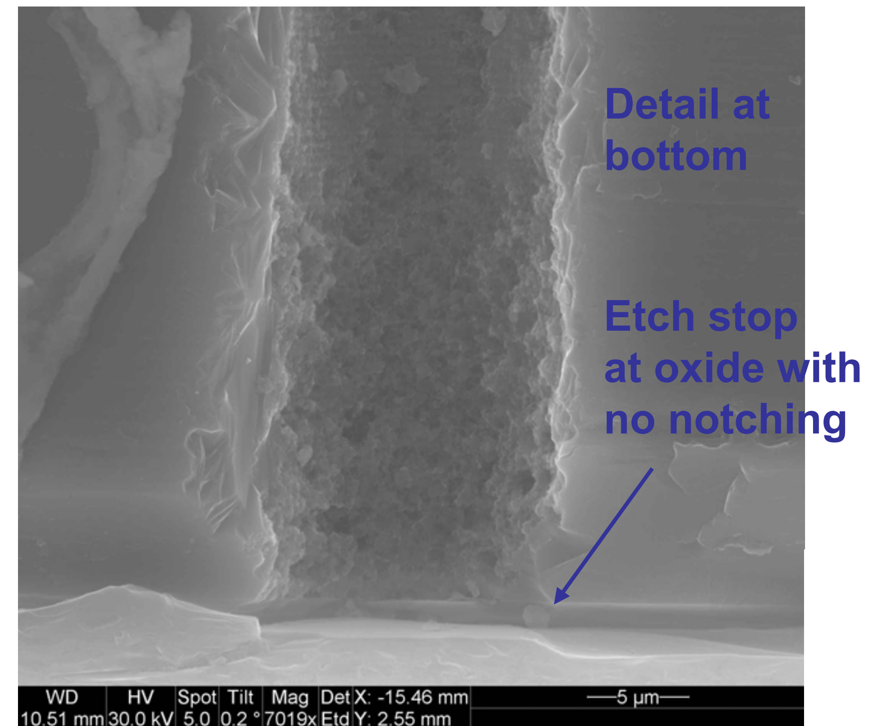


Tuning of AMS 200 ISPEEDER “IPROD” for 2nd SINTEF 3D – run

14 µm holes through 320 µm thick wafer bonded to support wafer in 40 min etch time

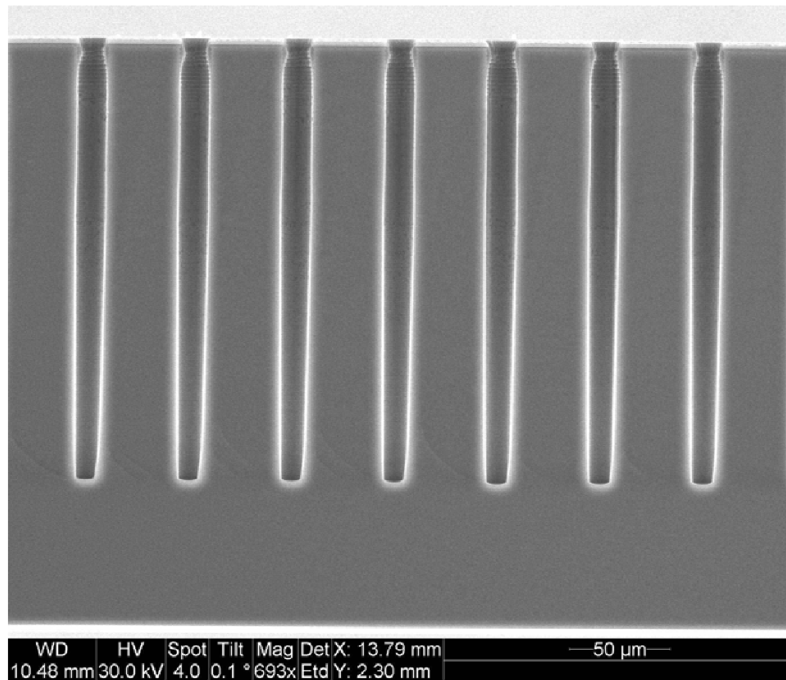
Etch stop against oxide with no notching



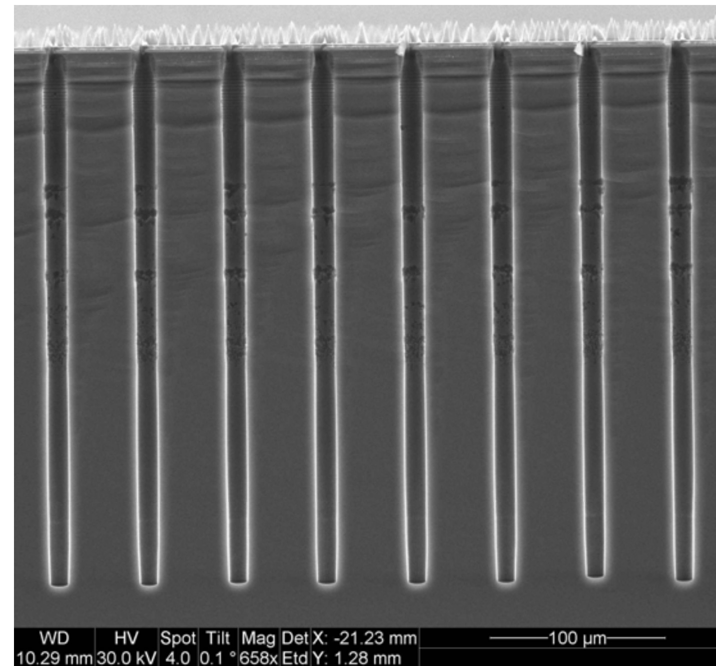


Further tuning of AMS 200 ISPEEDER “IPROD” after installing high selectivity kit Etching silicon with ≈ 1000 selectivity to SiO_2

14 µm holes, 200 and 320 µm deep



<u>200 µm deep hole</u>
No problem at wafer edge due to high silicon to SiO_2 selectivity



<u>320 µm deep hole</u>
Still need manual protection with photo resist to keep Al mask at edge for protection.

Experiences so far from 2nd run

Positive

- No wafer breakage
- No extensive warping or stress
- Technical Performance of AMS 200 ISPEEDER “IPROD” DRIE tool
  - High quality electrode holes
  - Fast etch time

Negative

- Reliability of AMS 200 ISPEEDER “IPROD” DRIE tool
  - Down time due to chuck breakdown. Had to be replaced
  - Down time due to crashed hard disc
  - Down time due to crashed fan (down since Easter!!)
  - Service situation unclear, Alcatel sold product line to TEGAL

} Delay

Updated project plan 2nd run

ID		Task Name	Duration	Start	Finish
1		PLANNING 3-D RUN II			
2		ISSUE 06, MAY 29, 2009			
3					
4		1. 3D-run II	285 days	Mon 04.08.08	Fri 04.09.09
5					
6	✓	1.1 Layout / mask tooling	80 days	Mon 04.08.08	Fri 21.11.08
11					
12	✓	1.2 DRIE Tuning	80 days	Mon 04.08.08	Fri 21.11.08
15					
16	✓	1.3 Completed Processing	215 days	Mon 04.08.08	Fri 29.05.09
47					
48		1.4 Remaining Processing	69 days	Tue 02.06.09	Fri 04.09.09
49		RIE oxide etch	2 days	Tue 02.06.09	Wed 03.06.09
50		DRIE etch	5 days	Mon 22.06.09	Fri 26.06.09
51		Polymer removal / aluminium e	2 days	Mon 29.06.09	Tue 30.06.09
52		Hole dope / poly dep /dope	5 days	Wed 01.07.09	Tue 07.07.09
53		2. Hole fill Stanford	3 wks	Wed 08.07.09	Tue 28.07.09
54		Remove exess poly	2 days	Wed 29.07.09	Thu 30.07.09
55		RIE Nitride etch	2 days	Fri 31.07.09	Mon 03.08.09
56		Segregation anneal	2 days	Tue 04.08.09	Wed 05.08.09
57		Photolith. RNCT mask	2 days	Thu 06.08.09	Fri 07.08.09
58		Aluminium sputter	1 day	Mon 10.08.09	Mon 10.08.09
59		Photolith. METAL mask	2 days	Tue 11.08.09	Wed 12.08.09
60		Anneal / Sintring	1 day	Thu 13.08.09	Thu 13.08.09
61		Passivation dep	2 days	Fri 14.08.09	Mon 17.08.09
62		Photolith. Passivation mask	2 days	Tue 18.08.09	Wed 19.08.09
63		RIE etch	1 day	Thu 20.08.09	Thu 20.08.09
64		Wafer Test	10 days	Fri 21.08.09	Thu 03.09.09
65		Finnish	1 day	Fri 04.09.09	Fri 04.09.09

Planned finish beginning of September 2009

Status on 2nd run

Status

- N-electrodes etched, doped and filled with poly-silicon at Stanford
- 31 out of 48 major process steps completed
- Ready and waiting for DRIE etch of P-electrodes and active edge. Tool down since Easter. Access probably not before Week 25/26
- Planned finish beginning of September 2009.

Causes for delays compared to original

- Long delays in getting CMS and Medipix chip layout
- Unclear funding on part of the Norwegian Research Council for 2009. Funding secured in February after full stop in January.
- Down time on “IPROD” DRIE tool and queuing for access

Required number of chips and wafers

Requirement: 520 FE-I4 chips plus spares

Chip size: ≈ 18.5 x 20.5 mm^2

Estimated number of wafers

Wafer size	Chips/wafer	Chips/wafer 50% yield	Number of wafers
4-inch	12	6	87 + spares
6-inch	26	13	40 + spares

At this stage SINTEF would prefer 6-inch wafers

- **Better capacity and more cost efficient**
- **Less reconfiguration of tools**
- **SINTEF policy to direct future production to 6-inch wafers**

SINTEF capacity for 3D-processing

Volume: 100 4” or 50 6” wafers

Production time: 2011

Risk analysis

Process steps	Risks / bottlenecks	Mitigating actions
Wafer bonding	0	
Oxidations, doping, diffusions, photolithography Note 1	0	
Metallization Note 1	0	
Electrode DRIE etch	Excessive down time and problems with access to tool	Share work with Stanford
Electrode poly-silicon filling	Limited to 1 μm films	Do filling at Stanford

Note 1: Planar processing capacity is 10.000 6-inch wafers / year on one shift, 4 mask process

Cost analysis (Not a quote!)

Assumptions:

- **Based on SINTEF 2009 industrial rates**
- **Exchange rate as per May 28, 2009 : € 1.00 = NOK 8.92**
- **Cost do not include design, photo mask layout and tooling**

Process steps	Cost (K€) 100 4 " wafers	Cost (K€) 50 6 " wafers
Wafer bonding and planar processing (oxidations, doping, diffusions, metallization, photolithography, passivation)	290	190
P- and N- electrode and active edge formation (aluminium masking, DRIE etch, first 1 μm poly-silicon film, doping)	162	93
Electrodes and active edge poly-silicon fill	Stanford	Stanford

Risk: **NOK may bounce back to an exchange rate ≤ 8.00**
(€ 1.00 = NOK 7.89 as per May 28, 2008)

Conclusions

Technically 2nd SINTEF 3D-lot has run smoothly so far

New IPROD DRIE tool give high quality electrode holes and fast etch times

However, reliability of IPROD tool not convincing with 3 long down periods so far. Large delays compared to project plan

Processing of the required number of FE - I4 chips more cost effective on 6-inch wafers. Estimated cost saving of 169 K€ compared to processing on 4-inch wafers

To reduce risks a work share should be agreed between Stanford and SINTEF, and especially on electrode and active edge formation. Possible cost reductions

Electrode poly-silicon filling at Stanford. So far SINTEF has not identified any other source

Thank you for your attention!